



Product Change Notification / RMES-14NRSU939

Date:

19-Apr-2023

Product Category:

AntiFuse FPGAs, General Purpose FPGAs, Radiation Tolerant FPGAs, System On Chip FPGAs

PCN Type:

Manufacturing Change

Notification Subject:

eSign # E000169897 Final Notice: Release of updated Synplify Pro ME version S-2021.09M-SP2 synthesis software bundled with Libero SoC v2022.3 for various FPGA devices.

Affected CPNs:

[RMES-14NRSU939_Affected_CPN_04192023.pdf](#)
[RMES-14NRSU939_Affected_CPN_04192023.csv](#)

Notification Text:

PCN Status:Final Notification

PCN Type:Manufacturing Change

Microchip Parts Affected:Please open one of the files found in the Affected CPNs section.
Note: For your convenience Microchip includes identical files in two formats (.pdf and .xls)

Description of Change:Release of updated Synplify Pro ME version S-2021.09M-SP2 synthesis software bundled with Libero SoC v2022.3 as described in the attached customer notification details.

Note:

Libero SoC v2022.3 was released on December 16, 2022, and is available for download on the webpage below.

<https://www.microchip.com/en-us/products/fpgas-and-plds/fpga-and-soc-design-tools/fpga/libero-software-later-versions#Download%20Software>

Pre and Post Change Summary:

	Pre Change	Post Change
Software / Tool	All Synplify Pro releases prior to Synplify Pro ME version S-2021.09M-SP2 and Libero SoC v2022.2 or earlier versions	Synplify Pro ME release S-2021.09M-SP2 and later, bundled with Libero SoC v2022.3 and later. The issue has also been fixed in Synplify Pro standalone release T-2022.09 and later.

Impacts to Data Sheet:None

Change Impact:None

Reason for Change:Release updated Synplify Pro ME version S-2021.09M-SP2 synthesis software bundled with Libero SoC v2022.3 to prevent incorrect VHDL expression evaluation during compilation, when performing subtraction with a real constant number operand, and an additional division/multiplication operation that uses a variable. This is to fix a VHDL compiler issue that occurs in specific VHDL expressions.

Change Implementation Status:Complete

Estimated First Ship Date:December 16, 2022 (date code: 2251)

Note: Please be advised that after the estimated first ship date customers may receive pre and post change parts.

Time Table Summary:

	December 2022					>	April 2023				
Workweek	4 9	5 0	5 1	5 2	5 3		1 4	1 5	1 6	1 7	1 8
Final PCN Issue Date									x		
Implementation Date			x								

Method to Identify Change:Not applicable. New software is available as defined above.

Qualification Report:Not Applicable

Revision History:

April 19, 2023: Issued final notification to reveal the appropriate software release.

The change described in this PCN does not alter Microchip's current regulatory compliance regarding the material content of the applicable products.

Attachments:

[CN_SynPro_FPGA_VHDL_Compiler_Libero_2022p3.pdf](#)

Please contact your local [Microchip sales office](#) with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

5962-0054301QXC
5962-0054301QYC
5962-0054302QXC
5962-0054302QYC
5962-0120303QUF
5962-0150805QXC
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U1AFS1500-FGG256
U1AFS1500-FGG256I
U1AFS250-FG256
U1AFS250-FG256I
U1AFS250-FGG256
U1AFS250-FGG256I
U1AFS600-FG256
U1AFS600-FG256I
U1AFS600-FGG256
U1AFS600-FGG256I



Customer Notification (CN)

Subject: Synplify Pro FPGA Synthesis VHDL Compiler Issue

Jan 16th, 2022

Description:

This customer notification applies to FPGA Synthesis software used with Microchip's FPGAs and Libero SoC design tool suite. Synplify Pro ME version S-2021.09M-SP2 synthesis software bundled with Libero SoC v2022.3 has been updated to fix a VHDL compiler issue that occurs in specific VHDL expressions, as described below. This issue has also been fixed in Synplify Pro standalone all-vendor version T-2022.09.

Reason for Change:

Prior to Synplify Pro ME version S-2021.09M-SP2 and all-vendor version T-2022.09, Synplify Pro synthesis software could incorrectly implement VHDL expressions containing a subtraction with a real constant number operand, and an additional division/multiplication operation that uses a variable. The issue occurs when the division/multiplication using a variable occurs in either the minuend or subtrahend terms of the subtraction operation.

The following scenarios are incorrectly implemented:

1. Variable in the denominator:

```
CONSTANT rec_elem : REAL := 2.0;  
zout : NATURAL := NATURAL((3.0/rec_constant.rec_elem) - 1.0);
```

Result without fix: 31'h7FFFFFFE

Result with fix: 31'h00000000

2. Multiplication operation:

```
CONSTANT rec_elem : REAL := 3.0;  
zout : NATURAL := NATURAL((3.0 * rec_constant.rec_elem) - 2.0);
```

Result without fix: 31'h0000000B

Result with fix: 31'h00000007

3. Variable in the numerator:

```
CONSTANT rec_elem : REAL := 3.0;  
zout : NATURAL := NATURAL((rec_constant.rec_elem / 3.0) - 1.0);
```



Result without fix: 31'h00000002

Result with fix: 31'h00000000

4. INTEGER in the expression:

```
CONSTANT rec_elem : REAL := 3.0;
```

```
zout : INTEGER := INTEGER((rec_constant.rec_elem / 3.0) - 1.0);
```

Result without fix: 31'h00000002

Result with fix: 31'h00000000

The issue occurs regardless of whether the division/multiplication using a variable occurs in the minuend or subtrahend terms of the subtraction operation.

In the scenarios affected, prior releases of Synplify Pro performed an incorrect optimization during the subtraction and in some cases converted the subtraction into addition.

All Microchip FPGA technologies supported by Synplify Pro, as well as all other vendor FPGA technologies supported in standalone Synplify Pro software, were affected in prior releases.

Application Impact:

During design verification, an affected design would experience a simulation mismatch between RTL and post-synthesis simulation results. The post-synthesis design functionality would not match the pre-synthesis RTL simulation functionality.

Required Action:

New and ongoing designs:

Microchip recommends upgrading to Synplify Pro ME version S-2021.09M-SP2 or later, bundled with Libero SoC v2022.3 or later, to prevent this VHDL compiler implementation issue from affecting the design.

Designs completed prior to the release of Synplify Pro ME version S-2021.09M-SP2 or Libero SoC v2022.3:

No further actions are listed if the affected design conditions described above don't apply to the design, or if the design has successfully completed both post-synthesis simulation and full system functional hardware testing on every production unit over the entire operating conditions range.

Completed designs that use the affected VHDL expressions and observe the issue described above:



Upgrade the synthesis tools and re-synthesize the design using Synplify Pro ME version S-2021.09M-SP2, or Synplify Pro standalone version T-2022.09, or later.

Contact Information:

If you have any questions about this subject, contact Microchip FPGA-BU Technical Support at the web portal below:

<http://www.microchip.com/support>

Regards,

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