Product Change Notification / SYST-11JVPT101

Date:

13-Oct-2021

Product Category:

Microprocessors

PCN Type:

Document Change

Notification Subject:

ERRATA - SAM9X60 Device Silicon Errata and Data Sheet Clarification Document Revision

Affected CPNs:

SYST-11JVPT101_Affected_CPN_10132021.pdf
SYST-11JVPT101_Affected_CPN_10132021.csv

Notification Text:

SYST-11JVPT101

Microchip has released a new Product Documents for the SAM9X60 Device Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at SAM9X60 Device Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change: Added silicon revision information throughout

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 13 Oct 2021

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

SAM9X60 Device Silicon Errata and Data Sheet Clarification

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SAM9X60 Device

SAM9X60 Device Silicon Errata and Data Sheet Clarifications

SAM9X60 Device

The SAM9X60 device that you have received conforms functionally to the current Device Data Sheet (DS60001579), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the following table. The silicon issues are summarized in 1. Silicon Issue Summary.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Data Sheet clarifications and corrections (if applicable) are located in 8. Data Sheet Clarifications, following the discussion of silicon issues.

The Device and Revision ID values for the SAM9X60 silicon device are shown in the following table.

Table 1. SAM9X60 Silicon Device Identification

Part Number	Silicon Revision	Device Identification	
		CHIPID_CIDR[31:0]	CHIPID_EXID[31:0]
SAM9X60-V/DWB	A1	0x819B35A1	0x00000000
	A0	0x819B35A2	

Note: Refer to the “Chip Identifier” and "Product Identification System" sections in the current device data sheet (DS60001579) for detailed information on chip identification and version for your specific device.

1. Silicon Issue Summary

Table 1-1. Silicon Issue Summary

Module	Item/Feature	Summary	Affected Silicon Revisions		
			A0	A1	
ROM Code	Secure Boot Mode: AES-RSA X.509 Certificate Serial Number Length Limit	The length of serial numbers is limited to 16 bytes by the ROM code.	X	X	
System Controller	System Controller Write Protection Status Register (SYSC_WPSR) Limitation	Write access violation is not reported by SYSC_WPSR.	X	X	
OTPC	OTPC Limited Number of Packets	The number of packets is limited to 2.	X	X	
	OTPC Restricted Operating Range in Write Mode	Write operations cannot be performed over the full temperature and VDDANA ranges.	X	X	
	OTPC Wrong Default Configuration	The default configuration cannot be used to access the OTP memory in Write mode.	X	X	
PMC	ULP1 Mode Entry Procedure	Spurious exit from ULP1 mode	X	X	
SMC	Register Write Protection Not Effective on SMC_OCMS Register	The register write protection is not effective on the SMC_OCMS register.	X	X	
FLEXCOM	FLEXCOM Sniffer Mode	Peripheral TWI*n+1* cannot be configured to analyze peripheral TWI*n*.	X	X	

2. ROM Code

2.1 Secure Boot Mode: AES-RSA X.509 Certificate Serial Number Length Limit

According to the standard RFC 5280 "Internet X.509 Public Key Infrastructure Certificate" section 4.1.2.2, the maximum length for serial numbers in X.509 certificates is 20 bytes.

When parsing the certificate chain in AES-RSA Secure Boot mode, the maximum serial number length allowed by the ROM code is 16 bytes.

Work Around

To use AES-RSA Secure Boot mode, do not use X.509 certificates with a serial number length higher than 16 bytes.

Affected Silicon Revisions

A0	A1						
X	X						

3. System Controller Write Protection (SYSCWP)

3.1 System Controller Write Protection Status Register (SYSC_WPSR) Limitation

The status register SYSC_WPSR does not set the write access violation status flag for write-protected registers of RTC, RTT and WDT peripherals when the bit WPEN is set in SYSC_WPMR for these peripherals. However, the write protection mechanism is active.

Work Around

None

Affected Silicon Revisions

A0	A1						
X	X						

4. OTP Controller (OTPC)

4.1 OTPC Limited Number of Packets

The number of OTP packets allowed to be written in the user area, in addition to those necessary to configure the ROM code boot features, is limited to 2. The maximum size of the payload for each packet is 8192 bits.

Work Around
None

Affected Silicon Revisions

A0	A1						
X	X						

4.2 OTPC Restricted Operating Range in Write Mode

The write operations in the OTPC cannot be performed over the full temperature and VDDANA power supply ranges specified.

Work Around
The write operations in the OTPC are restricted to the following ambient temperature and VDDANA power supply ranges:

- T_A = [0°C to 50°C]
- VDDANA = [3.15V to 3.45V]

Affected Silicon Revisions

A0	A1						
X	X						

4.3 OTPC Wrong Default Configuration

The default configuration of the OTPC cannot be used to access the OTP memory in Write mode.

Work Around
Prior to any write operation in the OTPC, the OTPC must be configured using the following code. This operation needs to be performed only once before the first write operation and whenever the peripheral reset (signal periph_nreset) is asserted.

```
#define ARRAY_SIZE(a) (sizeof(a) / sizeof((a)[0]))

/*
* writing one word lasts 350us
* the timeout was chosen to be enough for writing 10 words  **/
#define TIMEOUT 50000
#define OTPC_0    (0x1u << 0)
#define OTPC_1    16
#define OTPC_2    (0xffffu << OTPC_1)
#define OTPC_3    (0x4391u << OTPC_1)

static void otp_sam9x60_fixup(void)
{
       static const uint32_t fixup0[4] = {0x04194801, 0x01000000, 0x00000008, 0x00000000};
       static const uint32_t fixup1[4] = {0xfb164801, 0x4c017d12, 0x02120e01, 0x00004000};
```

```
__IO uint32_t *OTPC_4   = (__IO uint32_t *)((uint8_t *)OTPC + 0x090);
__IO uint32_t *OTPC_5 = (__IO uint32_t *)((uint8_t *)OTPC + 0x0A0);
__IO uint32_t *OTPC_6 = (__IO uint32_t *)((uint8_t *)OTPC + 0x0B0);
uint32_t timeout;
int i;

timeout = TIMEOUT;
*OTPC_4 = OTPC_0 | OTPC_3;
while (!(OTPC->OTPC_SR & OTPC_SR_UNLOCK) && --timeout > 0);

for (i = 0; i < ARRAY_SIZE(fixup0); i++)
       OTPC_5[i] = fixup0[i];

for (i = 0; i < ARRAY_SIZE(fixup1); i++)
       OTPC_6[i] = fixup1[i];

timeout = TIMEOUT;
*OTPC_4 = OTPC_3;
while ((OTPC->OTPC_SR & OTPC_SR_UNLOCK) && --timeout > 0); }
```

Affected Silicon Revisions

A0	A1						
X	X						

5. Power Management Controller (PMC)

5.1 ULP1 Mode Entry Procedure

If one or more read or write accesses to the PMC user interface follow the last instruction to enter ULP1 mode (set CKGR_MOR.ULP1), the ULP1 mode may be exited immediately after the entry.

Work Around

Add two dummy read accesses outside of the PMC user interface just after setting the CKGR_MOR.ULP1 bit.

Affected Silicon Revisions

A0	A1						
X	X						

6. Static Memory Controller (SMC)

6.1 Register Write Protection Not Effective on SMC_OCMS Register

The register SMC_OCMS is not write-protected when the bit WPEN is set in SMC_WPMR.

Work Around

None

Affected Silicon Revisions

A0	A1						
X	X						

7. Flexible Serial Communication Controller (FLEXCOM)

7.1 FLEXCOM Sniffer Mode

When using FLEXCOM in Sniffer mode, the peripheral TWI*n+1* cannot be configured to analyze the peripheral TWI*n* (n being the instance index of the TWI) in a full transparent mode via predefined internal connections between TWI instances.

Work Around

Configure TWI*n* to analyze TWI*n+1*.

Note: When n=12 (FLEXCOM12), n+1 means 0 (FLEXCOM0).

Affected Silicon Revisions

A0	A1						
X	X						

8. Data Sheet Clarifications

8.1 OTP Controller (OTPC)

8.1.1 OTPC Dependency to Main RC Oscillator

The main RC oscillator must be turned on prior to reading or writing the OTP memory.

9. Revision History

9.1 DS80000846E - 10/2021

Added silicon revision information throughout

9.2 DS80000846D - 09/2021

Updated SAM9X60 Silicon Device Identification table with additional chip ID
Added OTPC Dependency to Main RC Oscillator in 8. Data Sheet Clarifications

9.3 DS80000846C - 09/2020

Updated 4.1 OTPC Limited Number of Packets
Added 2.1 Secure Boot Mode: AES-RSA X.509 Certificate Serial Number Length Limit

9.4 DS80000846B - 02/2020

Added 7. Flexible Serial Communication Controller (FLEXCOM)
8. Data Sheet Clarifications: removed "EBI Controls in Special Function Registers (SFR)"

9.5 DS80000846A - 10/2019

First issue.

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Affected Catalog Part Numbers(CPN)

SAM9X60-V/DWB
SAM9X60-V/DWBVAO
SAM9X60D1G-I/4FB
SAM9X60D1GT-I/4FB
SAM9X60D5M-I/4FB
SAM9X60D5MT-I/4FB
SAM9X60D6K-I/4GB
SAM9X60D6KT-I/4GB
SAM9X60T-V/DWB
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