May 23, 2019

nexperia

Understanding Power MOSFETs

Agenda - MOSFET Parameters and Data Sheets

- Nexperia MOSFET Applications Handbook
  - Ap Notes of Interest
- Basics - MOSFET Part Numbers
  - Secret Decoder Ring
  - Data Sheet Headers
- Limiting or Maximum Values
  - Voltage, Current, Power etc.
  - Standard Derating Tables vs. Temperature
- Robustness
  - SOA – Safe Operating Area and Temperature Derating
  - Avalanche – Single Shot and Repetitive
- Static and Dynamic Characteristics
- Extended Topics
  - Thermal Loss Model
  - Understanding Snubbers
  - SOA Derating
    - Voltage and Current Scaling
    - Constant Power and Sprito Region

Power MOSFET Applications Handbook

Nexperia still prints the Big Book

- Can be downloaded from the Website.

Understanding power MOSFET data sheet parameters	1	AN11158
Power MOSFET single-shot and repetitive avalanche ruggedness rating	2	AN10273
Using RC Thermal models	3	AN11261
LFPAK MOSFET thermal design – part 1	4	AN10874
LFPAK MOSFET thermal design – part 2	5	AN11113
Using power MOSFETs in parallel	6	AN11599
Designing RC snubbers	7	AN11160
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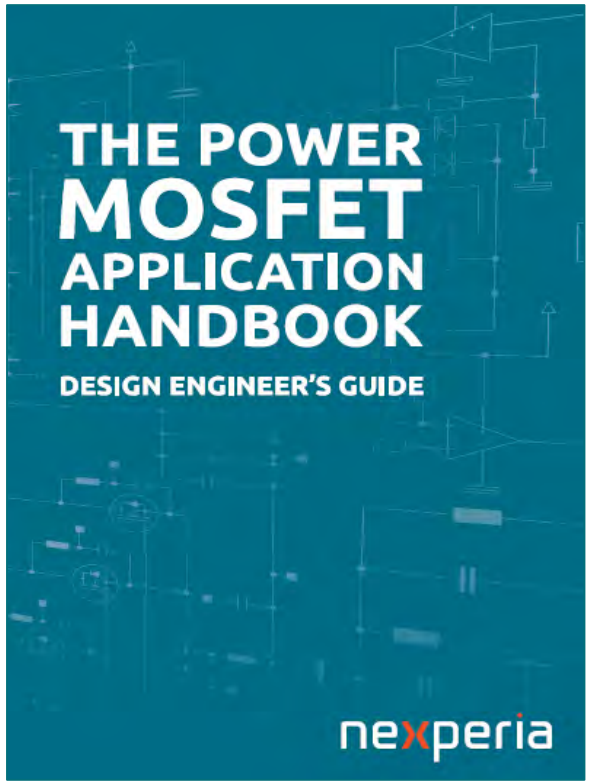
Power MOSFET frequently asked questions	9	TN00008
Abbreviations		



Other Applications Notes

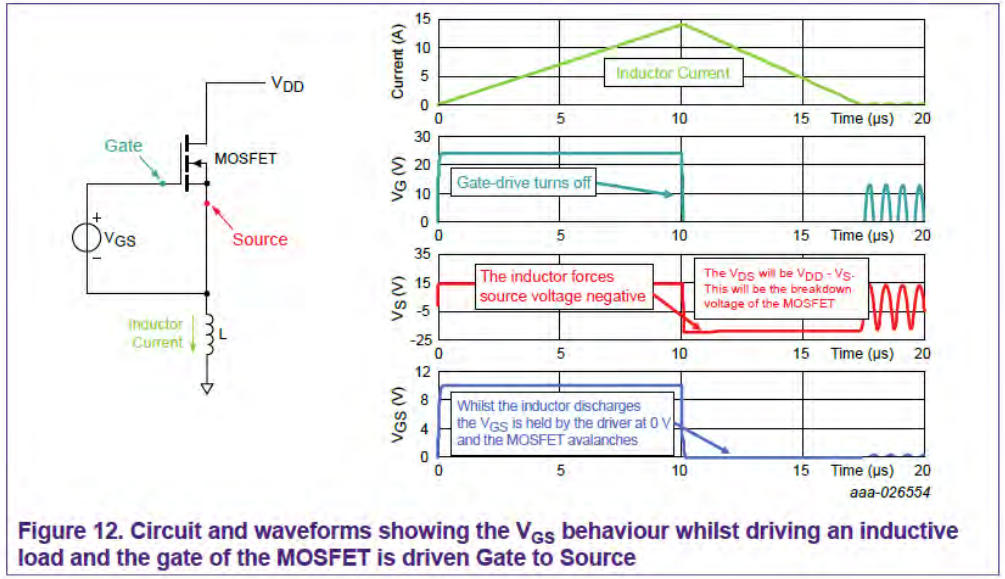


Figure 12. Circuit and waveforms showing the V_{GS} behaviour whilst driving an inductive load and the gate of the MOSFET is driven Gate to Source

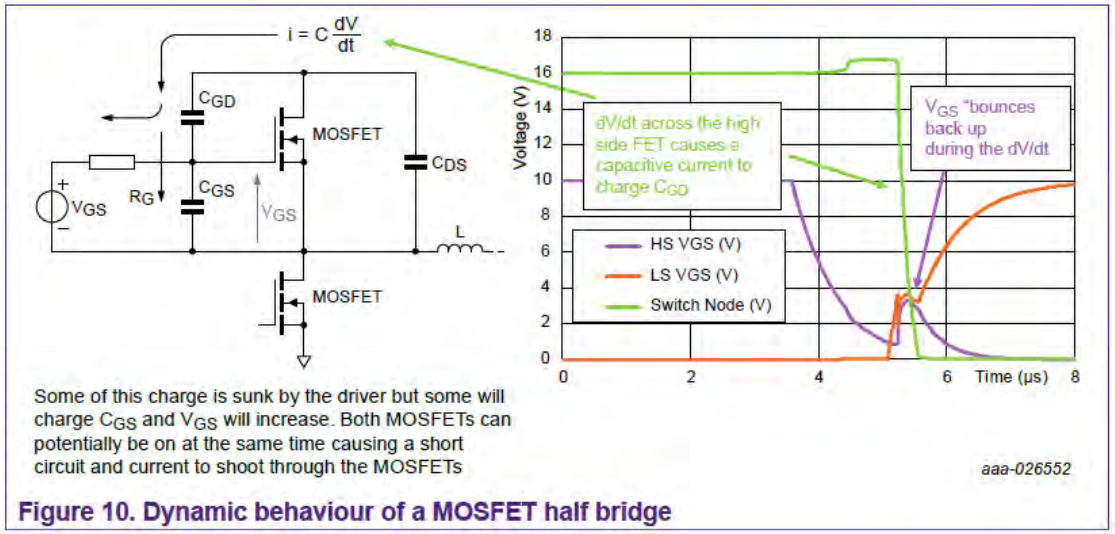


Figure 10. Dynamic behaviour of a MOSFET half bridge

Designing in MOSFETs for safe and reliable gate-drive operation

Rev. 1.0 — 31 March 2017 Application note

- **AN90001** – Explanation of Gate Oxide effects over life from **TDDB**, Gate Threshold (Vgs) decline over Temperature / Life.
- Source Inductance Effects – Package Inductance of Clip bond LFPAKxx is of minimal effect in Low Voltage applications. However, PCB layout and ground paths are pertinent.
- Parasitics C's and ½ Bridge drive, applicable to Inverters, H-Bridges, Buck Regulators, Motors, etc.

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MOSFET Basics

Data Sheet References

Many Application Notes have been written on MOSFET Data Sheets

A MOSFET datasheet generally contains:

1. A part number using the secret decoder ring of the supplier.
2. A general description including voltage, on-resistance, current ratings and package information
3. A table of absolute maximum ratings
4. A table of thermal resistance parameters
5. A table of electrical characteristics
6. Figures, including
    1. Graphs of typical characteristics
    2. Diagrams of test circuits
7. Package information

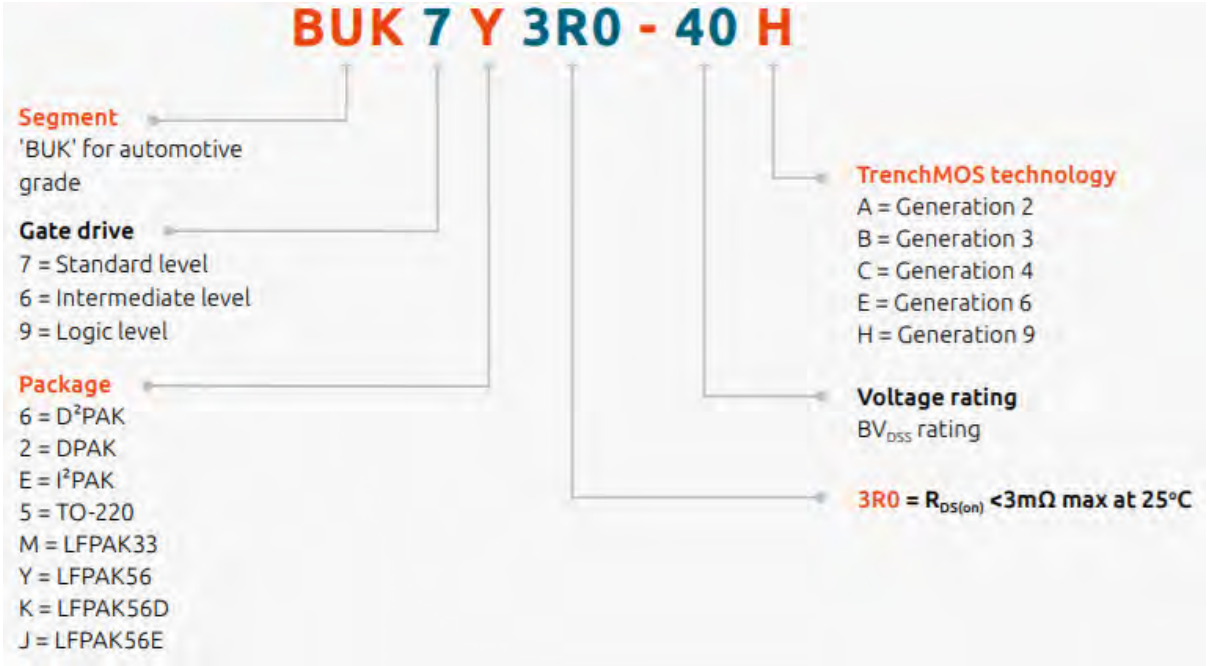
Nexperia

- *AN11158: Understanding power MOSFET data sheet parameters*, Nexperia

Others

- *How to Read a Datasheet*, Michigan State University ECE480
- *How to Read a FET Datasheet*, University of Nevada Las Vegas PHYS483
- *A Complete Guide to Data Sheets*, Allegro Microsystems
- *How to Read a Datasheet*, Analog Devices
- *Infineon OptiMOS Power MOSFET Datasheet Explanation*, Infineon

Automotive grade MOSFETs nomenclature



Product Profile

BUK9Y1R6-40H

N-channel 40 V, 1.6 mΩ logic level MOSFET in LFPAK56

31 May 2018 Product data sheet

Product Name

Product Type

Revision Control

Product Status
- Objective
- Preliminary
- Product

1. General description

Automotive qualified N-channel MOSFET using the latest Trench 9 low ohmic superjunction technology, housed in a robust LFPAK56 package. This product has been fully designed and qualified to meet AEC-Q101 requirements delivering high performance and endurance.

2. Features and benefits

- Fully automotive qualified to AEC-Q101:
  - 175 °C rating suitable for thermally demanding environments
- Trench 9 Superjunction technology:
  - Reduced cell pitch enables enhanced power density and efficiency with lower R_{DSon} in same footprint
  - Improved SOA and avalanche capability compared to standard TrenchMOS
  - Tight $V_{GS(th)}$ limits enable easy paralleling of MOSFETs
- LFPAK Gull Wing leads:
  - High Board Level Reliability absorbing mechanical stress during thermal cycling, unlike traditional QFN packages
  - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
  - Easy solder wetting for good mechanical solder joint
- LFPAK copper clip technology:
  - Improved reliability, with reduced R_{th} and R_{DSon}
  - Increases maximum current capability and improved current spreading

Quick Reference

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	-	40	V
I_D	drain current	$V_{GS} = 5$ V; $T_{mb} = 25$ °C; see Figure 1	[1]	-	-	120	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2		-	-	357	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5$ V; $I_D = 25$ A; $T_j = 25$ °C; see Figure 11		-	1.35	1.6	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	$V_{GS} = 5$ V; $I_D = 25$ A; $V_{DS} = 32$ V; see Figure 13; see Figure 14		-	40.9	-	nC

[1] Continuous current is limited by package.

Conditions are important!

When comparing MOSFETs from different suppliers, be aware of different specification conditions –

Particularly for front page headline figures.

VDS	The maximum voltage between drain and source that the device is guaranteed to block in the off state (tj ≥ 25°C).
ID	The maximum **continuous** current the MOSFET can carry when the mounting base temperature is held at 25°C with the device fully on.
Ptot	The maximum continuous power that the MOSFET can dissipate when the mounting base temperature is held at 25°C.
RDS(on)	(Drain-source on state resistance) - The typical and maximum drain to source resistance of the MOSFET in its on-state under the conditions described.
QGD	The quantity of charge transferred into the MOSFET gate pin from 0V, across the 'Miller plateau'. It is part of the Total Gate Charge. QGS(tot) + QGD= QG(tot).

Pinning Information

This section shows how the external outline and pin connections of the MOSFET relate to the internal connections to the die and the schematic symbol.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

SOT404 (D2PAK)

5. Pinning information

Table 2. Pinning information

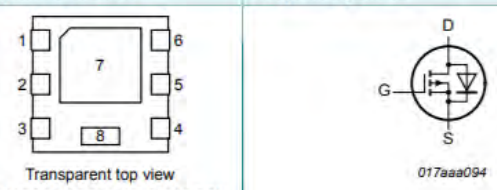
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

LFPAK56; Power-SO8 (SOT669)

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain		
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		
7	D	drain		
8	S	source		



DFN2020MD-6 (SOT1220)

Mounting base or backside tab is normally the Drain in both N and P Channel MOSETs. And this is the primary thermal path.

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MOSFET Limiting Values

Limiting Values

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	40	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20$ kΩ		-	40	V
V_{GS}	gate-source voltage	DC		-10	10	V
		Pulsed		-15	15	V
I_D	drain current	$T_{mb} = 25$ °C; $V_{GS} = 5$ V; see Figure 1	[1]	-	120	A
		$T_{mb} = 100$ °C; $V_{GS} = 5$ V; see Figure 1	[1]	-	120	A
I_{DM}	peak drain current	$T_{mb} = 25$ °C; pulsed; $t_p \leq 10$ µs; see Figure 4		-	1363	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2		-	357	W
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25$ °C	[1]	-	120	A
I_{SM}	peak source current	pulsed; $t_p \leq 10$ µs; $T_{mb} = 25$ °C		-	1363	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 120$ A; $V_{sup} \leq 40$ V; $R_{GS} = 50$ Ω; $V_{GS} = 5$ V; $T_{j(init)} = 25$ °C; unclamped; see Figure 3	[2][3]	-	1008	mJ

Again - conditions are important to make a fair comparison between competing parts.

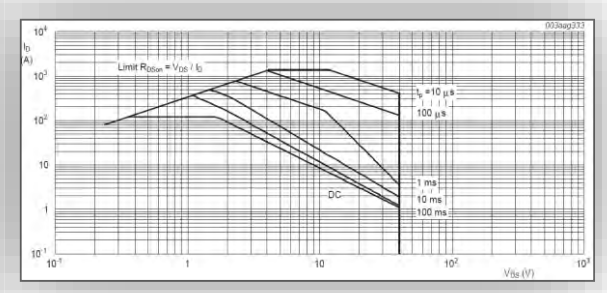
- Operation outside these limits is not guaranteed – except for avalanche ruggedness.
- They are all temperature dependent. They are quoted at Tj = 25°C and must be de-rated for Tj values <> 25°C.
- Datasheet de-rating graphs must be applied to check that the MOSFET is suitable for the worst-case application conditions).

Temperature dependence

Limiting Values

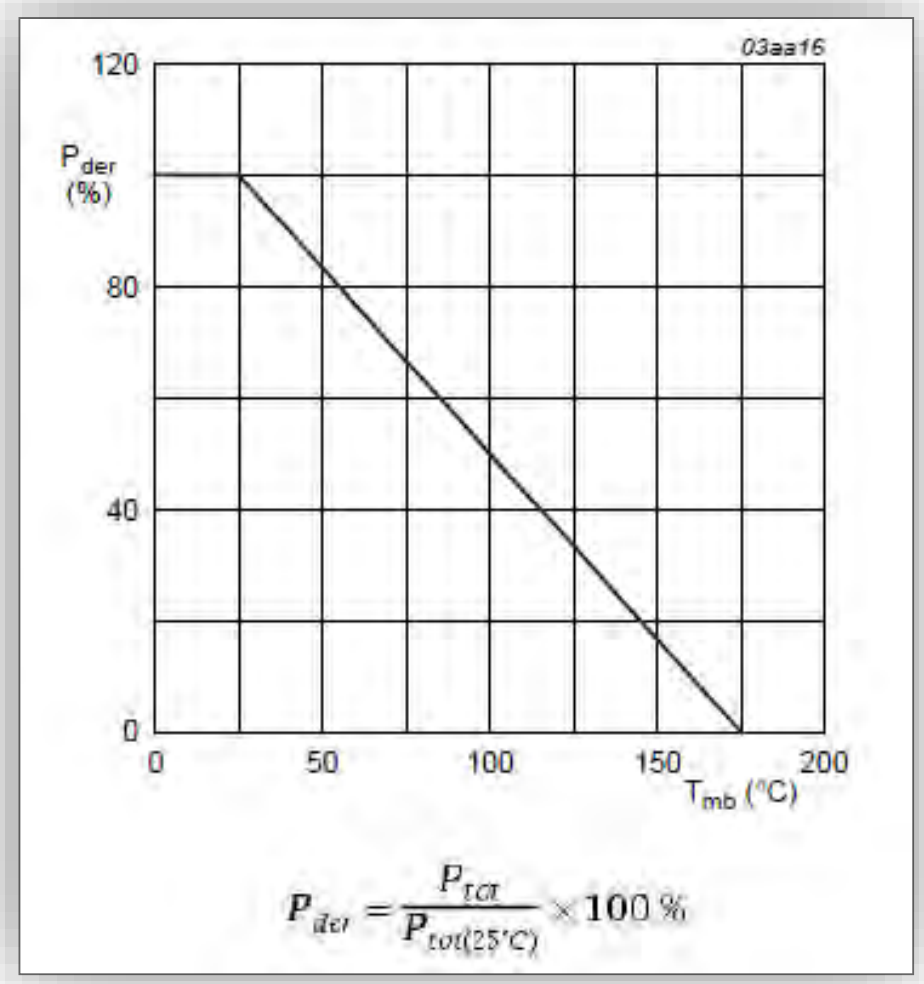
V_{DS}	The maximum voltage the device is guaranteed to withstand between the Drain and Source pins in the OFF-state **over the temperature range 25°C to 175°C.**
V_{GS}	The maximum voltage the device is guaranteed to withstand between the Gate and Source pins. (Note that TDDB also must be considered).
V_{DGR}	The maximum drain - gate voltage is the same value as the maximum V_{DS} voltage.
I_D	The maximum CONTINUOUS D.C. current that the MOSFET can handle under the specified conditions. **This is often limited by the package rather than the silicon die.** Some manufacturers state the theoretical silicon limit instead of package limit so be careful !
I_{DM}	The maximum current that the MOSFET can safely carry for a pulse time of ≤**10 µs.**
P_{tot}	The maximum continuous MOSFET power dissipation when its **mounting base temperature is HELD at 25°C**. Some MOSFET suppliers use different conditions so 'normalisation' is needed to do a valid comparison.
T_{stg} / T_j	These limit values define the safe **storage** and **junction operating** temperature range of the MOSFET.
I_S	The maximum continuous current of the MOSFET body diode. The same considerations apply as for I_D
I_{SM}	The maximum current that the MOSFET body diode is guaranteed to carry for a pulse time of ≤10 µs.

SOA Curve



Power Dissipation Derating

- The maximum (steady state) power dissipation allowed in the MOSFET is the power that would raise its junction temperature to **175°C** when its mounting base temperature is held at **25°C**.
- At T_{mb} = **25°C**, **100%** of the power (**357W**) can be dissipated. This would cause a **150°C** (K) Tj rise.
- At T_{mb} = **100°C**, **50%** of the power (**178W**) can be dissipated. This would cause a **75°C** (K) Tj rise.
- At T_{mb} = **175°C**, power dissipation >**0W** in the die would result in a Tj > 175°C.

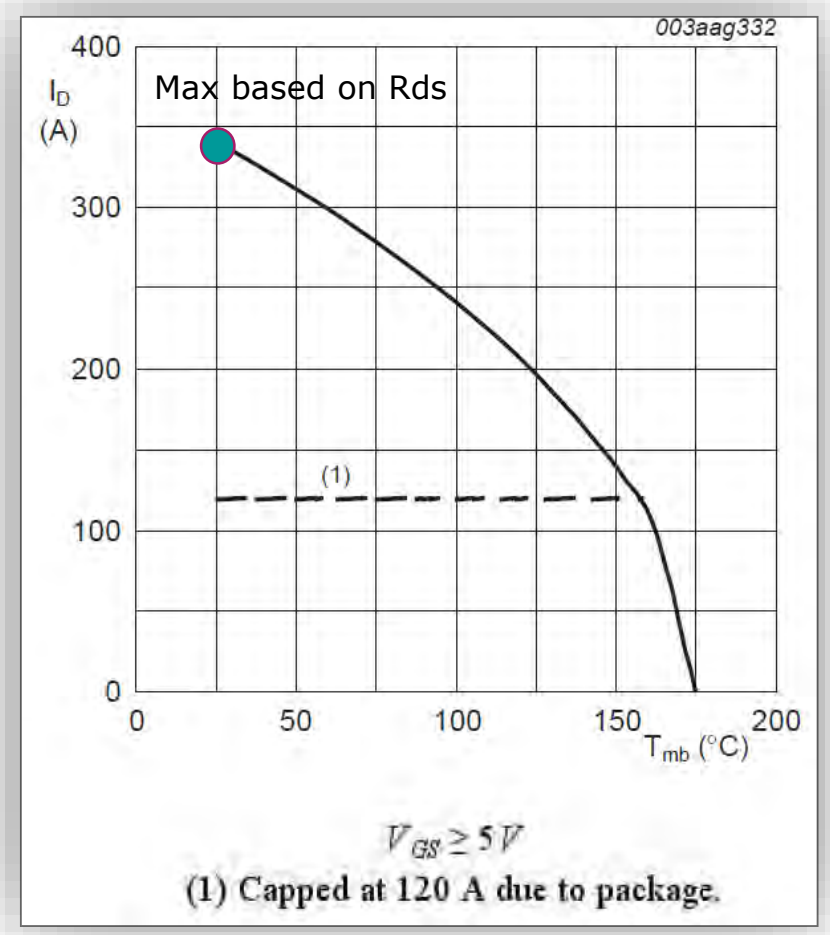


Continuous Drain Current Derating

- Continuous drain current is limited to a maximum of **120A by the package**.
- At high mounting base temperatures, maximum continuous drain current is limited by maximum die temperature rather than the package limit.
- This limit assumes that the die R_{dson} is at its maximum and die temperature is 175°C (**$Rds_{(ON)\_max.@175°C}$**)
- The maximum current at a given mounting base temperature can be calculated from the equation

$$I_D = \sqrt{(P / Rds_{(ON)\_max.@175°C})}$$

- **P** is derived from **P_{tot}** by applying the previous graph
- **$Rds_{(ON)\_max.@175°C}$** is stated on the datasheet (see slide 13)



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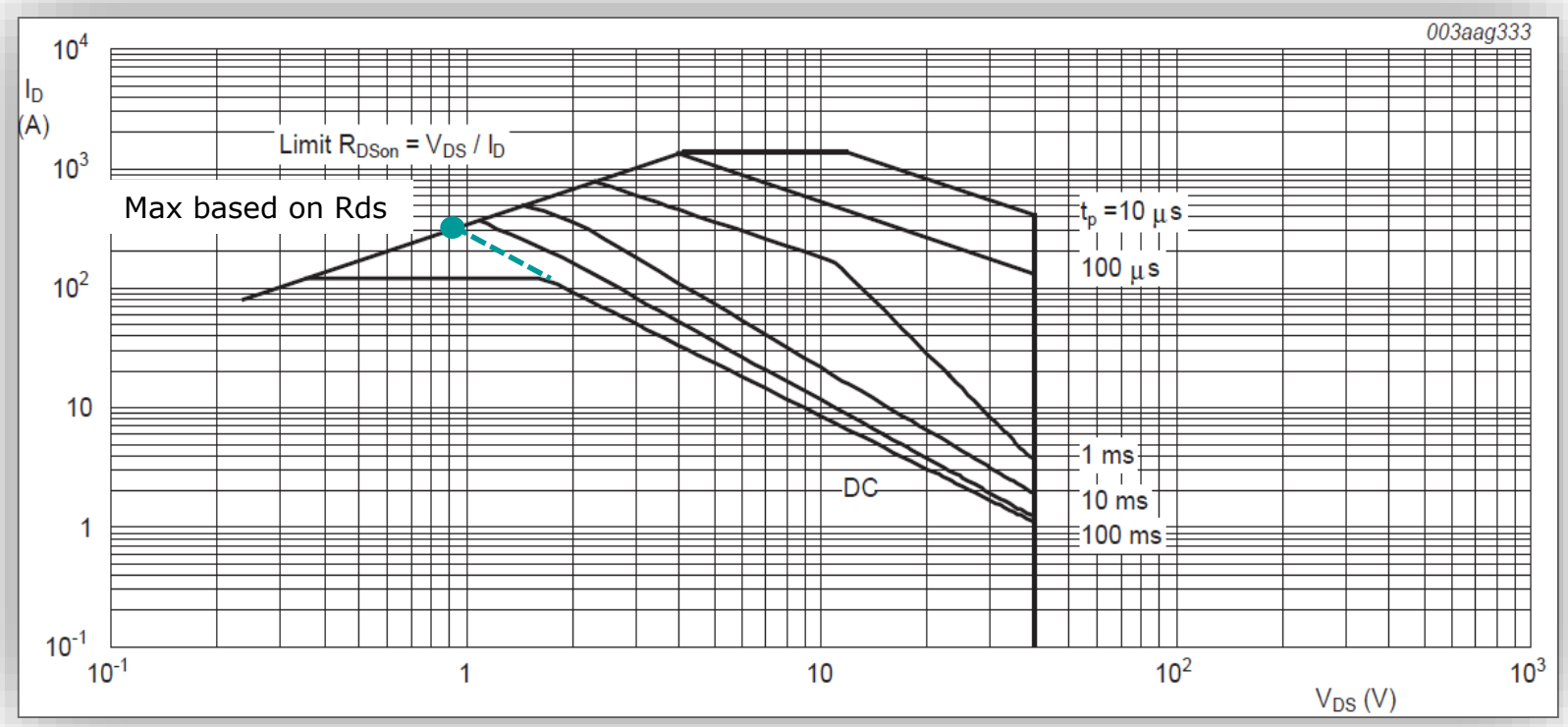
MOSFET Robustness

Safe Operating Area - SOA

- The SOA curves show the permitted voltage – current – time envelope limit for MOSFET **LINEAR MODE** operation. In this zone the MOSFET is not fully enhanced (it is between its OFF and ON states)
- The SOA lines are for a **single rectangular power pulse with initial T_j = 25°C; initial Tmb = 25°C**.



- If initial Tj is >25°C the graph **must be de-rated** in a similar way to power and current de-rating. If possible **this should be done by reducing V_{DS}**.
- Often the power pulse will not be rectangular (e.g. inductive load active clamping). **Nexperia Applications Engineers would be happy to advise in such cases**.

SOA Derating Example (Vds Scale Method)

BUK7880-55 Example

- SOA current pulse is a square wave. Therefore with constant voltage and a constant Current, **V * I** = a constant **Power.**

- The die heating is determined by the RC thermal model and is a scalable function with respect to Power. (i.e. – half the Power for a fixed pulse time will yield half the thermal rise at the die). The SOA curve represents a Power Level for a fixed pulse time, or a fixed amount of energy.

    - Scalable function: f(ax) = af(x)

- The SOA curve is for a starting temp of 25C. The max die temp is 150C. This is a temperature differential of 125C.

- For a 50C starting temperature for single event SOA pulse, the differential die temp allowed is 150C – 50C = 100C. Therefore the energy to get a die temp of 150C is
    - 100C / 125C = 80%

- As **V * I = Power**, we can adjust the 25C x-axis Voltage scale to achieve an 80% energy level in the same pulse period at 50C, as shown.

SOA Curve for BUK7880-55A

Scaled to 80% for 50C Solder Point starting temperature

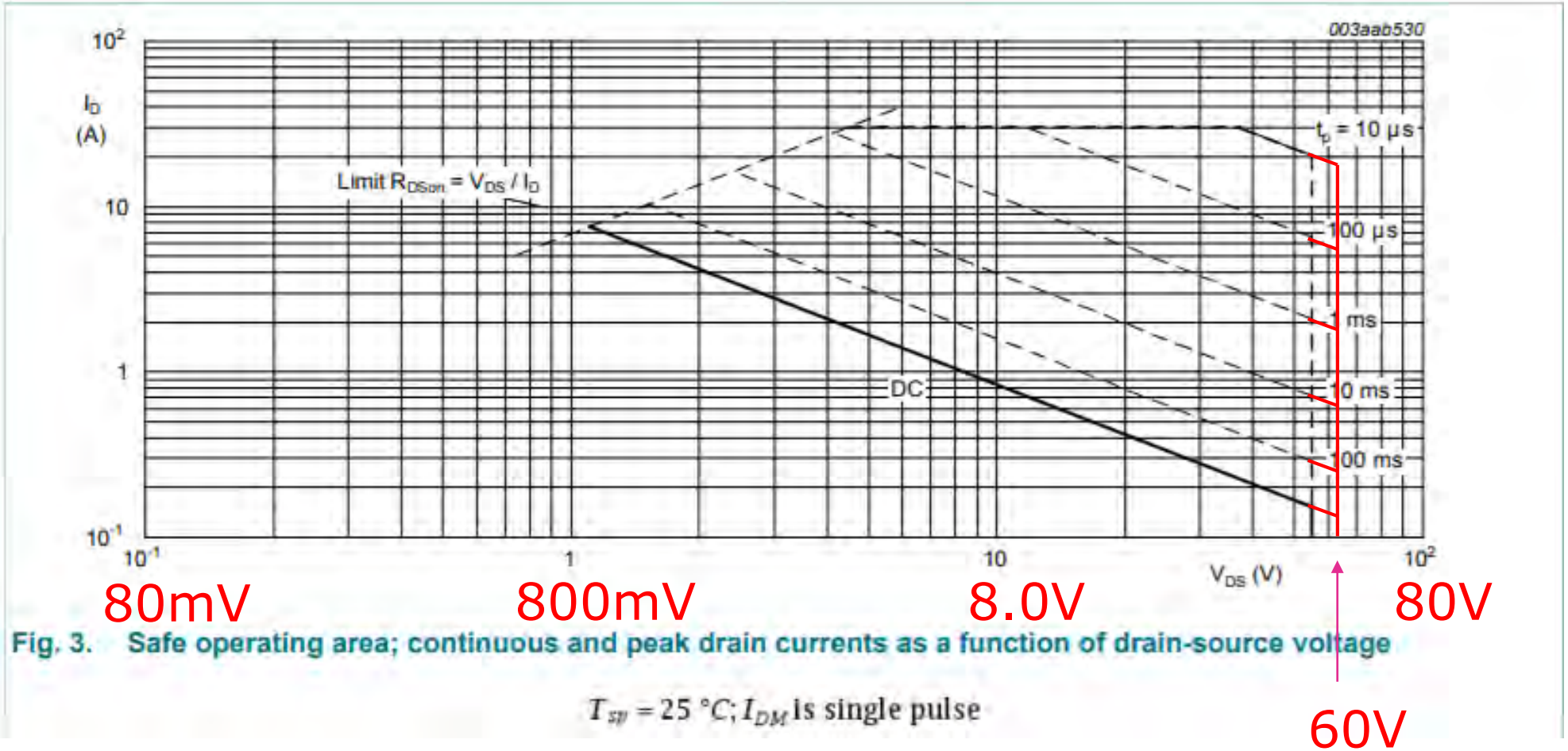


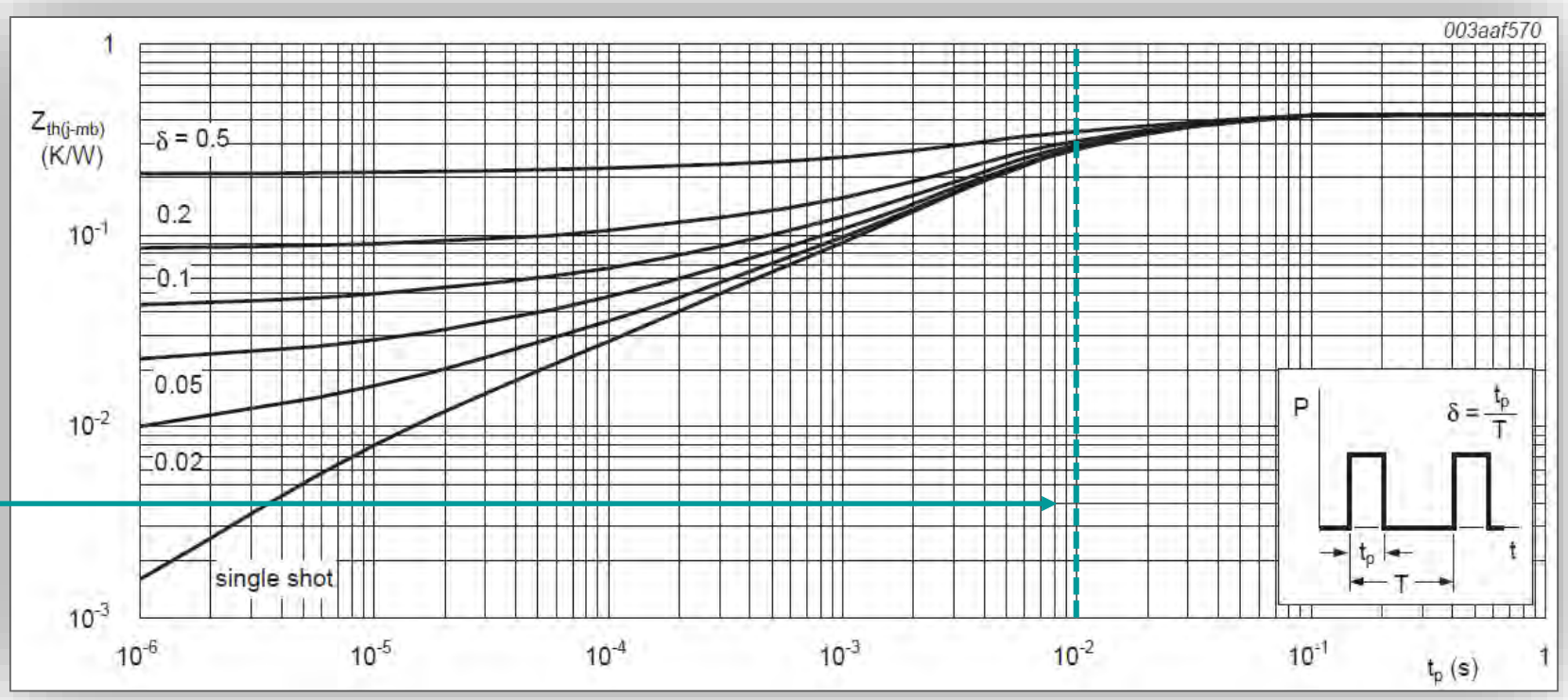
Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{sp} = 25\ °C; I_{DM}$ is single pulse

Tsp = 50C Derating

Thermal Characteristics

- Thermal impedance characteristics can be used to estimate MOSFET junction temperature rise caused by a single power pulse or a sequence of power pulses.
- At pulse durations where $t_p > 10^{-2}$s, **Zth = Rth** (steady state thermal resistance)
- At pulse durations < 10^{-2}s heat flow out of the die junction depends more on the die thermal capacity.



- $T_{j\_rise} = Z_{th(j-mb)} * P$; This temperature rise must be added to the initial mounting base temperature to give the actual junction temperature.
- **Thermal modelling using SPICE or Flotherm is often easier, more accurate and more informative.**

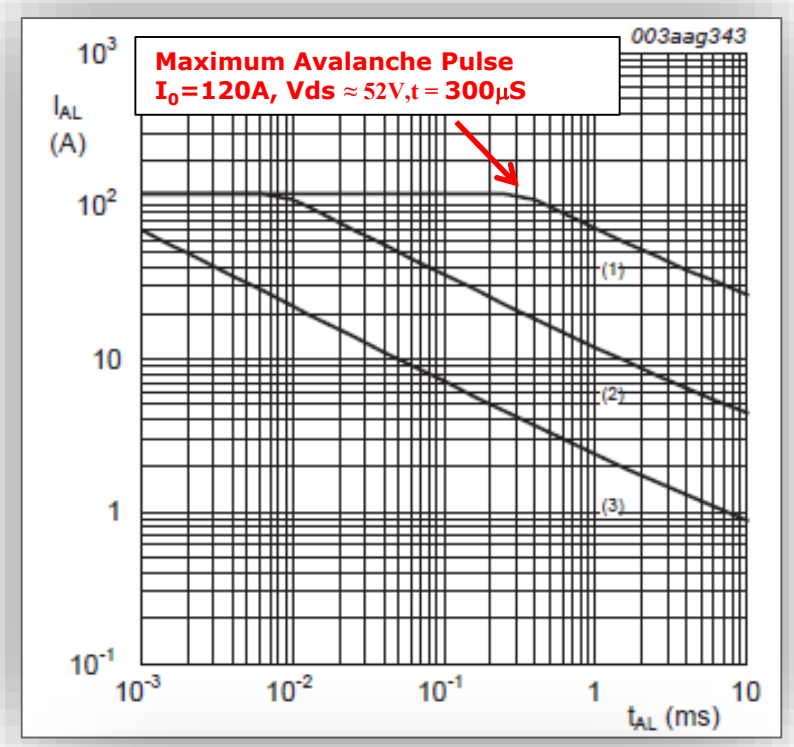
Limiting Values - Avalanche

EDS(AL)S (non-repetitive drain-source avalanche energy)	▸ The maximum single avalanche energy pulse allowed with the conditions specified. ▸ This is the avalanche energy pulse that would cause the junction temperature of the MOSFET to **rise from 25°C to 175°C** while its mounting base temperature is held at 25°C. The avalanche energy is specified for the maximum continuous drain current. ▸ Some vendors specify the avalanche energy for a lower current and longer duration, giving an apparent increase in avalanche energy. However this is only because the heat has a more time to dissipate.
EDS(AL)R (repetitive drain-source avalanche energy)	▸ The maximum avalanche energy allowed when the avalanche event is repetitive. ▸ This parameter is only listed on Nexperia MOSFET data sheets where the repetitive avalanche capability has been verified. ▸ The thermal requirements for repetitive avalanche events are that the repetitive limit line on the avalanche energy SOA graph should not be exceeded and ***average*** MOSFET junction temperature **must not exceed 170°C.** ▸ The ΔT caused by the avalanche is 10°C (10K); Tj cycles between **165°C and 175°C**

Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$T_{j(init)}$ = 25 °C; I_D = -0.85 A; DUT in avalanche (unclamped)		-	28	mJ

Avalanche Ruggedness

- In an avalanche event **Vds is taken above its limiting value** - usually by current fed from an unclamped inductive load. The MOSFET Body Diode conducts reverse (avalanche) current.
- To procure the avalanche, the MOSFET is initially switched ON (V_{gs}=5V); load current ramps up (to 120A). It is then switched OFF by pulling V_{GS} to zero; (R_{GS}= 50Ω).
- $E_{DS(AL)S}$ = 1008mJ causes Tj to rise from 25°C to 175°C.
- Avalanche voltage **(BVDSS) ≈ 1.3x V_{DS_max}**
- BVDSS increases (slightly) as die temperature increases.
- All Nexperia Automotive Power MOSFETs are subjected to TWO high energy avalanche pulses after packaging to verify their avalanche ruggedness capability.



Single-shot and repetitive avalanche rating
(1) Single pulse; T_j = 25 °C
(2) Single pulse; T_j = 150 °C
(3) Repetitive

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Static Characteristics

Static Characteristics

- Static characteristics define the steady state voltage, current and resistance ranges of the MOSFET over its full operating temperature range.
- They are the key parameters to consider when specifying a MOSFET for an application.
- Typical values are also given but **limit values should be used for design calculations.**

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	40	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 9; see Figure 10	1.4	1.7	2.1	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 9	-	-	2.45	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; see Figure 9	0.5	-	-	V
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 °C	-	0.13	1	µA
		V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 °C	-	-	500	µA
I_{GSS}	gate leakage current	V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 °C	-	2	100	nA
		V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 °C	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A; T_j = 25 °C; see Figure 11	-	1.35	1.6	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; see Figure 11	-	1.17	1.4	mΩ
		V_{GS} = 5 V; I_D = 25 A; T_j = 175 °C; see Figure 12; see Figure 11	-	-	3.1	mΩ

Temperature dependence

Transfer Characteristics

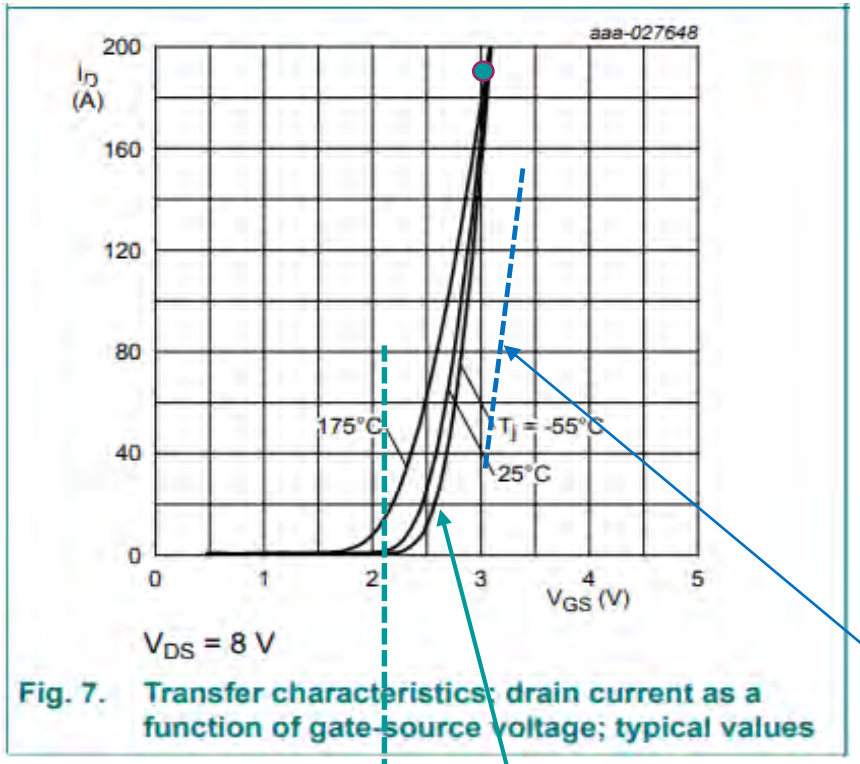
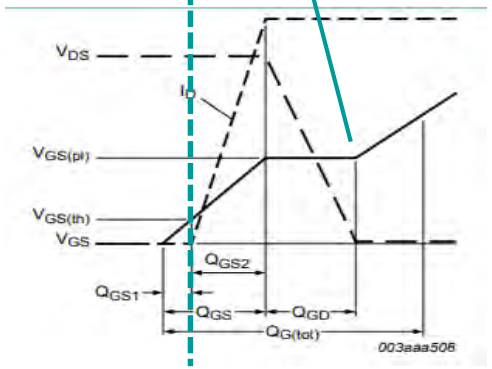


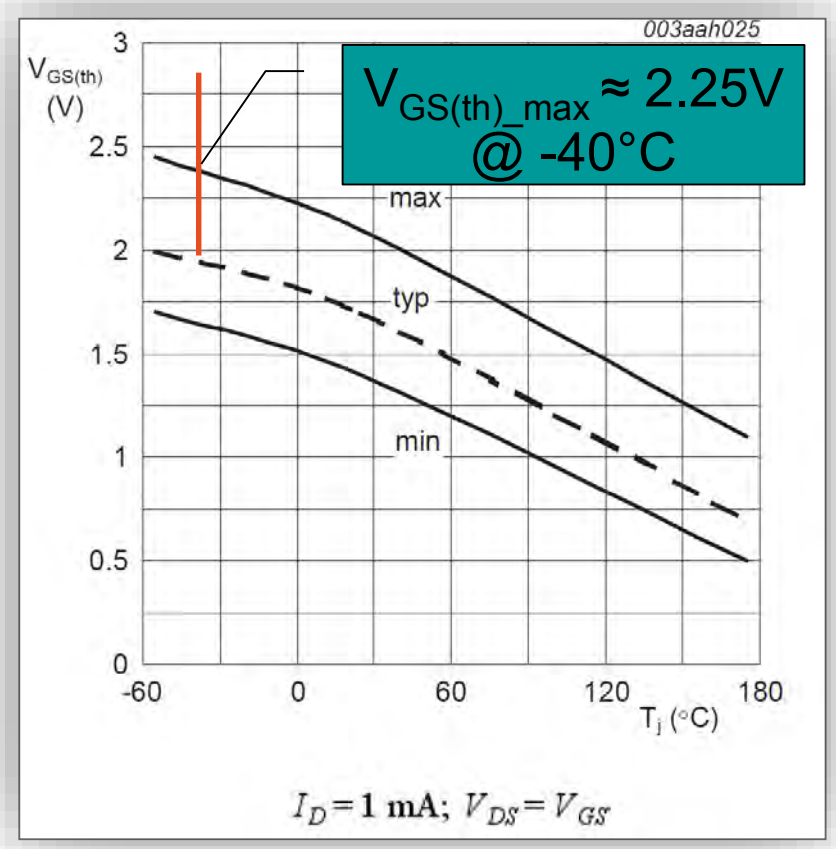
Fig. 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



- The Transfer Characteristics of the MOSFET shows its 'gain' how **I_D increases as V_{GS} increases**.
- It shows the 25°C and 175°C characteristics
- They are more separated at low V_{GS} values (near $V_{GS(th)}$) but merge together at a higher V_{GS} point ($V_{GS} \approx 3.3V$; $I_D \approx 320A$). **This is the Zero Temperature Coefficient ($I_{\_ZTC}$) point.**
- This is of further interest in Linear Hot Spot failure**.** Nexperia have developed **Trench MOSFETs that operate reliably in 'linear mode'.**
- At **$I < I_{\_ZTC}$** thermal instability due to **positive electro-thermal feedback** can occur.
- The slope at 25C across the Miller Plateau is used to define the Transconductance - **g_m** = delta A / delta V
- This is not usually a problem with (fast) switching, but careful design is needed for quasi steady state '**linear mode**' applications such as clamping.

VGS Threshold Characteristics

- Gate Source threshold voltage is the 'gate drive' voltage needed to **start** to turn the MOSFET **ON**.
- More critically it is the limit above which the MOSFET may conduct some current (and dissipate some power). Vg-s MUST be kept below this level to guarantee that it is held **OFF**.
- The gate drive circuit must accommodate application conditions (noise, high temperature etc.) that could cause the MOSFET to start to turn ON when it should be held OFF.
- **$V_{GS(th)}$** must be above 2.25V at -40C to begin to turn the device on.
- **$V_{GS(th)}$** decreases with Temperature. The BUK**9**61R6-40E is a '**Logic Level**' MOSFET. **At 175°C $V_{GS(th)}$** is guaranteed to be at least **0.5V**.
- In applications needing more margin, '**Standard Level**' MOSFETs (BUK7***) may be a better choice. **At 175°C $V_{GS(th)}$** is guaranteed to be at least **1.0V**.



Typical Logic Level

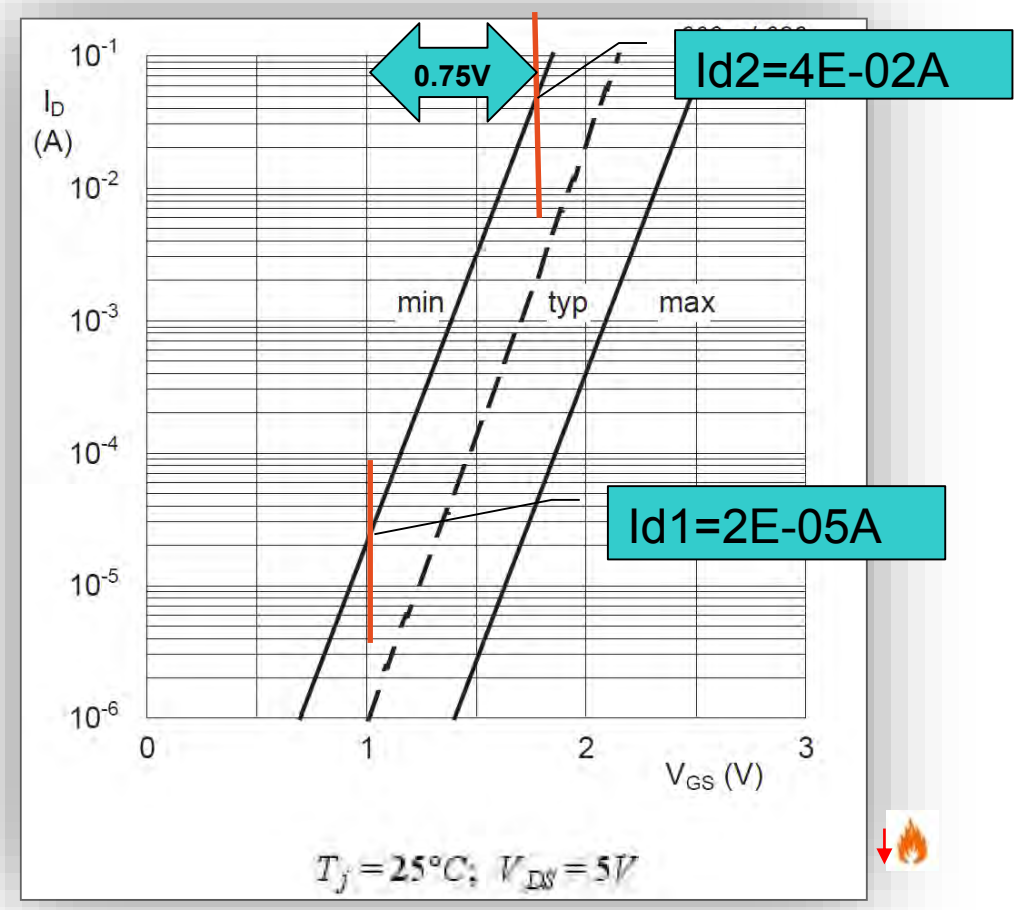
Threshold Ids vs Vgs

Customer Question Example: We have had a concern from the Boost converter chip supplier.

We need to ensure that the FET can achieve an ID of 2A with a VGS of 3V over temp from -40°C to 105°C.

Can the BUK98150-55A and BUK9880-55A achieve this requirement. The graphs below don't show the -40°C curves for Id Vs VGS.
I know VGS goes up with lower Temp's.

Can we get a updated graph with worst case curves for VGS Vs ID over temp from -40°C to 150°C (Tj) as below.



- This graph shows how drain current (I_D) increases exponentially with increasing V_{GS}. (y-axis log, x-axis linear as compared to Transfer Characteristic graph)
- Note that the difference between the minimum and maximum V_{GS} voltage for a given drain current is constant and independent of I_D.
- It can be used with the previous graph to match the MOSFET and its load to its gate driver

Vgsth max @ -40C = 2.25V (see last slide)
ΔV between 2.25V and 3V = 0.75V
ΔI_D for $\Delta V_{(0.75V)}$ or, $k_{I(0.75V)} = I_{D2}/I_{D1} = 2000$ (from graph above)
I_D at 3V => $I_{D(@Vgs=2.25V)}$*2000
$I_{dmin(@Vgs\ =3V)}$ = 1mA*2000 = 2A ✓

Drain Source On-State Resistance Rds ON

- **$R_{DS(on)}$** (Drain-Source on-state resistance) is often the **most important MOSFET parameter**.

  It determines how good a closed-switch the 'ON' MOSFET is. It is usually the key factor **determining the power loss and efficiency** of the circuit.

- ALL graphs where the title is followed by ***'typical values'*** **should not** be used for design data. They will **not** be worst case.

- They are usually shown with junction temperature = 25°C. This will rarely be the case with automotive applications.

- They are an **indication** of how the MOSFET characteristics are related.

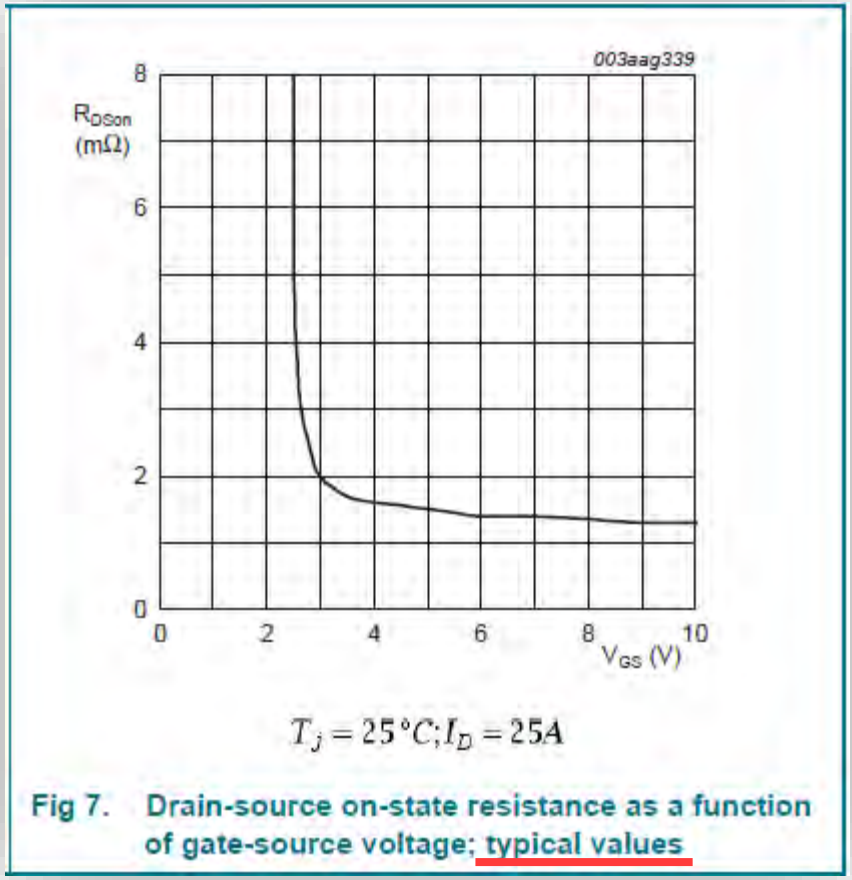


Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

Drain Source On-State Resistance Rds ON over Temperature

- This graph is 'normalised' – which means that the Tj = 25°C $R_{DS(on)}$ is equated to '1'.
- Its value at other temperatures within its operating range is scaled by the factor 'a'.
- This graph is valid for the specific technology (T6 40V Logic Level in this case) and **can** be used for design parameter estimation.

- e.g. at 105°C the $R_{DS(on)}$ for this technology will be 1.5 X the 25°C $R_{DS(on)}$ value.
- For the BUK**9**61R6-40E the maximum 25°C $R_{DS(on)}$ value is **1.6mΩ** (with **V_{gs} = 5V**).
- Max. **105°C $R_{DS(on)}$** value is therefore **2.4mΩ**.

Overdriving

- Driving it with **V_{gs} = 10V**, 25°C $R_{DS(on)}$ = **1.4mΩ**
- With **V_{gs} = 10V**, T_j = **105°C $R_{DS(on)}$ = 2.1mΩ**

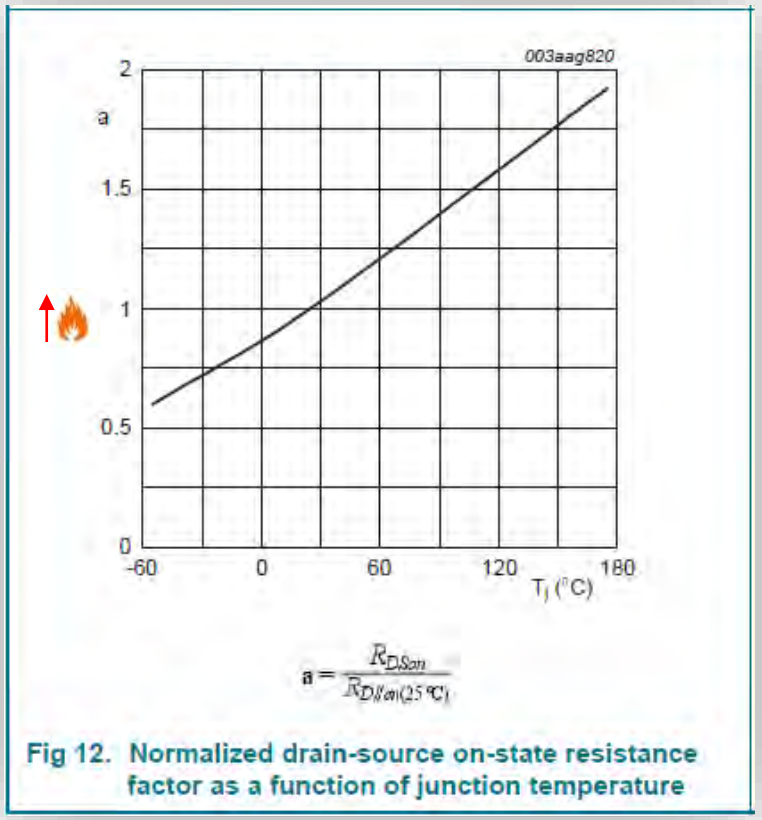
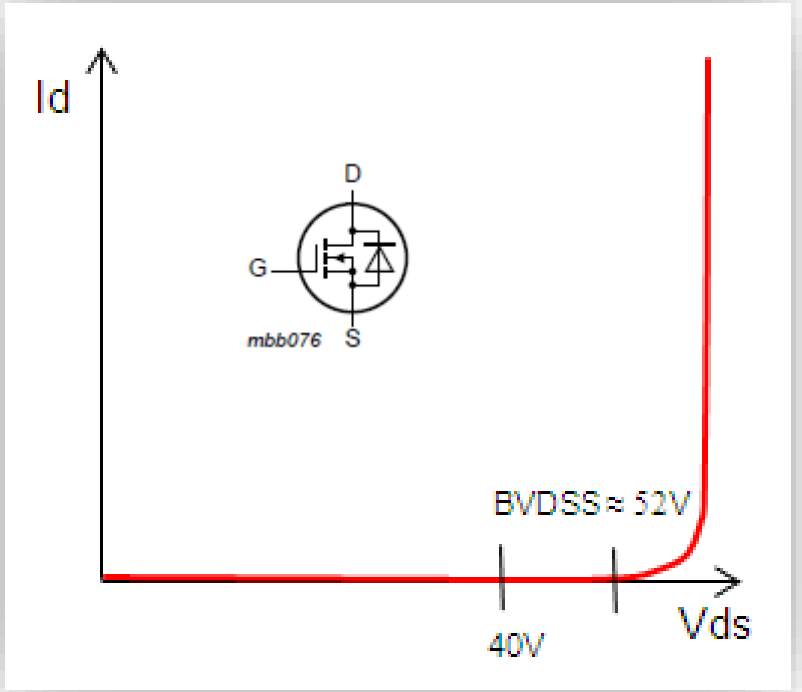


Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

Ids - Drain Source Leakage Current

- This current flows through the (reverse biased) body diode. **This diode is an integral part of the MOSFET** structure. **It cannot be omitted**.
- The leakage current is highly temperature dependent; it approximately **doubles for every 10°C rise in T_j**.
- As with any junction diode it **starts to conduct reverse current** when Vds reaches a critical value (**BVDSS**).
- BVDSS (or $V_{(BR)DSS}$) is nominally 1.3 times the rated V_{DS} (52V for a 40V MOSFET) at 25°C . Reverse current increases disproportionately above this voltage.
- The breakdown voltage ($V_{(BR)DSS}$) has a positive temperature coefficient, i.e. as temperature increases, BVDSS increases.
- At low temperatures $V_{(BR)DSS}$ may be **less than** V_{DS_max} .



Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	40	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	36	-	-	V

I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 °C	-	0.13	1	µA
		V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 °C	-	-	500	µA

NOTE: Nexperia give Idss conditions
At max. V_{ds}= 40V; max. Tj= 175°C

Idss – Example – Competitor

As mentioned previously, be aware of the conditions that the MOSFET parameters are specified at.

This is a 40V MOSFET but the maximum Idss condition is given at V_{ds}= 18V; Tj = 85°C.

These conditions are well below the maximum allowed ratings (40V; 175°C).

IDSS roughly doubles for every 10°C rise in temperature.

Although this 'headline' 20µA figure looks better than the 500µA Nexperia figure, it is in fact **WORSE**

Infineon

IPD100N04S4-02

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics[2]						
Thermal resistance, junction - case	R_{thJC}	-	-	-	1.0	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}	-	-	-	62	
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm² cooling area[3]	-	-	40	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D= 1mA	40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=95µA	2.0	3.0	4.0	
Zero gate voltage drain current	I_{DSS}	V_{DS}=40V, V_{GS}=0V, T_j=25°C	-	0.04	1	µA
		V_{DS}=18V, V_{GS}=0V, T_j=85°C[2]	-	1	20	

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Dynamic Characterists

Dynamic Characteristics

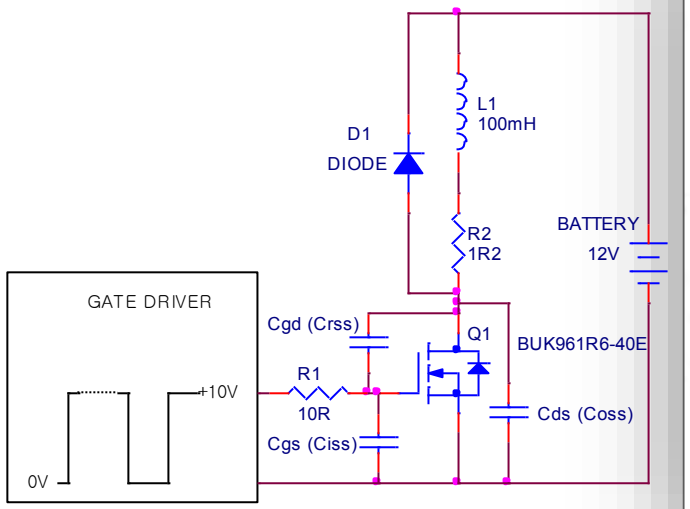
- **Dynamic characteristics** are parameters that affect **switching performance**.
- The MOSFET **gate is electrically insulated** from the channel structure by the **gate oxide**.
- However, it is capacitively coupled to the channel structure.
- The **electric field created by V_{GS} controls** the conductivity of the channel – hence **$R_{DS(on)}$**.

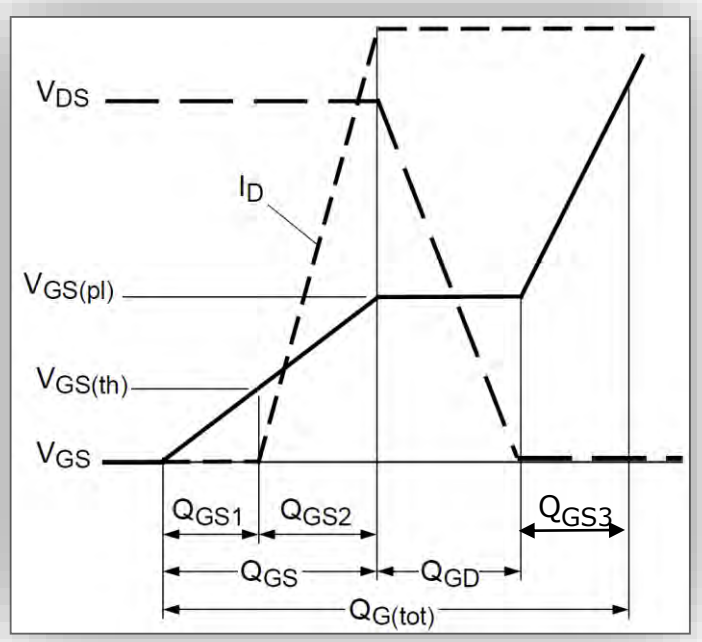
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 5 V; see Figure 13; see Figure 14	-	120	-	nC
Q_{GS}	gate-source charge		-	26.9	-	nC
Q_{GD}	gate-drain charge		-	40.9	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C; see Figure 15	-	12300	16400	pF
C_{oss}	output capacitance		-	1530	1840	pF
C_{rss}	reverse transfer capacitance		-	740	1020	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 5 V; $R_{G(ext)}$ = 5 Ω	-	95	-	ns
t_r	rise time		-	118	-	ns
$t_{d(off)}$	turn-off delay time		-	195	-	ns
t_f	fall time		-	119	-	ns
L_D	internal drain inductance	from upper edge of drain mounting base to center of die	-	2.5	-	nH
L_S	internal source inductance	from source lead to source bonding pad	-	7.5	-	nH
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 16	-	0.77	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 25 V	-	57	-	ns
Q_r	recovered charge		-	97	-	nC

The Switching Process

- This illustration shows the processes that are active during the switch ON of a MOSFET driving an inductive load.

- **Gate drive voltage rises from 0V to +10V** (Quckly !!).
- **Cgs // Cgd start to charge** up via R1. I_in is initially 1A.
- **V_{GS} rises to $V_{GS(th)}$.** The MOSFET channel starts to conduct.
- Channel current increases steadily until **channel current equals inductor current**. Current no longer flows in DIODE D1 and D1 becomes reverse biased. **V_{ds} starts to fall**.





- Input current now diverts into C_{gd} as V_{ds} decreases. Current flow into C_{gs} reduces and the '**Miller plateau**' phase starts.
- This continues until V_{ds} drops to I_D * $R_{DS(on)}$ (≈ 0V). C_{ds} (C_{oss}) has now fully discharged through the MOSFET. **Input current continues to flow into C_{gs} and C_{gd}** even though the **MOSFET is now fully enhanced (ON).**
- **To turn the MOSFET OFF, gate drive voltage is set to 0V**.
- Charge starts to flow out through R1 and the reverse sequence of events takes place. When **V_{GS} drops below $V_{GS(th)}$, channel current will stop flowing**.

MOSFET Capacitance and Charges

- The MOSFET capacitances are associated with structures within the MOSFET die. They are complex.
- **C_{ISS}** is associated primarily with the **gate oxide** layer. Its thickness is fixed; **C_{ISS} is not voltage dependent** (Stable over Vds)
- **C_{RSS} & C_{OSS}** are associated with the reverse biased (body diode) junction, they depend on '**depletion layer' thickness** (which **depends on V_{DS}**). **High V_{DS}** = thick depletion layer = **low capacitance**. **Low V_{DS}** = thin depletion layer = **high capacitance**.
- Due to the voltage dependence of the capacitances, it is often **easier to use gate charge** transferred to / from the capacitances as **design parameters**.
- To make valid comparisons between MOSFETs, the measurement conditions for the parameters must also be comparable

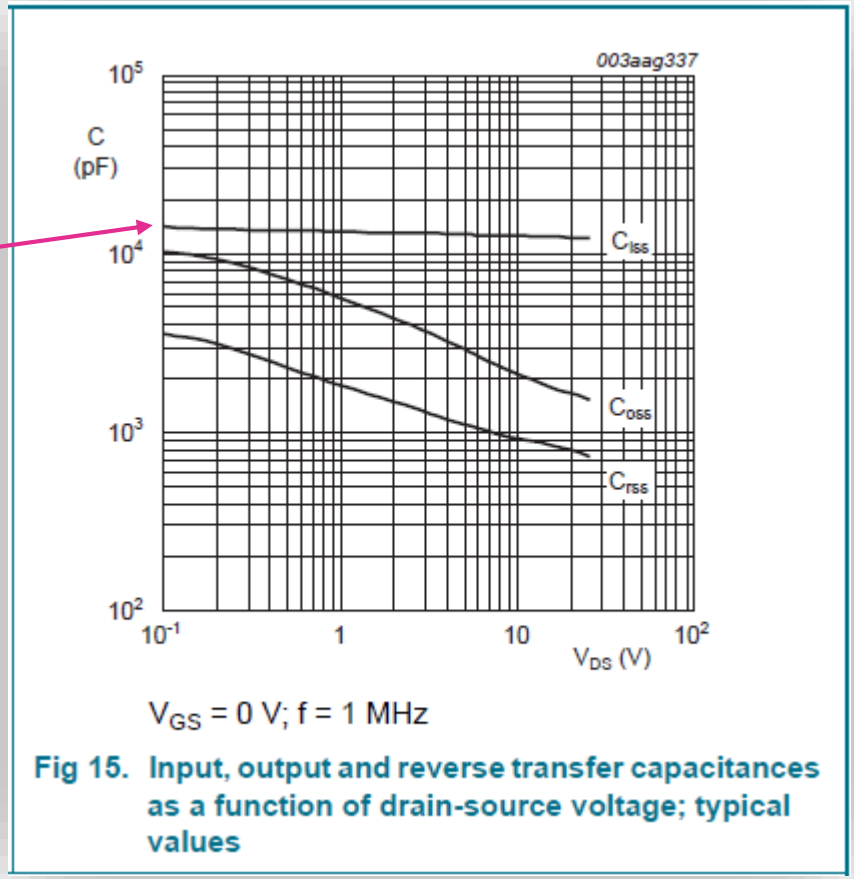
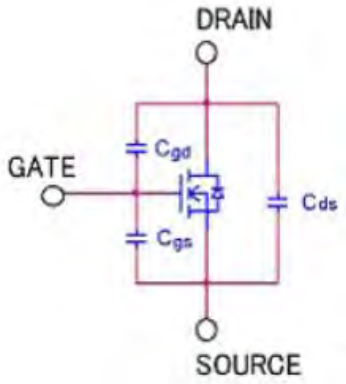


Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

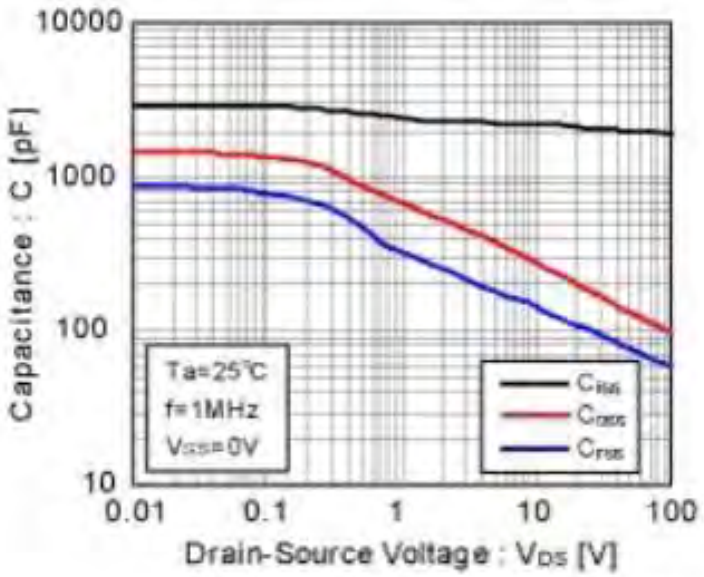
Dynamic Capacitance



$C_{iss} = C_{GS} + C_{GD}$, C_{DS} shorted

$C_{rss} = C_{GD}$

$C_{oss} = C_{DS} + C_{GD}$



Capacitance-V_{DS} dependence

Ciss, Coss, Crss relate to the parasitic capacitances referred to as the as dynamic characteristics.

Ciss is the input capacitance, and is the capacitance obtained by totaling the gate-source capacitance Cgs and the gate-drain capacitance Cgd; it is the capacitance of the MOSFET as a whole, as seen from the input. This capacitance must be driven (charged) in order to cause the MOSFET to operate, and so is a parameter of importance when studying the drivability of an input device or input losses. Qg is the amount of charge necessary to drive (charge) Ciss.

Coss is the output capacitance, obtained by adding the drain-source capacitance Cds and the gate-drain capacitance Cgs, and is the total capacitance on the output side. If Coss is large, a current arising due to Coss flows at the output even when the gate is turned off, and time is required for the output to turn off completely.

Crss is the gate-drain capacitance Cgd itself, and is called the feedback capacitance or the reverse transfer capacitance. If Crss is large, the rise in drain current is delayed even after the gate is turned on, and the fall in current is delayed after the gate is turned off. In other words, this parameter greatly affects switching speed. Qgd is the charge amount necessary to drive (charge) Crss.

Gate Charge Definitions

Electrical characteristics of MOSFETs (Charge Characteristic $Q_g/Q_{gs1}/Q_{gd}/Q_{SW}/Q_{OSS}$)

- **Gate charge**

  Because the Gate (G) input terminal of a MOSFET is insulated, the amounts of charge Q seen from the Gate are important characteristics. Figure 1.5 illustrates the definitions of gate charge characteristics.

- **Total gate charge Q_g**

  The amount of charge to apply voltage (from zero to designated voltage) to gate

- **Gate-source charge 1 Q_{gs1}**

  The amount of charge required for a MOSFET to begin to turn on (before dropping drain-source voltage)

- **Gate-drain charge Q_{gd}**

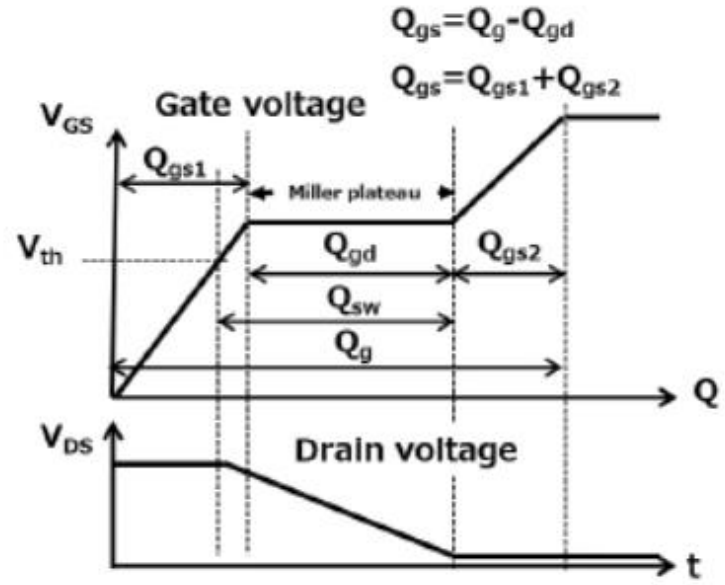
  The amount of gate charge charged in the Miller plateau

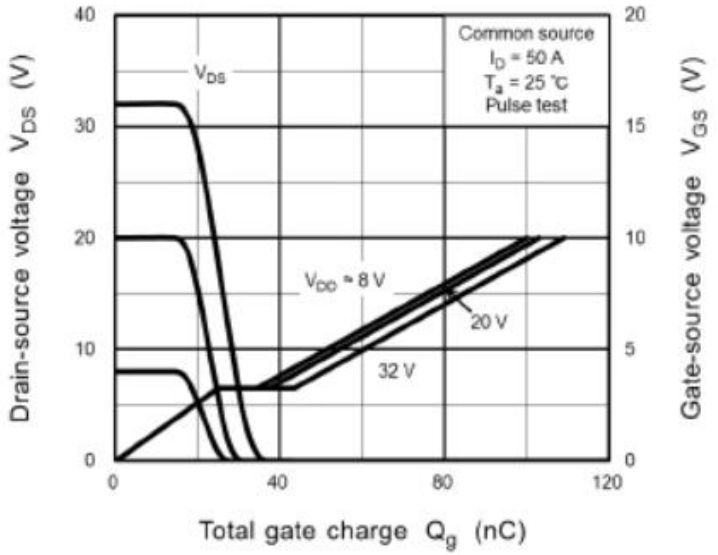
- **Gate switch charge Q_{sw}**

  The amount of charge stored in the gate capacitance from when the gate-source voltage has reached V_{th} Until the end of the Miller plateau

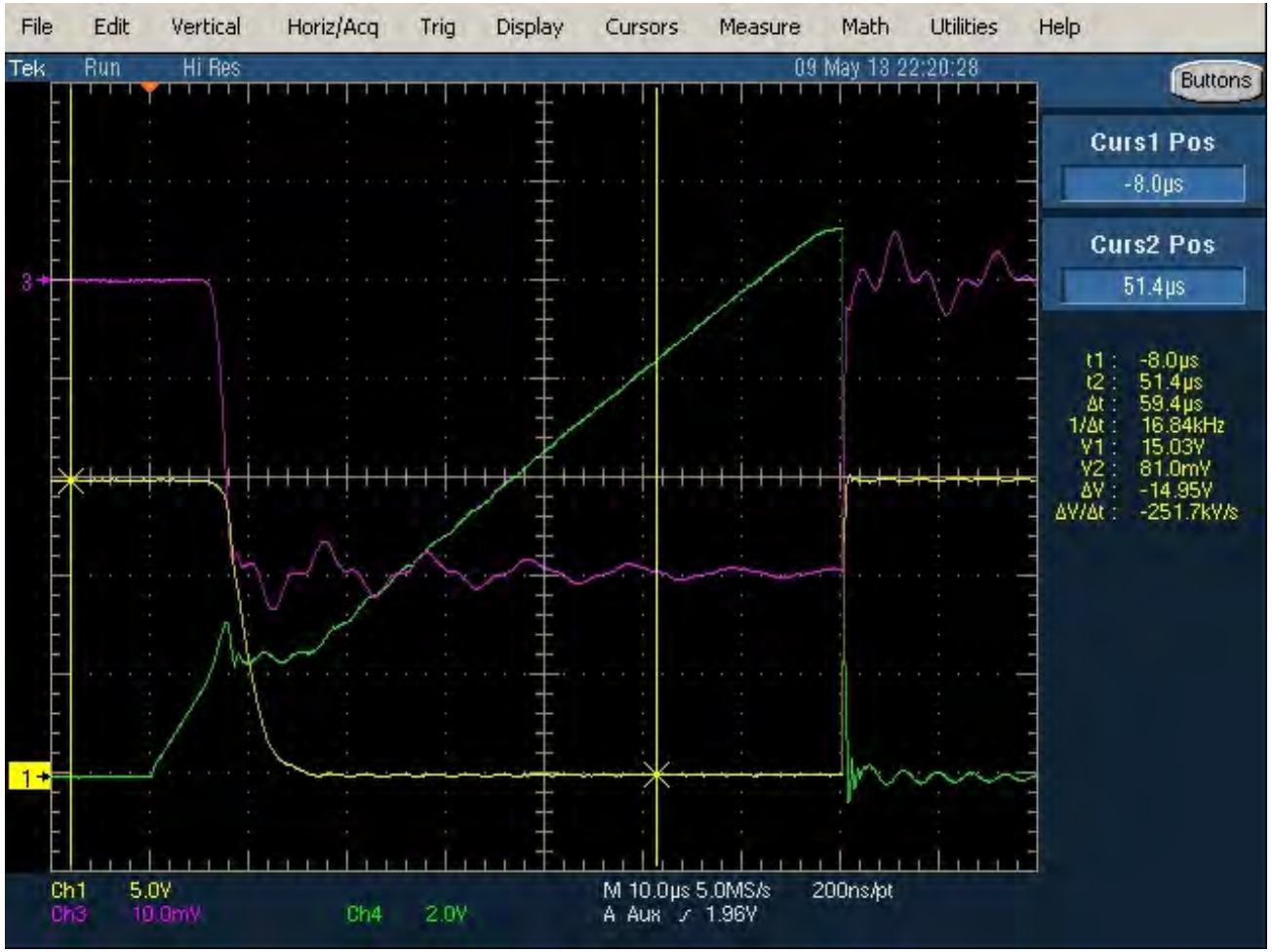
- **Output charge Q_{oss}**

  Drain-source charge

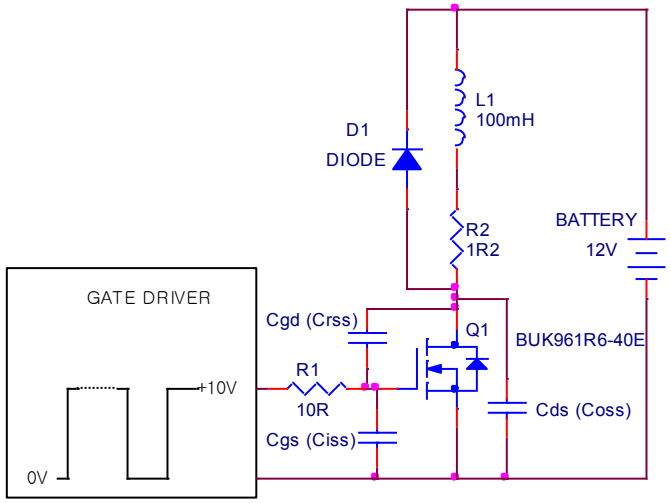




Oscilloscope Traces of MOSFET switching On / Off



- Green trace V_{GS}
- Yellow trace V_{DS}
- Purple trace I_D (10mV = 1A)
- Gate drive source current << gate drive sink current.
- Turn OFF time << turn ON time (different gate drive currents)
- Note the VGS 'ring' due to high dV/dt



Delay, Rise and Fall Times

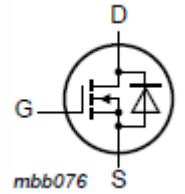
- There is always some resistance associated with the gate structure of the MOSFET. Also it is advisable to **include a low value external resistance in series with the gate** (to damp out any oscillatory transients).
- Initial MOSFET response to gate drive depends on the nature of the load. A resistively loaded MOSFET should be used for these measurements.
- Turn Off depends on Vgs. i.e. it's quicker to turn off from Vgs =5V than Vgs = 10V due to RG
- There is always some unavoidable 'stray' **inductance** associated with the conductors (lead frame, wire bonds etc.) of a packaged MOSFET. These inductances will affect the switching behaviour while the channel current is changing.

$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 5 V; $R_{G(ext)}$ = 5 Ω	-	95	-	ns
t_r	rise time		-	118	-	ns
$t_{d(off)}$	turn-off delay time		-	195	-	ns
t_f	fall time		-	119	-	ns
L_D	internal drain inductance	from upper edge of drain mounting base to center of die	-	2.5	-	nH
L_S	internal source inductance	from source lead to source bonding pad	-	7.5	-	nH

MOSFET Body Diode Characteristics

- The 'Body Diode' in the MOSFET structure behaves similarly to all silicon junction diodes. In normal MOSFET operation this diode is reverse biased and **plays no part** in the function.
- When the MOSFET is OFF (V_{GS}=0), it will still operate as a diode; D = cathode, S = anode. **It will carry current if it is forward biased ($V_{SD} \geq$ 0.5V @ 25°C)**
- If the channel is fully enhanced (switched ON) at this stage, **current flows through the channel rather than through the diode (if $I_D * R_{DS(on)} < 0.5V$)** . Power loss reduces.
- This '**third quadrant**' operation when the MOSFET is turned ON is called '**synchronous rectifier**' mode.
- As with all p-n junction diodes, current does not cease immediately when the bias voltage is reversed. There is a short '**reverse recovery**' time while charge carriers are withdrawn from the junction. The charge that is withdrawn from the p-n junction in this process is the '**recovered charge**'.
- These non ideal diode characteristics contribute towards power losses. The reverse recovery event can be a troublesome EM noise source, hence an EMC concern.

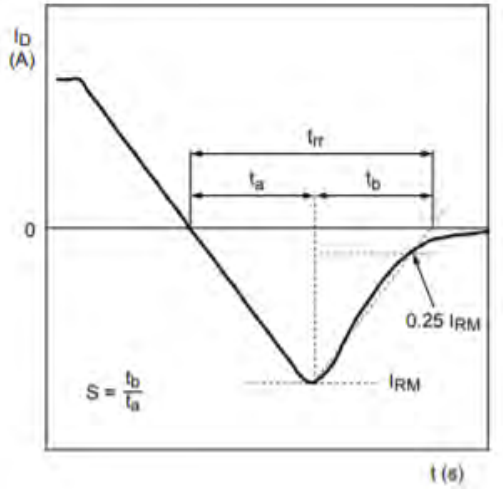
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 15		-	0.8	1.2	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; T_j = 25 °C; Fig. 16		-	32.3	-	ns
Q_r	recovered charge			-	26.8	-	nC
S	softness factor			-	0.85	-	
		I_S = 25 A; dI_S/dt = -500 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; T_j = 25 °C; Fig. 16		-	0.7	-	

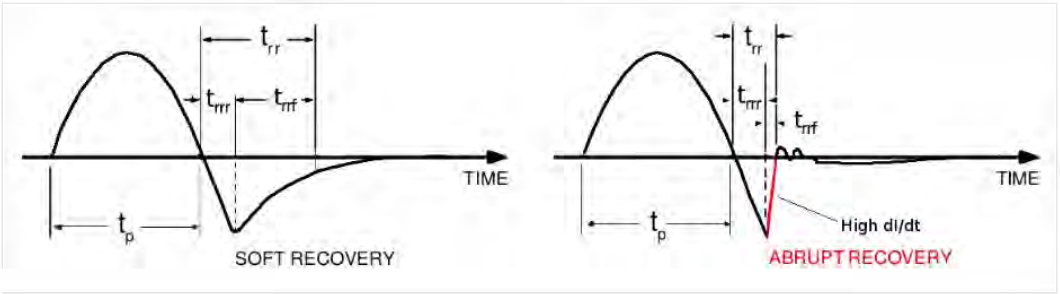


Diode Recovery terminology and MOSFETs

- **Speed => trr and Charge => Qrr**
  - SiC Rectifiers have minimal Qrr (HV Schottky)
  - Schottky has low Qrr
  - PN Rectifiers have higher Qrr
- **trr classes**
  - Schottky <10nS (including SiC HV devices)
  - Standard PN ~1000nS
  - Fast ~200nS , Ultrafast 50 to 150nS, Hyperfast <25nS
  - Soft Recovery usually 45 to 120nS
- **Softness Factor**
  - Stated at a dI/dt value (ex. 200A / uS)
  - RRSF = Tb / Ta

- **MOSFET PN Junction - Recovery**
  - trr and Qrr are listed in Data Sheets. (previous slide)
  - RRSF, Softness is not normally listed for MOSFETs for the body diode (PN). For Trench 9 devices this is in the data sheet.
  - This can be measured using the same Double Pulse test used for Rectifiers. Example on next slide.



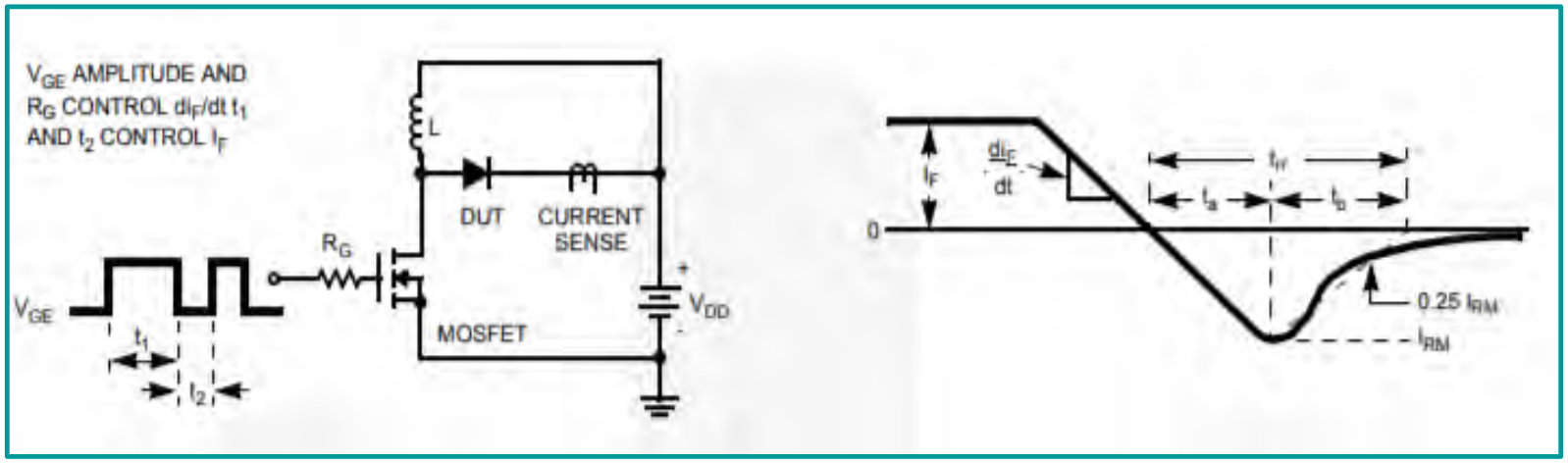


Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 15		-	0.8	1.2	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; T_j = 25 °C; Fig. 16		-	32.3	-	ns
Q_r	recovered charge			-	26.8	-	nC
S	softness factor			-	0.85	-	
		I_S = 25 A; dI_S/dt = -500 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; T_j = 25 °C; Fig. 16		-	0.7	-	

How trr and Softness are measured

Double Pulse Method

- Test Circuit for MOSFET Body Diode as DUT is the same test method as used for Rectifiers. Test method is similar to ½ Bridge applications.
- DUT is MOSFET with Gate shorted to source.
  - First Pulse establishes the current If in t1
  - Off Pulse t2, establishes current in Diode as If
  - Second Pulse used to measure the waveform.



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Extended Topics

Power Dissipation Thermal Design

- Power Handling
  - Average Power Total Loss Model
  - Loss Calculation Methods
    - Conduction
    - Switching
    - Avalanche
  - Static Device Temperature
  - Dynamic Die Temp

Total Power Loss Model

Why:

1) A large percentage of customer design questions are thermal.
2) Aside from ESD, MOSFET operational failure is primarily from thermal overstress.

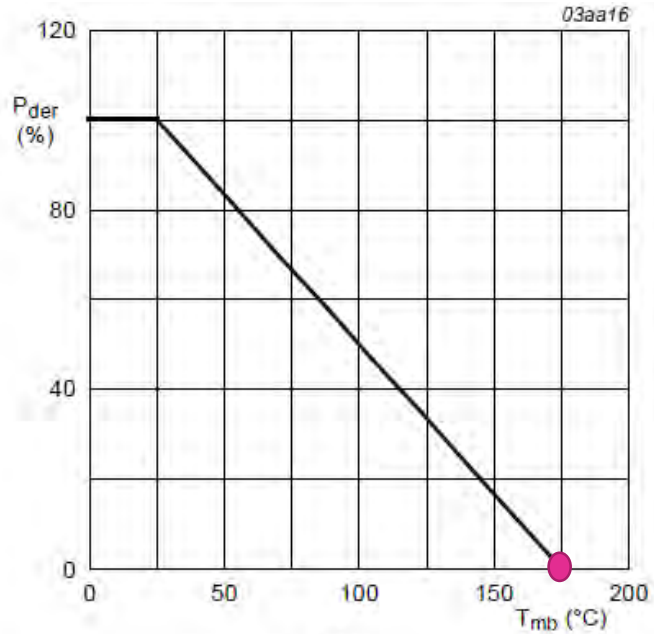
Primary Components

$$P_{total} = P_{conduction} + P_{switching} + P_{avalanche}$$

- $P_{conduction} \sim f$ (I, R_{ds}@Vgs, DutyCycle) in ON State
  - Fairly easy to estimate at max constant current ($I_{dc}^2 * R_{ds}$)
  - Also, Reverse conduction in OFF state across body diode ($I_r * V_d$)
- $P_{switching} \sim f$ (deltaI, deltaV, $F_{switching}$, Zload)
  - Also could include Gate Drive losses if $F_{switching}$ is high. With large power MOSFETs, most the gate drive losses are in the driver circuitry (i.e. low R_{gate})

    $P_{gatesw} \sim f$ (Q_{gtot} @Vgs, $F_{switching}$, R_{gate})
- $P_{avalanche}$ - f (V_{bat}, I_{avl}, V_{avl}, F_{avl}, Z_{avl})
  - BVdss exceeded from switching off Inductive load. E_{as} is specified as one time event.

Normalized Derating



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Example Application

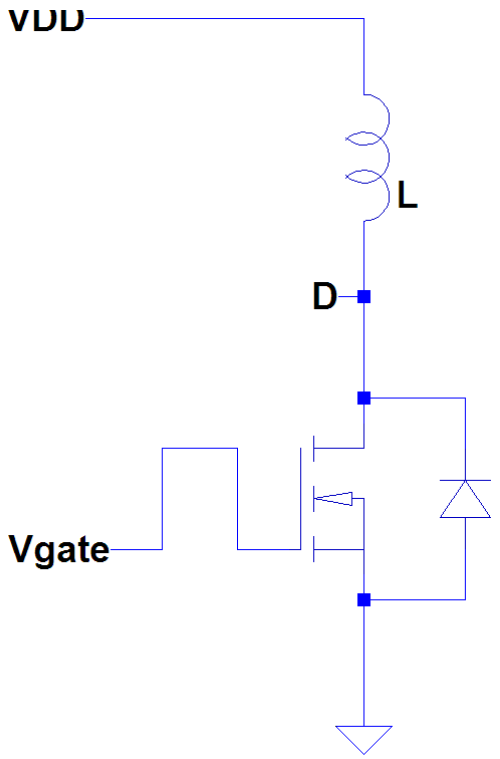
Inductive Load – 14V Fuel Injector

Customer Application Parameters Example:

Conduction
Rload = 22 Ohms
Vdd = 16V
DTY = 12% (max at Fmax)

Switching
Trise = 50uS
Tfall = 50uS
Fmax = 60Hz (7200 rpm, 4 cycle)
delta**I** = 16V/22Ohms
delta**V** = **V**dd – Gnd = 16V

Avalanche
Lload = 12mH
*Cload = 0.3uF
Rmb-ambient = 10 K/W



Conduction Losses - Estimating

Pconduction ~ *f* (Id, Rds@Vgs, Rload, Vbat, DutyCycle) in ON State

- Fairly easy to estimate at max constant current ($Id^2 * Rds * DutyCycle$)
- Steps:
  1. Use max Id (**R**load and **V**bat)
  2. Use ON Duty Cycle
  3. Use max Steady State Tj design target in Application (1st pass) to estimate max **R**dson. Example: 25mOhm * 1.5 (at 120C) = 33mOhm

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 8 A; T_j = 25 °C		-	18	25	mΩ

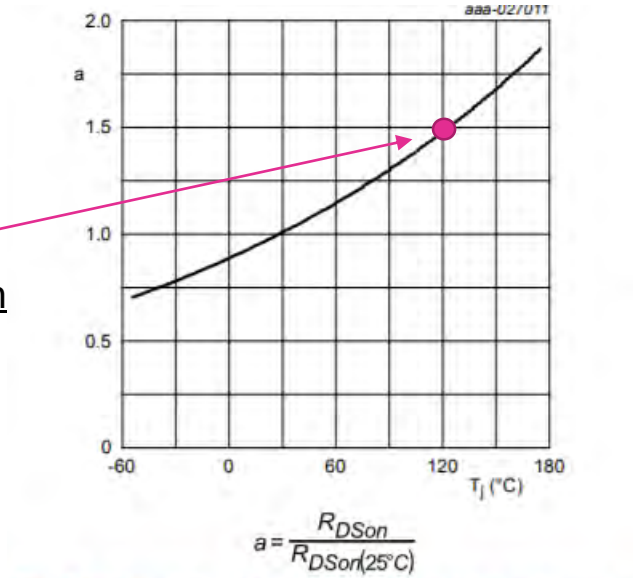


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

Prconduction ~ *f* (Ir, Vd, Tr, Fswitching) in OFF State

- Reverse conduction in OFF state across body diode during periodic switching.
- Specifications and Spice models of Body Diodes are simplistic.

Switching Losses - Estimating

Methods used to Estimate Switching Losses

Validation →

Pswitching ~ *f* (deltaI, deltaV, Fswitching, Tsw, Zload)

Mostly Resistive: Id proportional to Vload

***P**switching >= 1/6 * Fswitching * Vds * Id * Ts

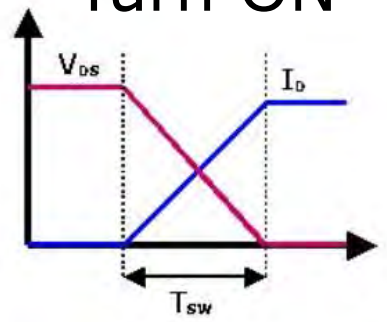
Increasing | Power Dissipation

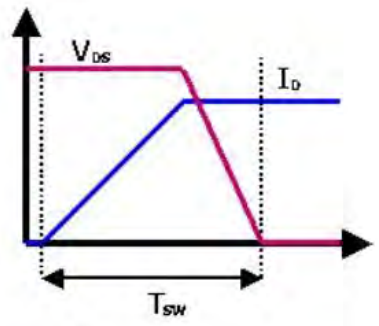
Complex: Vds decline lags Id

***P**switching <= 1/2 * Fswitching * Vds * Id * Tsw

* Turn on only. Turn off needs to be included if not an avalanche application. For Resistive loads if Ton = Toff, then Pon = Poff.

Turn ON





Spice Simulation

Electrical Model of Load

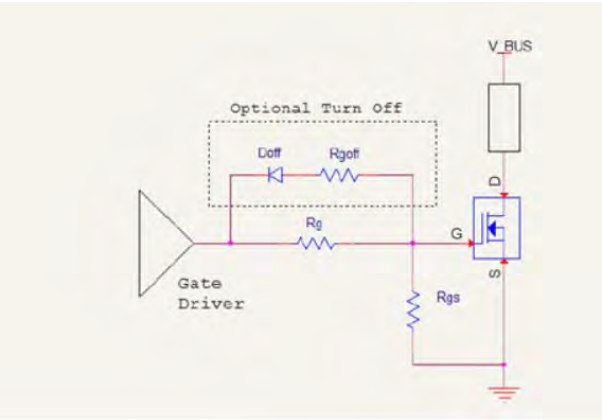
- Loads are not ideal. inductance changes with current, or Solenoid

Spice Model with Accurate Switching

Gate Drive Model is critical.

Compare Simulation to circuit performance.

Gate Drive Losses can be evaluated in model. Usually, small enough to neglect.

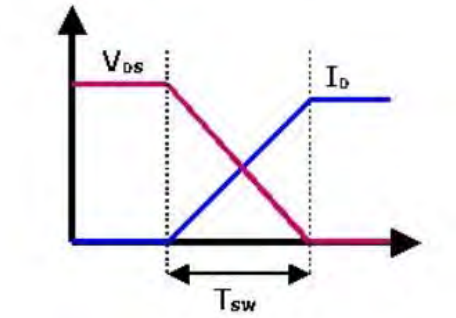


* Figures from Peter Markowski, ePOWER LLC (2012) and John Hargenrader, Fairchild Semiconductor (2013)

Resistive Load Example

For the linear waveforms shown, where T is the total switching time:

Resistive Load waveforms



Vds = **V**p (1-t/T)
Ids = **I**p (t/T)

So, the instantaneous power is

Pswon = **V**p * **I**p * t/T * (1-t/T)

Integrating the Energy over T (switching time) gives the ON switching Energy as:

Eswon = $\int_0^T$ **P** dt

= $\int_0^T$ **V**p* **I**p * t/T * (1-t/T) dt

= **V**p* **I**p * [$\int_0^T$ t/T dt - $\int_0^T$ $(t/T)^2$ dt]

= **V**p* **I**p * [[$1/2T * t^2$] – [$1/3T^2 * t^3$]]$_0^{Tsw}$

= **V**p* **I**p * [1/2Tsw – 1/3Tsw]

= 1/6 * **V**p* **I**p * Tsw

Avalanche Losses

Eas specifications in data sheets is for a one time event at specific I and L value. Can be used for device comparison, but limited value for design.

1. Avalanche (**E**as) calculations can be used for **P**avalanche**,** to be used in Static Thermal analysis.
2. Avalanche data sheet curves can be used for singular and repetitive event robustness. (Discussed later)

Eas - Avalanche energy can be higher than the energy stored in the inductor. (What??)
Vavl – Is higher than BVdss. A Swag factor is included in these calculations, normally 1.2 to 1.3. This can be verified in the application with the exact device.
RL - When the series R of the Inductor is small, these losses can be ignored. **T**av –Time in Avalance depends on rate of energy dissipated across MOSFET.

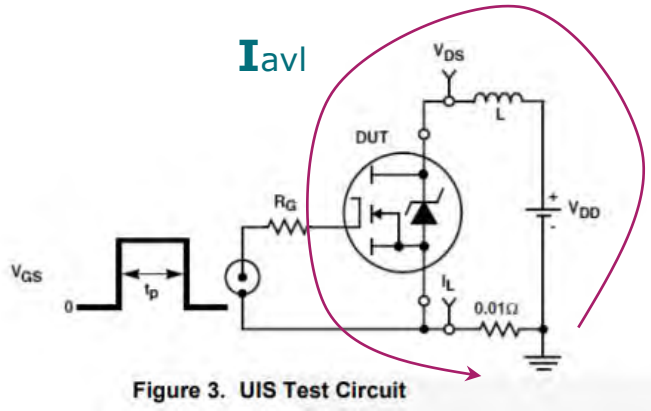


Figure 3. UIS Test Circuit

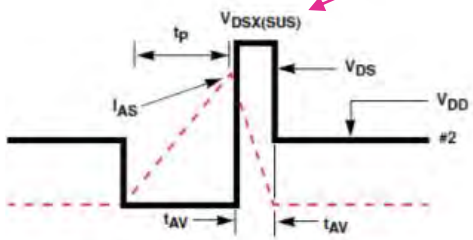


Figure 4. UIS Waveforms

$$E_{as} = [\ \tfrac{1}{2}\ L \times I_{as}^2\ ] \times [\ V_{avl} / (V_{avl} - V_{dd})\ ]$$

where, $V_{avl} = BV_{dss} \times 1.3$

Now, $P_{avalance} = E_{as} * F_{avl}$

(* Figure from AN-7514 Fairchild 2002)

Static Thermal Model – Final Output - T_{mb}

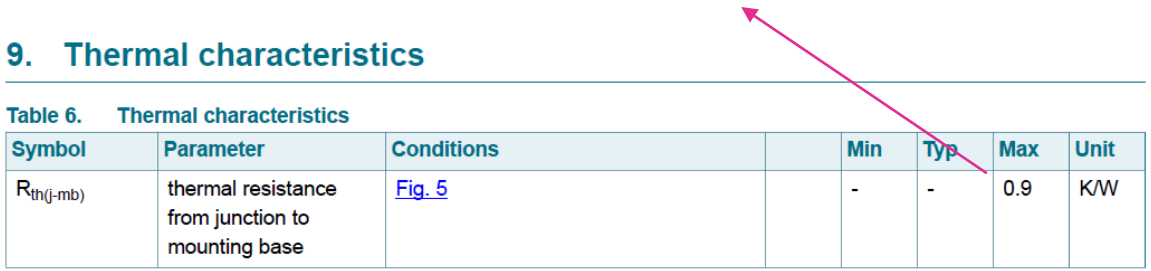
1. Use the **P**total Power Dissipation to estimate the Device Mounting Base Max Operating Temperature, **T**mb(max)
   - 3D thermal model (i.e. - *FloTherm*)
   - Physical Calculations of **R**mb-ambient (old school, sometimes including blackbody radiation portion)
   - Use of standard **R**mb-ambient ratings for device on specified pad area *(*No longer specified on many device data sheets),* or from Test Card in the literature.
   - Lab Measurement with known power dissipation, and thermocouples on prototype hardware.

2. Use **T**mb(max) as input to Dynamic Spice Model with RC Thermal network.

   Output: **T**jmax, delta**T**j, **T**javg

3. Use the data sheet **R**j-mb to Calculate the Max average die temp, **T**javg. This can be used for FIT Rate Calculations, and to cross check the simulations. **

Tjavg = (**P**conduction + **P**switching + **P**avalanche) * (**R**j-mb + **R**mb-Ambient)



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	-	0.9	K/W

Dynamic Die Temp – RC Thermal Model

Methodology

1. Construct Electrical Spice Model

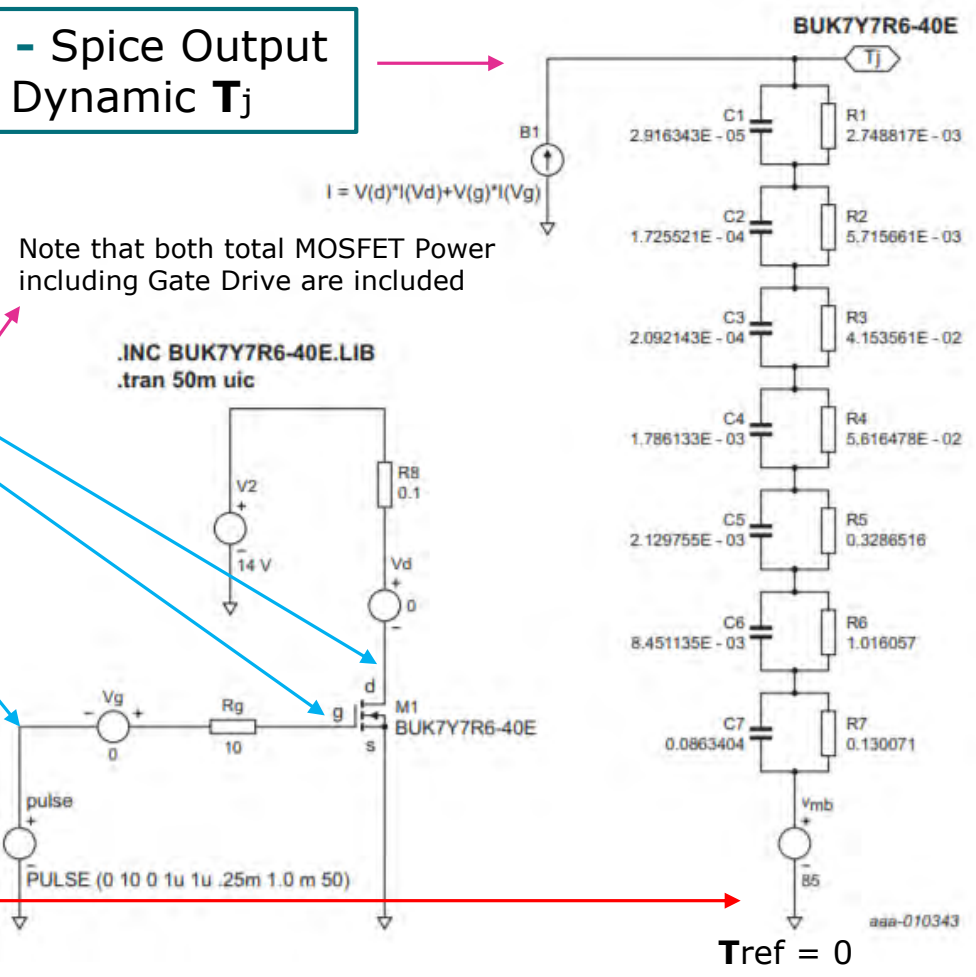
   Compare Model to switching waveforms of actual circuit

   Verify Maximum Conditions, Duty Cycle, Min load R, Max load L, etc.

2. Integrate RC Thermal Model (Foster or Cauer) in Spice.
   - May be integrated into Spice Model already
   - If not, set up Power Input to RC Network.

3. Establish **T**mb reference Voltage. Use **T**mb(max) as input to Dynamic Spice Model. (here **T**mb is set to 85)

NEXT - Spice Output – Plot Dynamic **T**j



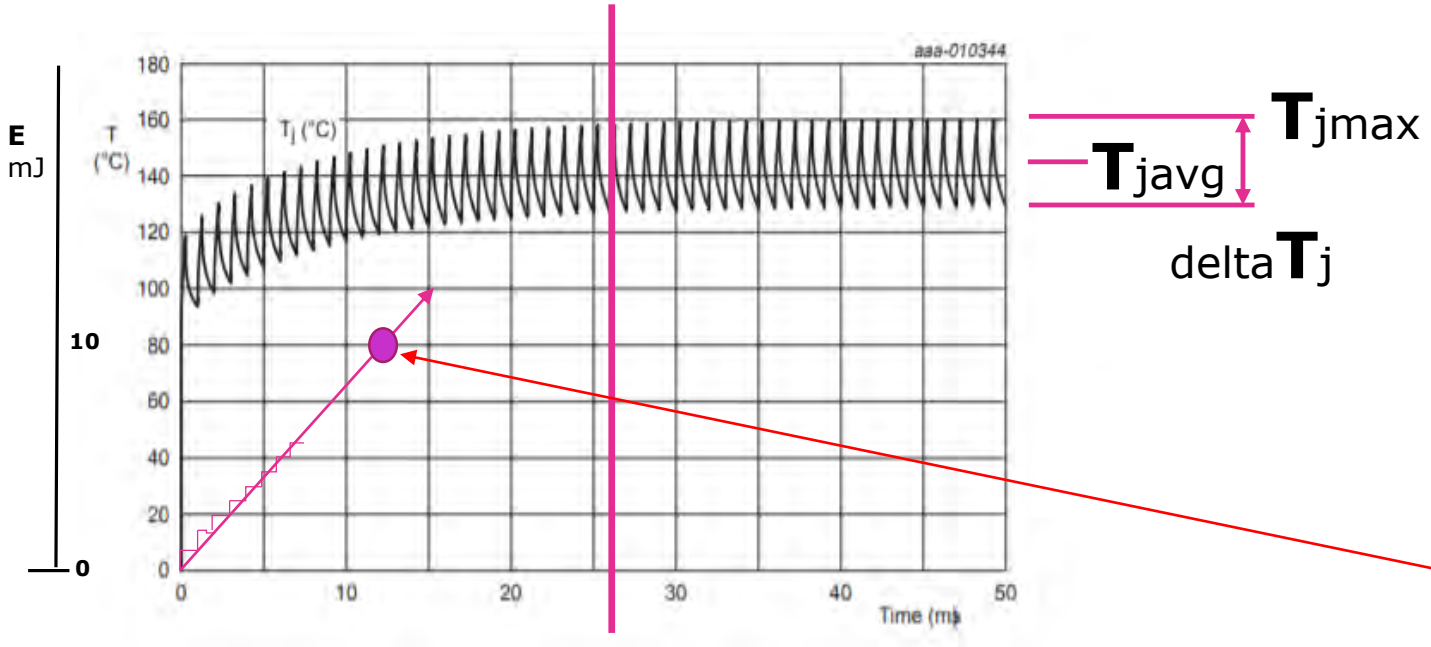
Tref = 0

*figures from Power MOSFET Application Handbook, Nexperia Semiconductor

Dynamic Die Temp – RC Thermal Model

Spice Output – Dynamic Die Temp

Thermal Model Reaches Steady State



Questions Using Spice:

1) Is Rds thermally adjusted for Temp? In models that have embedded Cauer RC models, if they are connected to a reference temp, the Rds may be compensated.
2) Is Rds set to the max, or to nominal in the model at 25C as a starting point.

Basic Thermal Design elements:

1) Is **T**jmax below 175C?
2) Is delta**T**j extreme?

** Crosscheck **T**javg with calculated value from slide 19

Conduction, Switching and Avalanche loss estimates, can all be compared to the Spice Model calculations.

Switching - Using the integrated Energy functions in Spice and looking at the loss over multiple cycles is useful.

Example = (10mJ / 12mS)

~= **0.83W**

May 23, 2019

Understanding Snubbers

Snubbers - ½ Bridge Example AN11160

- **What does a snubber do?**
  - Manages sudden changes in current during switching.
  - In AN11160, the stray inductance in series with the MOSFET is what is being 'snubbed', from PCB traces and package inductance.
- **Basics of Selecting RC components.**
  - **R_S** is selected to maintain instantaneous current during switching event.
  - **C_S** is selected to allow transfer of stored energy from Inductor to damp ringing from **C_{OSS}**, **L_{LK}** interaction.

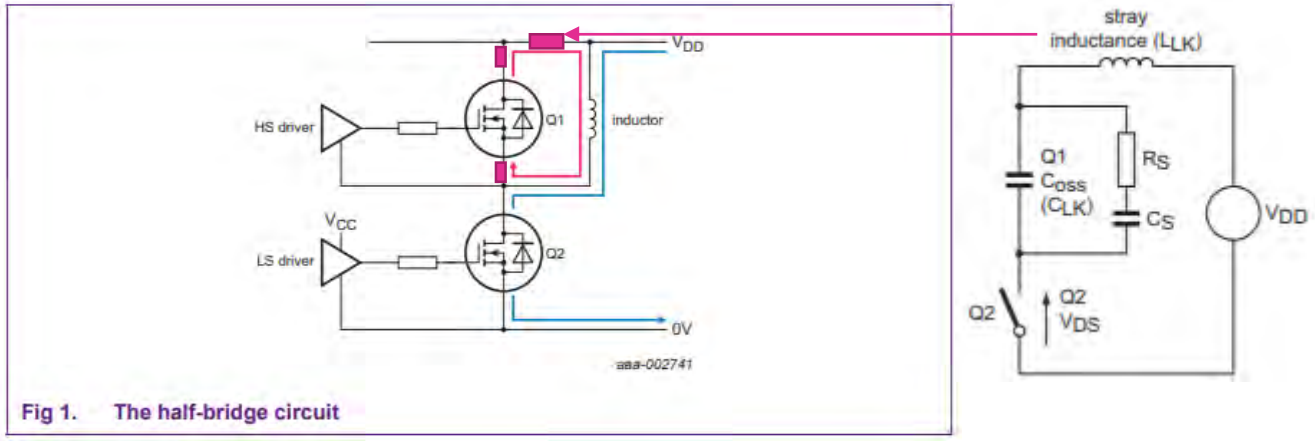


Fig 1. The half-bridge circuit

- **R_S (Snubber Resistor)**
  1. Rule of Thumb – use the load current, and Vdd. **$R_S = V_{dd} / I_{load}$**
  2. Experimental - Use **C_{add}** in parallel with **C_{OSS}**, and measure frequency of **f_{ring}** at two different points in the Lab (Section 3). Calculate **L_{lk}** (Section 5).
     - Use **$C_{lk} = C_{OSS}$**, **L_{lk}**, to find **R_S**

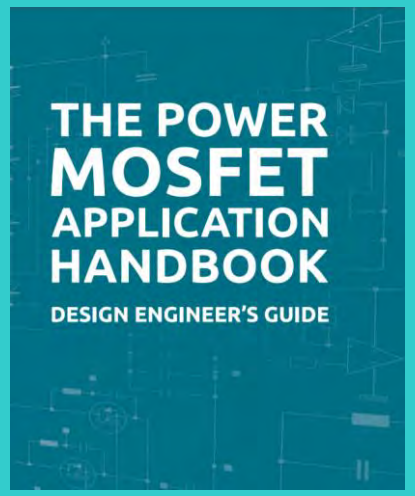
$$R_S = \left(\frac{1}{2\zeta}\right)\sqrt{\frac{L_{LK}}{C_{LK}}}$$

- **C_S (Snubber Cap)**
  1. Rule of Thumb
     - Use **C_S** = ~**C_{OSS}** of the MOSFET
  2. Experimental - Use **R_S** and **f_{ring}** to calculate. (Section 5)

$$C_S = \frac{1}{2\pi R_S f_{RINGO}}$$

May 23, 2019

SOA Derating



Voltage Scale or Current Scale SOA Method

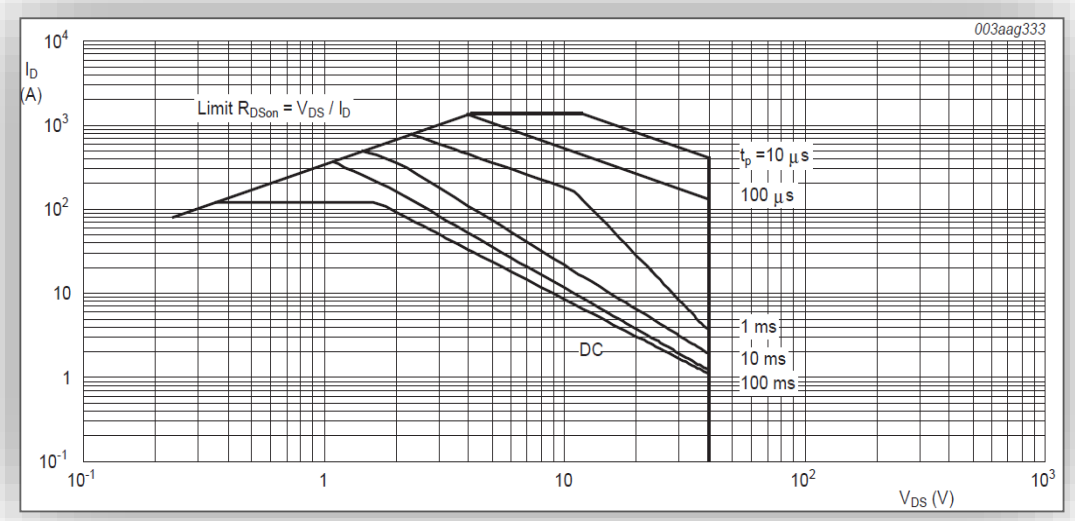
- Calculate the proportion based on Tjmax and Tmb

  Power Scale Factor = [Tjmax – Tmb(application)] / [Tjmax – Tmb(SOA Curve)]

  For a 175C device at 100C this is:

  PSF = [175 – 100] / [175 – 25] = 0.5

1) Scale either the Voltage Axis or Current Axis using this factor.
2) Reposition the BVdss vertical line or Imax line to the new axis scale
3) Reposition the Rds Limit line based on the new x-axis scale
   - Move horizontally for Voltage axis
   - Move Vertically for Current axis
4) Extend the data lines to the endpoints with the same slope



De-rated to 50% power using Voltage Scaling on the x-axis,
This is a 50% derating for 100C (using 175 C max)

Nexperia

BUK7M6R3-40E

N-channel 40 V, 6.3 mΩ standard level MOSFET in LFPAK33

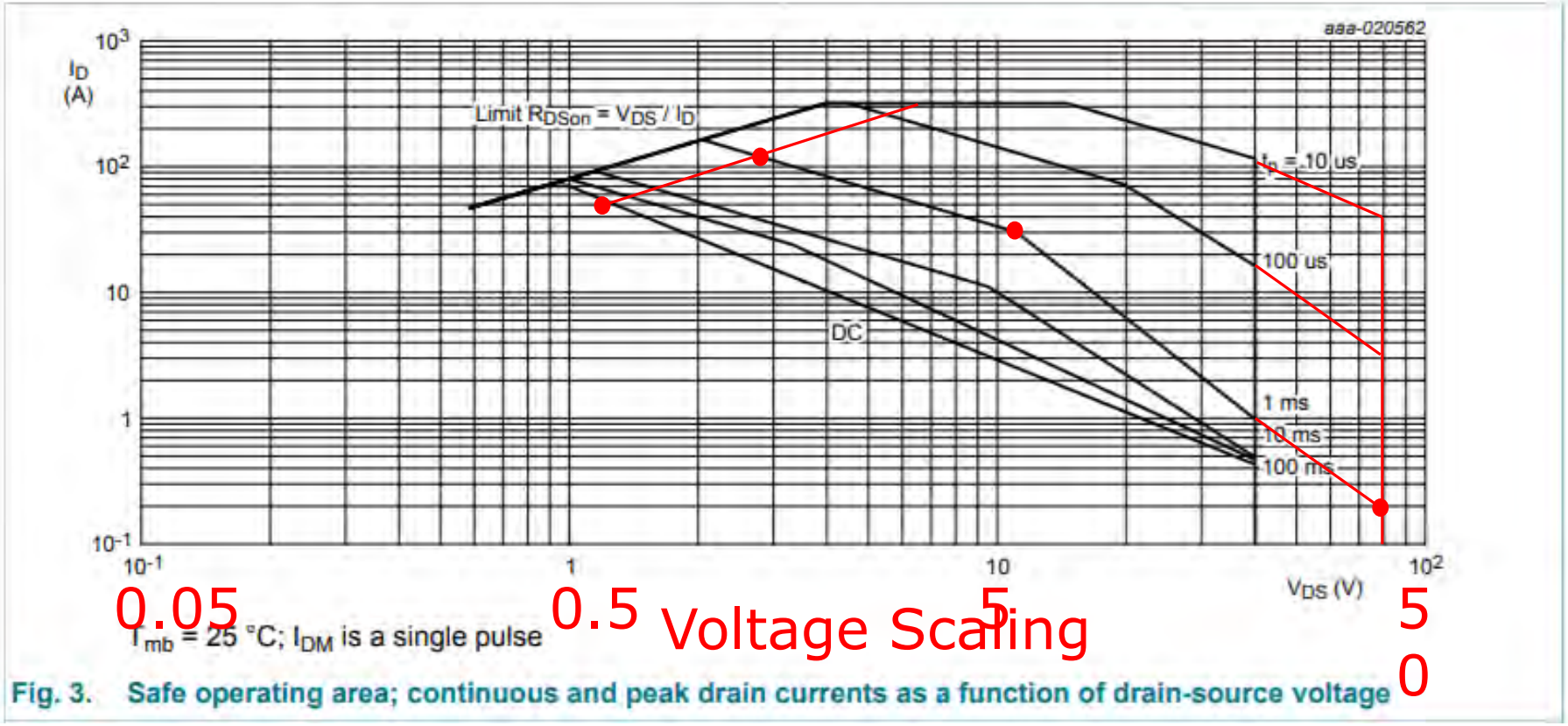


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

Derated to 50% power using Current Scaling on the Y-Axix

This is a 50% derating for 100C (using 175 C max)

Nexperia

BUK7M6R3-40E

N-channel 40 V, 6.3 mΩ standard level MOSFET in LFPAK33

50A, 600mV

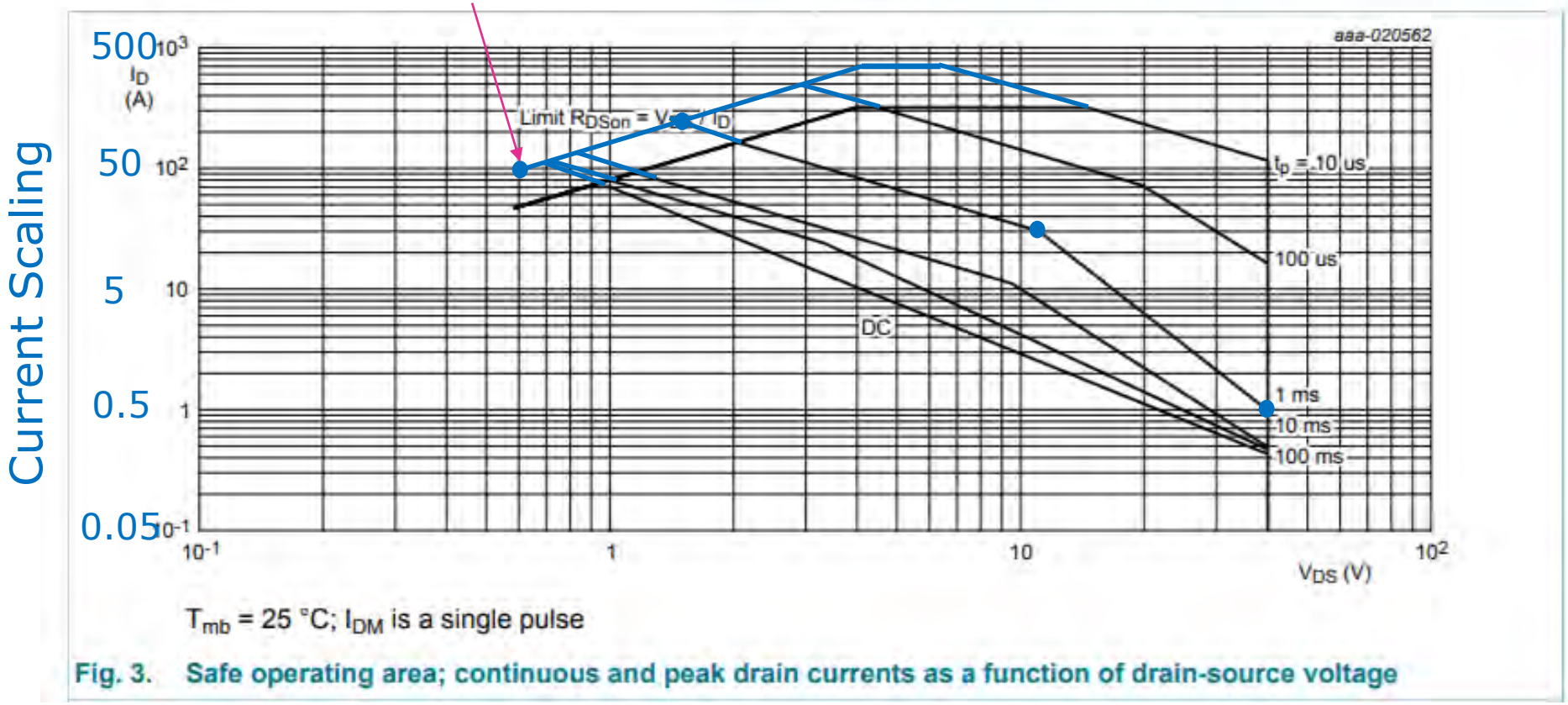


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

*New - Combined V & I - SOA De-rating Method

- Calculate the proportion based on Tjmax and Tmb

  Power Scale Factor = [Tjmax – Tmb(application)] / [Tjmax – Tmb(SOA Curve)]

  For a 175C device at 100C this is:

  PSF = [175 – 100] / [175 – 25] = **0.5**

  Take the Square Root of the PSF.

  √ PSF = **0.707**

  1) Rescale the x and y axis using the square root of the scale factor.
  2) Reposition the Imax and BVdss lines based on the new scale
  3) Extend the Rds limit line based on the new scale to intersect Imax
  4) Extend the data lines using the existing slopes

Derated to 50% power using combined Voltage and Current Scaling

This is a 50% derating for 100C (using 175 C max)

Nexperia

BUK7M6R3-40E

N-channel 40 V, 6.3 mΩ standard level MOSFET in LFPAK33

0.6V, 50A replot on new scale to define Rds limit

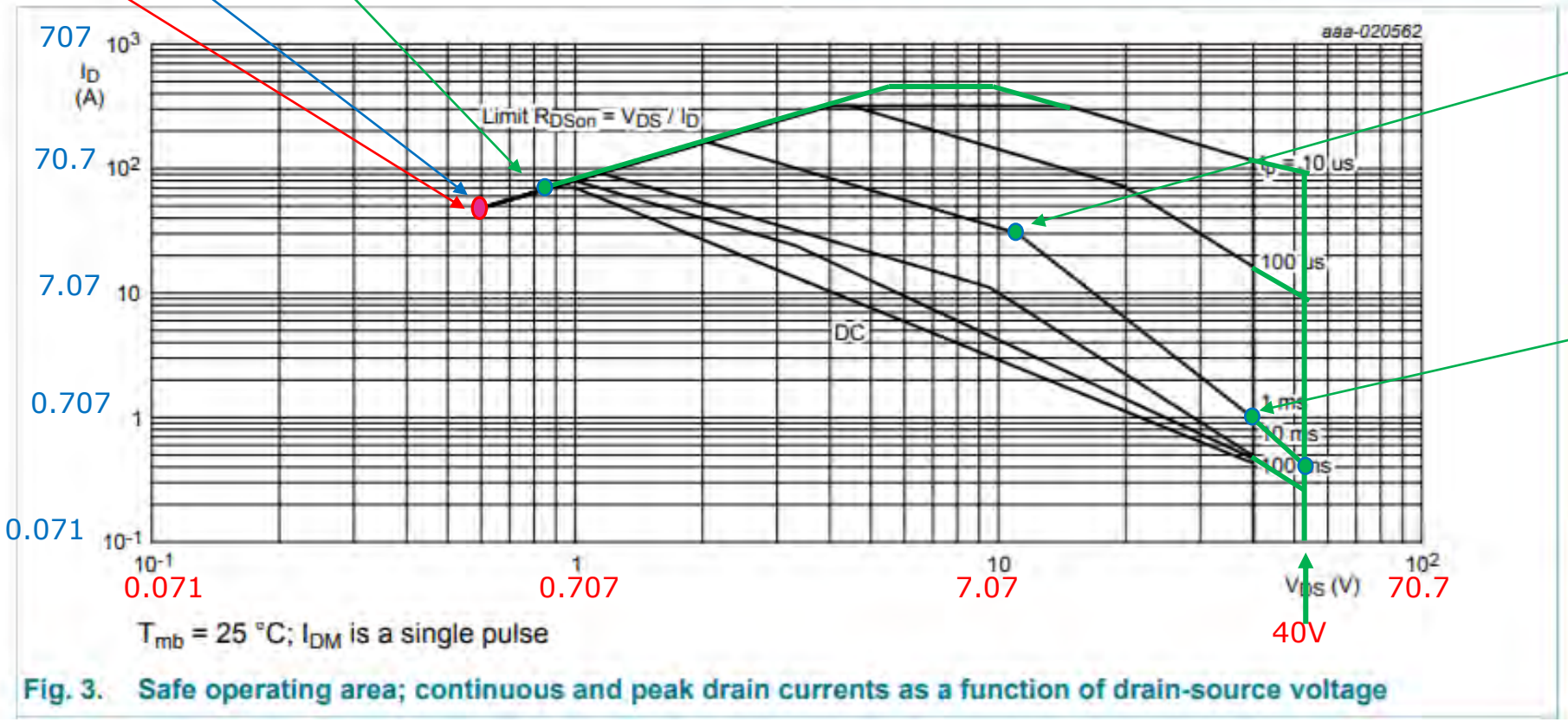


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

New Inflection Point

12V, 30A ➔ ~8V, 21.2A

40V, 1A ➔ 28.28V, 0.707A

Derated to 50% power comparison at 1mS – derating for 100C (using 175 C max)
Voltage vs. Current vs. V*I

Nexperia

BUK7M6R3-40E

N-channel 40 V, 6.3 mΩ standard level MOSFET in LFPAK33

Breakpoint at Constant Voltage with Current Scaling

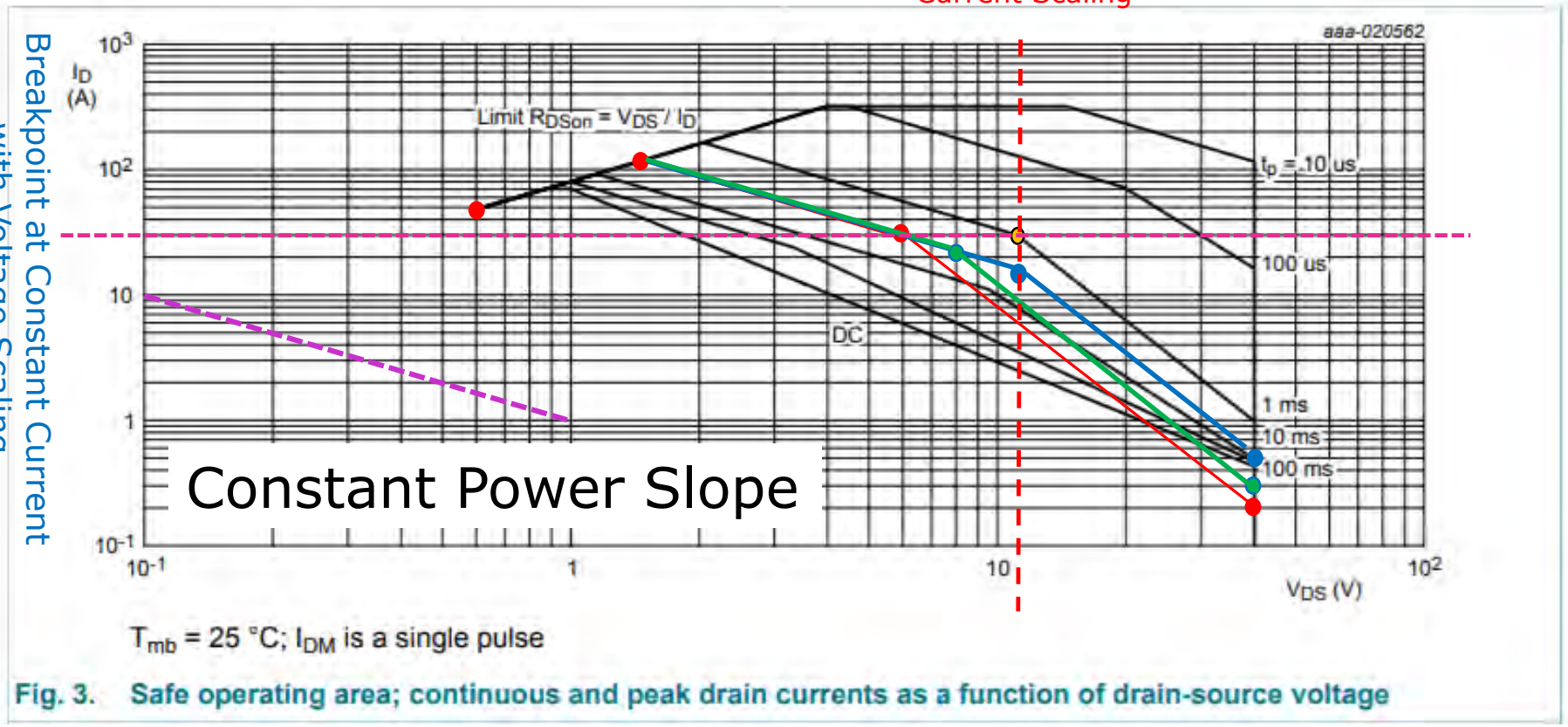


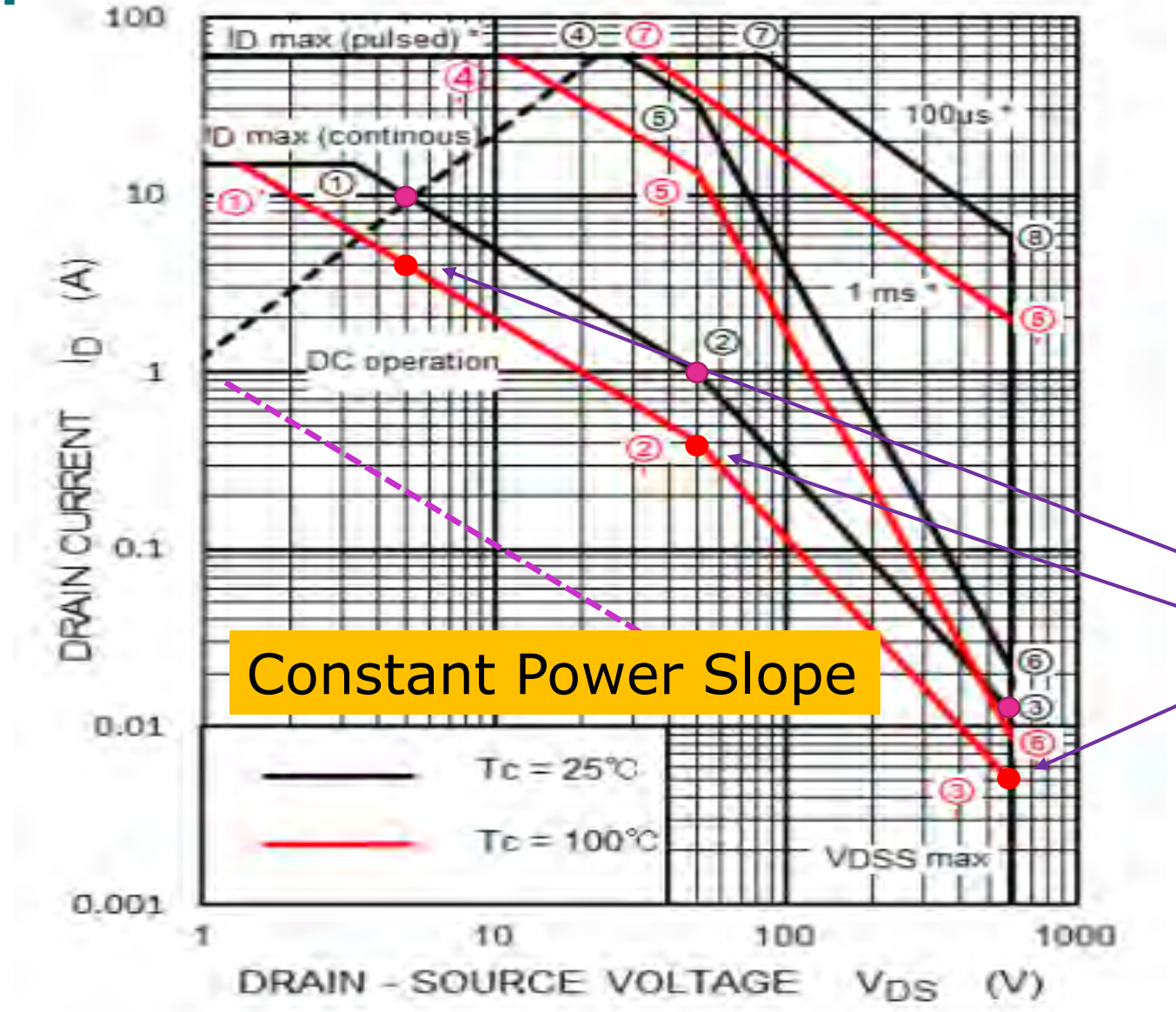
Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

Note that there is no difference in any method left of the Spirito effect region where the line follows the constant power formula.

The difference lies in where the Spirito effect break point starts.

(named after Professor Paolo Spirito)

Comparison to Toshiba method which uses more complex derivations



Derating from Toshiba Ap Note to 40% (i.e. 100C rating for 150C device.)

Although the Ap Note uses a complex mathematical approach, the result is simply the same as using 0.4 **Current derating on the Id y-axis**.

xV, yA @ 25C ➔ xV, **0.4*yA** @ 100C

5V, 10A ➔ 5V, 4A

50V, 1A ➔ 50V, 0.4A

600V, 0.014A ➔ 600V, 0.0056A

EFFICIENCY WINS.