

Information note

N° 10411AERRA

Dear customer,

With this Infineon Technologies AG information note, we would like to inform you about the following

Errata sheet Rev 1.0 affecting products TLE9210x

Infineon Technologies AG

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Information note

N° 10411AERRA

▶ **Products affected**

Please refer to attached affected product list
“ERR_10411AERRA_[customer-no].pdf”

▶ **Detailed change information**

Subject Introduction of an Errata sheet affecting products TLE9210x.

Reason Introduction of Errata sheet Rev.1.0 due to new known issue.

Description

<u>Old</u>	<u>New</u>
■ No Errata sheet	■ Errata sheet Rev.1.0

▶ **Product identification**

Not applicable (no change of product)

▶ **Impact of change**

Assessment in application required!

▶ **Attachments**

ERR_10411AERRA_[customer-no].pdf 3_cip10411	affected product list Errata sheet Rev. 1.0
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▶ **Intended start of delivery**

Not applicable, new Errata sheet is valid with immediate effect.

If you have any questions, please do not hesitate to contact your local sales office.

TLE9210x errata

About this document

Scope and purpose

This errata sheet describes the deviations of the TLE92108-232QX, TLE92104-232QX, TLE92104-131QX, TLE92108-231QX from the current datasheets and shows the workaround principles.

Table 1 Current datasheets

Device	Release date
Infineon-TLE92108-232QX-DataSheet-v01_00-EN	2019-08-29
Infineon-TLE92104-232QX-DataSheet-v01_00-EN	2020-09-21
Infineon-TLE92104-131QX-DataSheet-v01_00-EN	2020-09-21
Infineon-TLE92108-231QX-DataSheet-v01_00-EN	2019-08-29

Intended audience

Engineers developing applications with the TLE92108-232QX, TLE92104-232QX, TLE92104-131QX, TLE92108-231QX.

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1 Errata

1.1 Possible low-side drain-source overvoltage reported before expiration of the drain-source overvoltage filter time in PWM operation

Expected behavior

When the low-side (LS) MOSFET is the active MOSFET, after the expiration of the blank time (t_{BLANK}), the device does not detect a drain-source overvoltage (VDSOV) for a LS if:

- a falling edge of the internal LS control signal is generated
- while the drain-source voltage of the LS ($V_{\text{DS_LS}}$) exceeds the configured threshold ($V_{\text{VDSMONTHX}}$) for a duration shorter than the configured filter time (t_{FVDS})

The internal LS control signal is a control signal derived from the synchronized PWM signal.

A falling edge of the internal LS control signal signals that the LS MOSFET starts to be turned off, due to the PWM operation.

Actual behavior

After the expiration of t_{BLANK} , a VDSOV is detected for a LS if:

- a falling edge of the internal LS control signal is generated
- while $V_{\text{DS_LS}} > V_{\text{VDSMONTHX}}$ for $t < t_{\text{FVDS}}$ (**Figure 1**)

The LS is latched off and the VDSOV status bit of the corresponding LS is set.

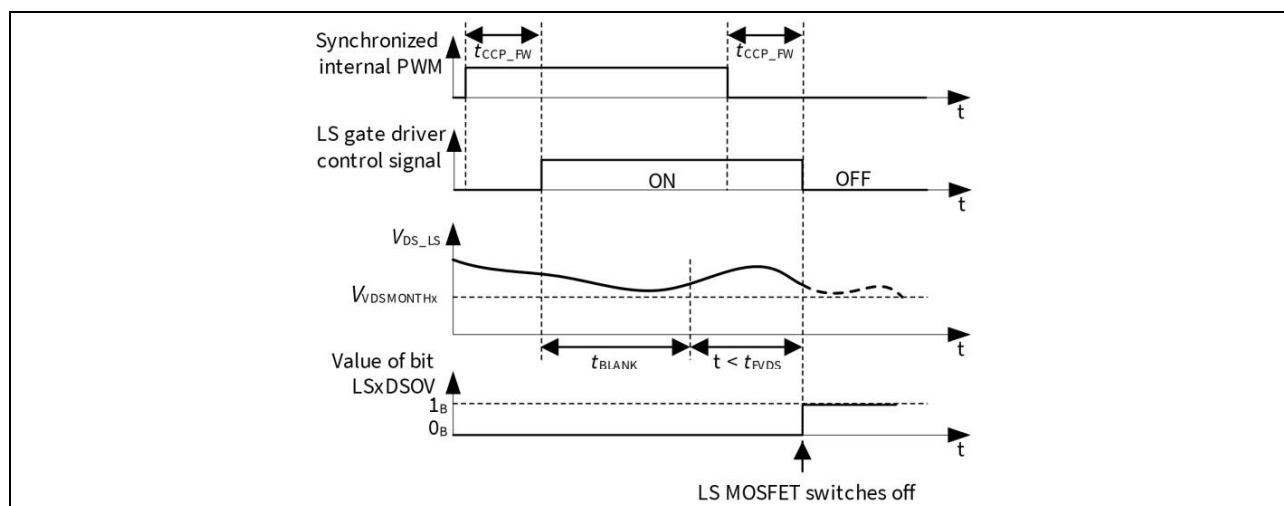


Figure 1 Falling edge of the internal LS control signal before the expiration of t_{FVDS}

Future action

Update the datasheets.

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1.2 Possible high-side drain-source overvoltage reported before expiration of the drain-source overvoltage filter time in PWM operation

Expected behavior

When the HS MOSFET is the active MOSFET, after the expiration of t_{BLANK} , a VDSOV is not detected for a HS if:

- a falling edge of the internal HS control signal is generated
- while $V_{\text{DS_HS}} > V_{\text{VDSMONTHX}}$ for $t < t_{\text{FVDS}}$

$V_{\text{DS_HS}}$ is the drain-source voltage of the high-side.

The internal HS control signal is a control signal derived from the synchronized PWM signal.

A falling edge of the internal HS control signal signals that the HS MOSFET starts to be turned off, due to the PWM operation.

Actual behavior

After the expiration of t_{BLANK} , a VDSOV is detected if:

- a falling edge of the internal HS control signal is generated
- while $V_{\text{DS_HS}} > V_{\text{VDSMONTHX}}$ for $t < t_{\text{FVDS}}$ (Figure 2)

The device reaction is:

- the HS is latched off
- the VDSOV status bit of the HS is not set
- the VDSOV status bit of the LS from the same half-bridge is set

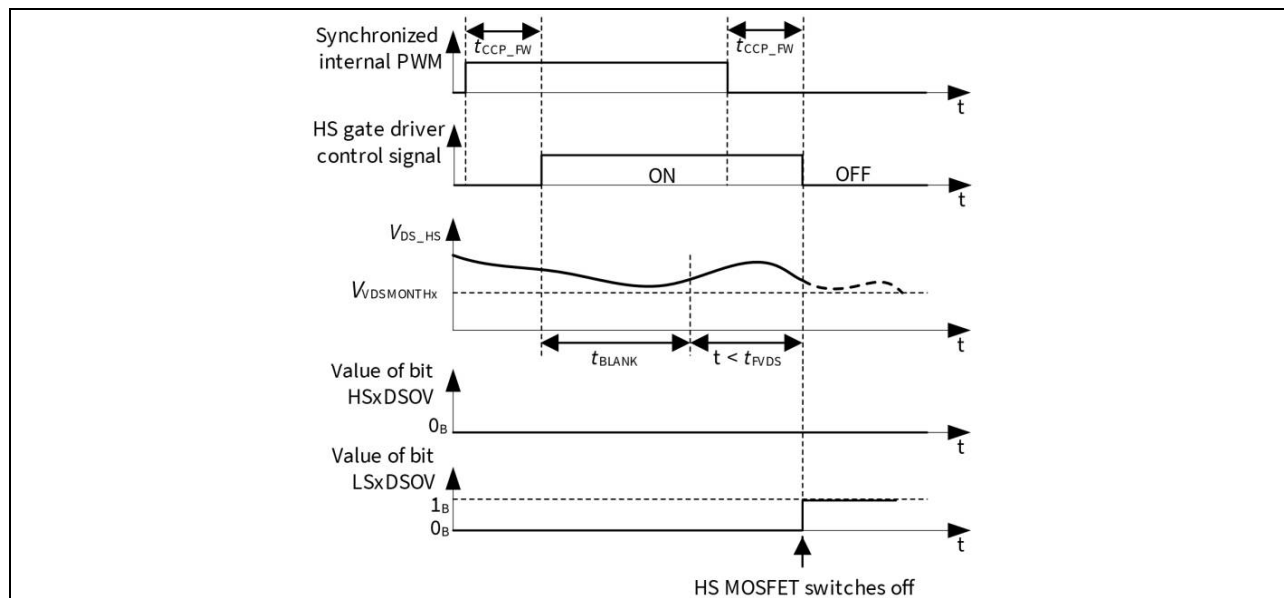


Figure 2 Falling edge of the internal HS control signal before the expiration of t_{FVDS}

Proposed workaround

Whenever a VDSOV is reported, perform an off-state diagnostic to confirm which MOSFET of the half-bridge is impacted.

References

Future action

Update the datasheets.

References

- [1] TLE92108-232QX datasheet, Infineon-TLE92108-232QX-DataSheet-v01_00-EN, 2019-08-29
- [2] TLE92104-232QX datasheet, Infineon-TLE92104-232QX-DataSheet-v01_00-EN, 2020-09-21
- [3] TLE92104-131QX datasheet, Infineon-TLE92104-131QX-DataSheet-v01_00-EN, 2020-09-21
- [4] TLE92108-231QX datasheet, Infineon-TLE92108-231QX-DataSheet-v01_00-EN, 2019-08-29

Revision history

Revision history

Document revision	Date	Description of changes
1.0	2023-05-01	First release

Trademarks

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Do you have a question about this document?

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Document reference

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Errata sheet Rev 1.0 affecting products TLE9210x

Affected products sold to FUTURE ELECTRONICS INC. (4000624)

Sales name	SP number	OPN	Package	Customer part number
TLE92104-131QX	SP001689960	TLE92104131QXXUM A1	PG-VQFN-48-31	TLE92104131QXXUMA1
TLE92104-232QX	SP001689962	TLE92104232QXXUM A1	PG-VQFN-48-31	TLE92104232QXXUMA1