Product Change Notification / SYST-11ETCK067

Date:

12-Apr-2023

Product Category:

EtherCAT

PCN Type:

Document Change

Notification Subject:

Data Sheet - LAN9252 2/3-Port EtherCAT SubDevice Controller with Integrated Ethernet PHYs

Affected CPNs:

SYST-11ETCK067_Affected_CPN_04122023.pdf
SYST-11ETCK067_Affected_CPN_04122023.csv

Notification Text:

SYST-11ETCK067

Microchip has released a new Datasheet for the LAN9252 2/3-Port EtherCAT SubDevice Controller with Integrated Ethernet PHYs of devices. If you are using one of these devices please read the document located at LAN9252 2/3-Port EtherCAT SubDevice Controller with Integrated Ethernet PHYs.

Notification Status: Final

Description of Change:

Section/Figure/Entry	Correction
Throughout Document	•I2C Host changed to I2C Controller •I2C Client changed to I2C Target •SPI or SQI “slave” changed to SQI “client” •Ethernet Slave Controller changed to ESC, Slave changed to SubDevice, and Master changed to MainDevice where appropriate
Table1-2, "Buffer Types", Table3-9, "EtherCAT Distributed	Added VOS8 buffer type.

Clock Pin Descriptions", Table3-10, "EtherCAT Digital I/O and GPIO Pin Descriptions", Table18-7, "Variable I/O DC Electrical Characteristics"	
Table7-1, "Hard-Strap Configuration Strap Definitions"	Updated strap tx_shift_strap MII TX Timing Shift numbers from “00 = 0ns, 01 = 10ns, 10 = 20ns, 11 = 30ns” to “00 = 20ns, 01 = 30ns, 10 = 0ns, 11 = 10ns”.
Table11-9, "100BASE-FX LOS, SD and TP Copper Selection PHY A"	Updated first entry in FXLOSEN column from “<1 V (typ.)” to “<2 V (typ.)”.
Section12.14.7, Port Descriptor Register	References to “EBUS” have been updated to “RESERVED”.
Section12.14.28, PDI Configuration Register	Updated Bits 5:4 from “00: End of Frame” to “00: Start of Frame”. Updated Bit 2, removing “direction configuration is ignored” and adding “Note: Direction control must be set to input.”
Section12.14.30, Extended PDI Configuration Register	Updated notes in Bits 7:0 from “Reserved in bidirectional mode (0b)” to “Must be cleared to 0 during bidirectional mode”.
Section12.14.48, EEPROM PDI Access State Register	Updated Bit 0 from “0: Do not change, 1: Reset” to “0: PDI releases EEPROM access, 1: PDI takes EEPROM access (PDI has EEPROM control)”.
Section12.14.61, Receive Time Port 0 Register, Section12.14.62, Receive Time Port 1 Register, Section12.14.63, Receive Time Port 2 Register	Removed APWR from description of Bits 31:0.
Section 18.1, "Absolute Maximum Ratings*"	Updated “Junction Temperature” to “Maximum Storage Junction Temperature.
Section18.2, Operating Conditions**	Added “125oC maximum operating junction temperature”
Figure19-1, Figure19-2, Figure19-3	Updated 64-VQFN package diagrams.

Impacts to Data Sheet: See above details.

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 12 Apr 2023

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices::N/A

Attachments:

LAN9252 2/3-Port EtherCAT SubDevice Controller with Integrated Ethernet PHYs

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

LAN9252/ML
LAN9252/PT
LAN9252I/ML
LAN9252I/PT
LAN9252V/ML
LAN9252TV/ML
LAN9252T/ML
LAN9252T/PT
LAN9252TI/ML
LAN9252TI/PT