Product Change Notification / SYST-18YIFQ586

Date:

20-Apr-2023

Product Category:

General Purpose FPGAs, System On Chip FPGAs

PCN Type:

Document Change

Notification Subject:

ERRATA - SmartFusion®2 Device Errata

Affected CPNs:

SYST-18YIFQ586_Affected_CPN_04202023.pdf
SYST-18YIFQ586_Affected_CPN_04202023.csv

Notification Text:

SYST-18YIFQ586

Microchip has released a new Errata for the SmartFusion®2 Device Errata of devices. If you are using one of these devices please read the document located at SmartFusion®2 Device Errata.

Notification Status: Final

Description of Change: Added 1.25. Avoid eNVM Page Lock and Unlock if Code is Being Executed from eNVM both in Release and Debug Mode

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 20 Apr 2023

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

SmartFusion®2 Device Errata

Please contact your local Microchip sales office with questions or concerns regarding this notification.

Terms and Conditions:

If you wish to receive Microchip PCNs via email please register for our PCN email service at our PCN home page select register then fill in the required fields. You will find instructions about registering for Microchips PCN email service in the PCN FAQ section.

If you wish to change your PCN profile, including opt out, please go to the PCN home page select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.

SYST-18YIFQ586 - ERRATA - SmartFusionÂ®2 Device Errata

Affected Catalog Part Numbers(CPN)

M2S010TS-FGG484IS0005
M2S010TS-FGG484IX416
M2S010TS-FGG484IX418
M2S010TS-FGG484I
M2S010TS-FGG484X418
M2S010TS-FGG484
M2S025TS-1VFG256T2
M2S025TS-1VFG400T2
M2S025TS-1FGG484T2
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M2S005S-VFG256H0276
M2S005S-VFG256H0290
M2S005S-VFG256IH0048
M2S005S-VFG256IH0094

SmartFusion®2 Device Errata

Introduction

The following table lists the device specific errata and the affected SmartFusion2 devices. See SmartFusion2 SoC FPGAs Data Security Devices Product Brief for the die revision part marking specification.

Table 1. Summary of SmartFusion2 Devices Errata

Errata No.	Errata	Silicon Revisions													Software Errata
		M2S005		M2S010			M2S025		M2S060	M2S090			M2S150		
		0	1, 2	0	1, 2	3	0	1, 2	0	0	1, 2	3	0	1, 2	
1.1	1.1. VPP Must Be Set to 2.5V While Programming and Writing the eNVM at Industrial Temperatures Range	X	—	X	—	—	X	—	—	—	—	—	—	—	—
1.2	1.2. Over-Voltage Support on MSIOs During Flash*Freeze	X	—	X	—	—	X	—	—	—	—	—	—	—	—
1.3	1.3. Verification of the FPGA Fabric at Junction Temperatures Higher than 50°C Erroneously Indicates a failure	X	—	X	—	—	X	—	—	—	—	—	—	—	—
1.4	1.4. DDR_OUT and I/O-Reg Functional Errata Due to a Software Bug	—	—	—	—	—	—	—	—	—	—	—	—	—	X
1.5	1.5. Dedicated Differential I/O Driving the Reference Clock of the CCC May Cause a Functional Failure Due to a Software Bug	—	—	—	—	—	—	—	—	—	—	—	—	—	X
1.6	1.6. Power-Up Digest is Not Supported	X	—	X	—	—	X	—	—	X	—	—	X	—	—
1.7	1.7. Programming of the eNVM Must Only Occur as Part of a Bitstream also Containing the FPGA Fabric	—	—	—	—	—	—	—	—	—	—	—	—	—	X
1.8	1.8. Updating eNVM from the MSS or the FPGA Fabric Requires Changes of the FREQRNG Register	X	X	X	X	X	X	X	X	X	X	X	X	X	—
1.9	1.9. SYSCTRL_RESET_STATUS Macro is Not Supported	X	—	X	—	—	X	—	—	X	—	—	X	—	—
1.10	1.10. Zeroization is Not Supported	X	—	X	—	—	X	—	—	X	X	—	X	—	—
1.11	1.11. Arm® Cortex®-M3 Register Corruption Under Very Specific Literal Loads from eNVM and Cache Miss/Hit Sequences	—	—	—	—	—	—	—	—	—	—	—	—	—	X
1.12	1.12. The System Controller RC Oscillator Runs at 25 MHz After a Programming Recovery Operation	—	—	NS	X	—	—	—	—	NS	X	—	—	—	—
1.13	1.13. ECC Point-Multiplication Service and ECC Point-Addition System Service are not Supported	—	—	—	—	—	—	—	—	X	—	—	X	—	—
1.14	1.14. Programming Silicon Requires Cortex-M3 Firmware Code	—	—	—	—	—	—	—	—	X	—	—	X	—	—
1.15	1.15. Programming of the FPGA Fabric Can Occur Only at Room Temperature	—	—	—	—	—	—	—	—	X	—	—	X	—	—
1.16	1.16. Programming of the eNVM Blocks needs to Occur Independent of the Fabric	—	—	—	—	—	—	—	—	X	—	—	X	—	—

.....continued

Errata No.	Errata	Silicon Revisions													Software Errata
		M2S005		M2S010			M2S025		M2S060	M2S090			M2S150		
		0	1, 2	0	1, 2	3	0	1, 2	0	0	1, 2	3	0	1, 2	
1.17	1.17. PCIe Hot Reset Support Requires a Soft Reset Solution	—	—	X	X	X	X	X	X	X	X	X	X	X	—
1.18	1.18. Executing SRAM-PUF Services Fails While the Cortex-M3 Code is Executed from eNVM_1	—	—	—	—	—	—	—	—	X	X	X	X	X	—
1.19	1.19. After Successful Completion of 2-step IAP or CM3 ISP (without a SYSRESET), LSRAM Read and Write Access Fails from the Fabric Path	X	X	X	X	X	X	X	X	X	X	X	X	X	—
1.20	1.20. SRAM-PUF System Services May Take Two to Three Seconds to Complete	—	—	—	—	—	—	—	—	X	X	X	X	X	—
1.21	1.21. Disable Cortex-M3 While Programming eNVM Only	X	X	X	X	X	X	X	X	X	X	X	X	X	—
1.22	1.22. The I/Os State During Programming is Changed from Z to Weak Pull-Up	X	—	X	—	—	X	—	—	—	—	—	X	—	—
1.23	1.23. For S (security) Grade Devices, User Must not Enable Write Protection for Protected 4K Regions, Also Known as Special Sectors in the eNVM	X	X	X	X	X	X	X	X	X	X	X	X	X	—
1.24	1.24. Users Must Not Set Page Lock in eNVM0 for the 060 Device and eNVM1 for 090/150 Devices	—	—	—	—	—	—	—	X	X	X	X	X	X	—
1.25	1.25. Avoid eNVM Page Lock and Unlock if Code is Being Executed from eNVM both in Release and Debug Mode	X	X	X	X	X	X	X	X	X	X	X	X	X	—

Notes: In the preceding table,

- X indicates that the errata is available for that device and revision number.
- "—" indicates that errata is not available or the feature does not exist for that device and revision number.
- NS (Not Supported) indicates that the Programming Recovery Mode is not available in this revision.
- Software errata can be avoided by using Libero® SoC v11.4 SPI or later.
- Contact Microchip SoC Technical Support for any additional questions. To order a specific die, contact your local Microchip sales office.

Table 2. Revisions Released per Device

Silicon Devices	Revisions	Device Status
M2S005 (S)	Commercial/Industrial	Production
M2S010 (S, T, TS)	Commercial/Industrial	Production
M2S025 (T, TS)	Commercial/Industrial	Production
M2S060 (T, TS)	Commercial/Industrial	Production
M2S090 (T, TS)	Commercial/Industrial	Production
M2S150 (T, TS)	Commercial/Industrial	Production

Table of Contents

1. Errata Descriptions and Solutions

This section describes the Errata and solutions of SmartFusion2 device.

1.1 VPP Must Be Set to 2.5V While Programming and Writing the eNVM at Industrial Temperatures Range

VPP can be set to 2.5V or 3.3V. However, while writing or programming the eNVM of Revision 0 of the M2S005, M2S010, and M2S025 devices below 0°C, VPP must be set to 2.5V. See DS0128: IGLOO2 and SmartFusion2 Datasheet for VPP minimum and maximum settings.

Note: eNVM reading with VPP set to 3.3V or 2.5V operates as intended.

1.2 Over-Voltage Support on MSIOs During Flash*Freeze

When the input voltage is driven above the reference voltage for that bank, additional current can be consumed in the Flash*Freeze mode for Revision 0 of the following devices: M2S005, M2S010, and M2S025.

1.3 Verification of the FPGA Fabric at Junction Temperatures Higher than 50°C Erroneously Indicates a failure

In Revision 0: M2S005, M2S010, and M2S025 devices, standalone verification (STAPL VERIFY action) must be run at temperatures lower than 50 °C. If a VERIFY action is run at temperatures higher than 50 °C, a false verify failure may be reported.

Note: The Check Digest system services can be used to confirm design integrity at temperatures within the recommended operation conditions.

1.4 DDR_OUT and I/O-Reg Functional Errata Due to a Software Bug

This Errata only applies if you created or updated your design using Libero SoC v11.1 SP1 or v11.1 SP2. If you have one of the following in your design, the corresponding I/O will not function properly in the silicon due to the wrong software implementation of the I/O macro.

- If you use DDR_OUT macro in your design.
- If you combine an output or output enable register with an I/O using the PDC command set_io <portName> -register yes

Workaround

Both the Erratas are fixed in Libero SoC v11.1 SP3. Migrate your design to Libero SoC v11.1 SP3 or newer version, and re-run compile and layout.

1.5 Dedicated Differential I/O Driving the Reference Clock of the CCC May Cause a Functional Failure Due to a Software Bug

If your design has the dedicated differential I/O pair driving the reference clock of the CCC, the input clock may not propagate to CCC due to a software bug and the device will fail during silicon testing. There are several options to drive the ref clock of the CCC. One of the options is to drive from “Dedicated Input PAD x” (x = 0 to 3); this uses hardwired routing. In this option, choose single-ended I/O or differential I/O as the ref clock. This Errata exists when you choose the differential I/O option, meaning the dedicated differential I/O is used as CCC reference clock input. This Errata cannot be detected in any functional simulation and can only be detected in silicon testing.

Workaround

The Errata is fixed in the Libero SoC v11.1 SP3. Migrate your design to the Libero SoC v11.1 SP3 or newer version, and re-run compile and layout.

1.6 Power-Up Digest is Not Supported

Power-up digest is not supported in Revision 0 of the M2S005, M2S010, M2S025, M2S090, and M2S150 devices.

Workaround

Use NVM Data Integrity Check System service after the device is ON and check the data integrity.

1.7 Programming of the eNVM Must Only Occur as Part of a Bitstream also Containing the FPGA Fabric

The Bitstream Configuration Dialog Box in the Libero SoC allows programming eNVM and the FPGA fabric, separately. However, if using Libero v11.1 SP2 or an older version, program the eNVM along with the FPGA fabric for the M2S005, M2S010, M2S025, and M2S050 devices. The fabric can be programmed separately, if needed.

Workaround

The Errata is fixed in the Libero SoC v11.1 SP3. Migrate your design to the Libero SoC v11.1 SP3 or newer version, and re-run compile and layout.

1.8 Updating eNVM from the MSS or the FPGA Fabric Requires Changes of the FREQRNG Register

While updating the eNVM from the FPGA fabric, the NV_FREQRNG register must be changed from the default value 0x07 to 0x0F; eNVM reads are not affected. SmartFusion2 eNVM firmware driver v2.2 has been updated with the correct NV_FREQRNG settings. See Appendix B of AC429 for more details on eNVM Read/Write Operation and eSRAM Read/Write Operations.

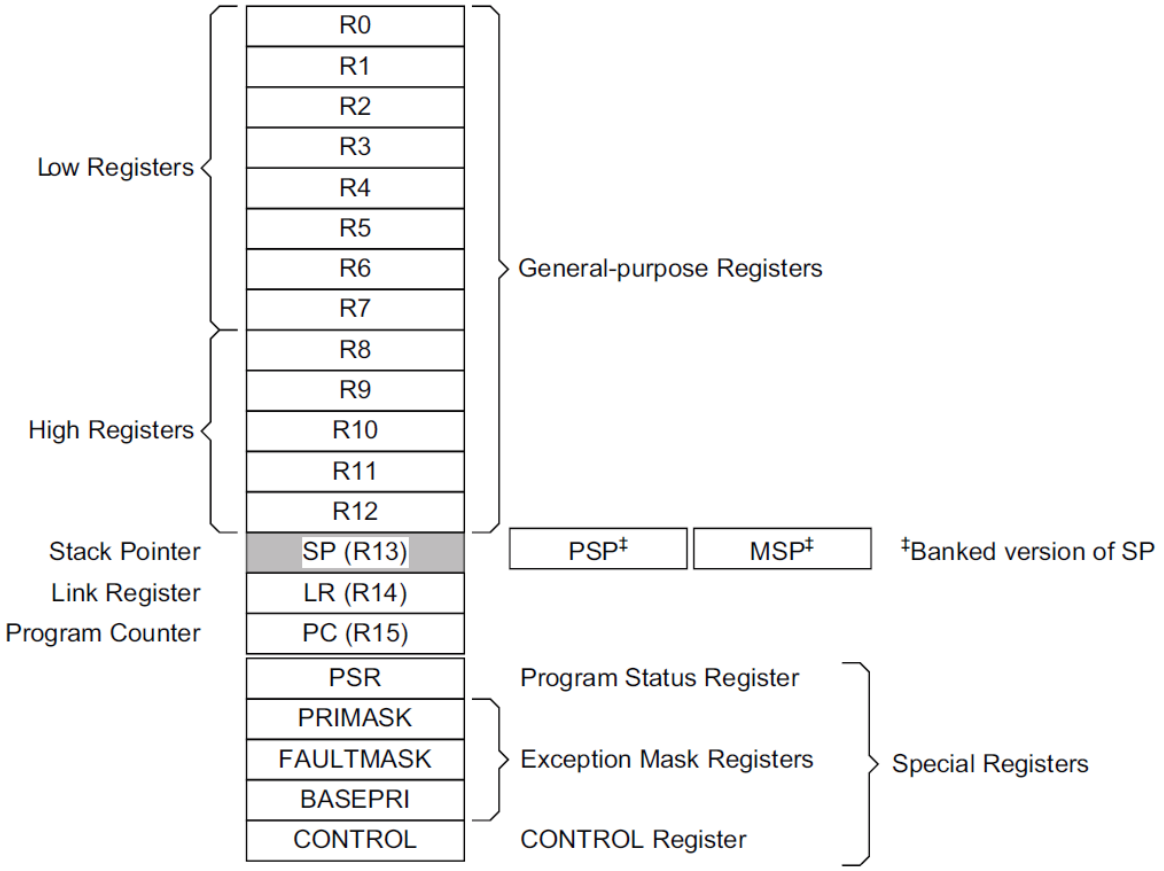
1.9 SYSCTRL_RESET_STATUS Macro is Not Supported

1.10 Zeroization is Not Supported

1.11 Arm® Cortex®-M3 Register Corruption Under Very Specific Literal Loads from eNVM and Cache Miss/Hit Sequences

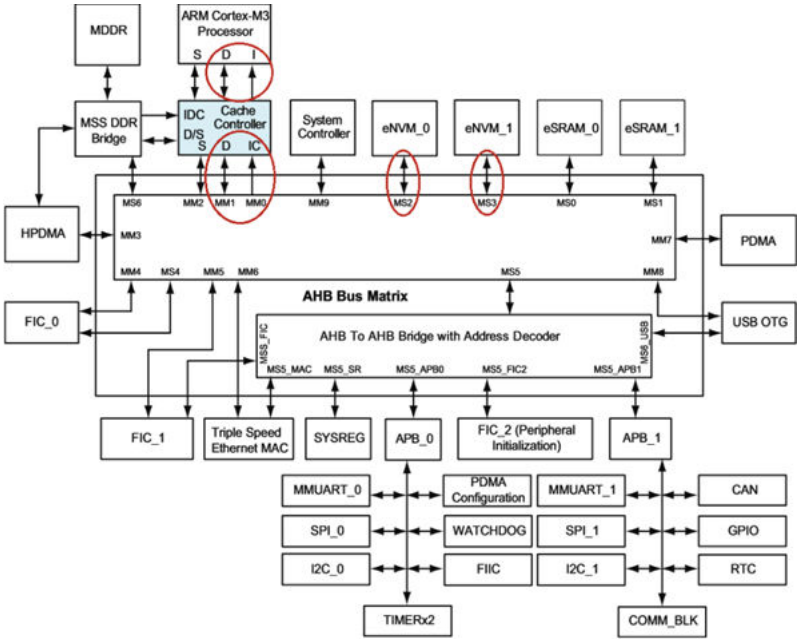
Cortext-M3 internal general-purpose registers (for example R6) gets corrupted when two nested D-Bus (must be a non-64-bit-aligned access) and I-Bus cache miss cycles occur in cache controller fetching from eNVM followed immediately by a D-Bus read without cache miss.

Figure 1-1. Cortex-M3 Core Register Set



SmartFusion2 system implements a cache controller in between Cortex-M3 and the memory subsystems (eNVM, eSRAM, Fabric sRAM, and DDR). An AHB matrix is used to arbitrate between eNVM, eSRAM, and Fabric sRAM access while a separate dedicated bus interfaces with DDR.

Figure 1-2. Cache Controller Interfaces and Paths Affected by CN (Red Circles)



SmartFusion2 Cache Controller allows mapping these memories, that is eNVM, on cacheable code regions. All M2S devices, apart from M2S050 (see Microchip SmartFusion2 Microcontroller Subsystem User Guide (UG0331)), come with a Cortex-M3 configuration that explicitly avoids simultaneous I-Bus and D-Bus address phases to ease arbitration of cache resource.

When the cache controller is enabled and mapped to eNVM, the following sequence of operations causes I-Bus and D-Bus accesses to be queued internally, leading to a state analogous to an I-Bus and D-Bus concurrent access.

1. A D-Bus miss has occurred to a non-aligned 64-bit address causing the cache controller to fetch the data from eNVM. This misaligned transaction extends the memory bus cycle.
2. While the cache logic is completing the cache fill operation after fetching from eNVM, an I-Bus miss occurs. The I-Bus operation is put on hold while waiting for cache filling operation to complete.
3. While I-Bus operation is in a wait state, a D-Bus read without a cache miss occurs. For this event to occur the D-Bus read must be within three cycles (the number of Cortex-M3 pipeline stages) to the I-Bus read/miss, a situation that mimics a simultaneous I-Bus and D-Bus read access.

A D-Bus read takes the precedence over an I-Bus but the data loaded into the Cortex-M3 internal register (for example, R6) is erroneously the I-Bus data which causes the corruption and consequently the application fails in an unpredictable manner.

Impact

The occurrence of this scenario described is rare. Moreover, the applications that meet any one of the four conditions listed are **not** impacted:

- The application executable has been 100% functionally tested across all supported operating conditions on every production unit and no such failures are observed.
- The cache controller is disabled in the design MSS configuration.
- The application is executed in any memory space other than eNVM.
- D-Bus literal loads are disabled during the compile of the code.

However, the corruption happens every time the specific cache miss/hit sequence occur regardless of the operating conditions or clock frequency.

Workaround

1. Add one the following compiling options depending on the toolchain used. This option prevents a D-Bus read to happen after I-Bus read. The following is a list of most common compilers used.
   - Keil, `--no_integer_literal_pools` or similar options
   - IAR, `--no_literal_pool`
   - GCC-ARM, `-mpure-code`
2. Recompile the code and update the executable code on the boot medium.

If using SoftConsole, you might need to update the project to the v5.1 or newer version, since the `-mpure-code` option is available only in recent gcc-arm toolchains.

1.12 The System Controller RC Oscillator Runs at 25 MHz After a Programming Recovery Operation

After a programming recovery event, the system controller will be operating at 25 MHz. Ideally the system controller must operate at 50 MHz after a programming recovery event.

Workaround

If operating the system controller at 50 MHz is important to your design, contact soc_tech@microsemi.com.

1.13 ECC Point-Multiplication Service and ECC Point-Addition System Service are not Supported

1.14 Programming Silicon Requires Cortex-M3 Firmware Code

For the Revision 0 of the M2S090 and M2S150 devices, the eNVM needs to contain valid Cortex-M3 code. By default, SmartFusion2 parts are shipped with a default boot-up program stored at the eNVM address 0x60000000. If this default program is no longer valid or overwritten by the user, and there is no valid user boot code, the Cortex-M3 does not execute to a valid state. This leads to unexpected behavior including the programming lockout condition in Revision 0 of the M2S090 and M2S150 devices.

Workaround

The firmware code must be programmed into the eNVM prior to re-programming a commercial device. A while(1) statement will work. See *Knowledge Base (KB) SmartFusion2: Managing Cortex-M3*, while accessing MSS from fabric, when there is no default or valid boot code for Cortex-M3 to execute for details.

1.15 Programming of the FPGA Fabric Can Occur Only at Room Temperature

1.16 Programming of the eNVM Blocks needs to Occur Independent of the Fabric

Customer using Revision 0 of M2S090 or M2S150 devices must Program the eNVM block independently in Libero v11.6 or older. Contact Microchip SoC Technical Support, to program the eNVM block independently in Revision 0 of M2S090 and M2S150 devices using Libero v11.7.

1.17 PCIe Hot Reset Support Requires a Soft Reset Solution

On SmartFusion2 devices, a PCIe Hot Reset requires a soft FPGA logic reset scheme which clears the sticky bits of the PCI configuration space.

Workaround

On SmartFusion2 devices, a PCIe Hot Reset requires a soft FPGA logic reset scheme which clears the sticky bits of the PCI configuration space.

The application note AN437 – Implementing PCIe Reset Sequence in SmartFusion2 and IGLOO2 Devices describes the PCIe Hot Reset reset scheme. However, this reset scheme causes PCIe violations in some cases.

- For the M2S060/090T(S) devices there are no violations.
- For the M2S010/025/150T(S) devices at Gen1 rates there are no violations.
- For the M2S/025/150T(S) devices at Gen2 rates there are two PCIe CV violations.
  - Test case 1: TD_1_7 (Advanced Error Reporting Capability)
  - Test case 2: TD_1_41 (LinkCap2Control2Status2 Reg).

1.18 Executing SRAM-PUF Services Fails While the Cortex-M3 Code is Executed from eNVM_1

In the SmartFusion2 M2S090/M2S150 devices, the system controller does not release the eNVM1 access after executing the following SRAM-PUF system services:

- Create User AC (Activation Code) service
- Delete User AC service
- Create User KC for an Intrinsic Key service
- Create User KC for an Extrinsic Key service
- Delete User KC service

The above system services get executed successfully but the eNVM1 becomes inaccessible to Cortex-M3 and to fabric master.

- Any subsequent access to eNVM1 after this point, where eNVM1 is locked by System Controller, results in a stall, and a Power on Reset (POR) is needed to remove the stall.

Workaround

Execute “Get Number of the Key Code (GET_NUMBER_OF_KC)” SRAM-PUF system services immediately after the above services.

- The additional GET_NUMBER_OF_KC services releases the eNVM1 access from the System Controller.
- The firmware code for running SRAM-PUF services workaround must be executed from eNVM0, eSRAM, or DDR memories only, as Cortex-M3 does not get access to the eNVM1 that time.

1.19 After Successful Completion of 2-step IAP or CM3 ISP (without a SYSRESET), LSRAM Read and Write Access Fails from the Fabric Path

If LSRAM Read and Write access fails from the fabric path after performing 2-step IAP or CM3 ISP, perform a system reset or F*F Entry/Exit.

Workaround

The user application must execute System Reset as soon as the IAP/ISP system service is completed. Otherwise, user write and read accesses to LSRAM/uRAM is not possible. The System Reset can be generated using the tamper macro (availably in the Libero SoC Catalog). Immediately after the IAP/ISP service, the user logic checks the LSRAM/uRAM access. If access is denied, the user logic sends the reset request/interrupt to the system controller through the tamper macro (by enabling the RESET function in the tamper macro configuration window) and then the system controller executes the system level reset. For more information, see UG0451: IGLOO2 and SmartFusion2 Programming User Guide.

The following application notes have more information and design examples on how to implement the workaround:

- SmartFusion2 SoC FPGA - In-System Programming Using USB OTG Controller Interface - Libero SoC v11.5 Demo Guide.
- SmartFusion2 SoC FPGA - In-System Programming Using UART Interface Demo - Libero SoCv11.5 Demo Guide.
- SmartFusion2 SoC FPGA In-Application Programming Using PCIe Interface - Libero SoC v11.5 Demo Guide.

1.20 SRAM-PUF System Services May Take Two to Three Seconds to Complete

This Errata is fixed in the newer date code devices, where SRAM-PUF system services will run faster. Contact soc_tech@microsemi.com for more information.

1.21 Disable Cortex-M3 While Programming eNVM Only

The user uses the Bitstream Configuration dialog box in the Libero SoC tool and generates an eNVM only stapl file. During programming, the system controller takes control of the eNVM block. If the user design has the application code running from the eNVM block, the Cortex-M3 processor halts as it cannot access the eNVM block. When the eNVM block programming is completed, the system controller releases the eNVM. The Cortex-M3 continues running from the same address from where it was halted at unless the device is re-started. If the device in not re-started, the Cortex-M3 behavior will be unpredictable as the eNVM is updated with the new code.

Workaround

- Use the M3_Reset_N signal to hold the Cortex-M3 processor in reset before programming the eNVM block.
- Force a device to re-start.
- Program eNVM and fabric. Libero v11.7 will fix the unpredictable behavior issue by forcing a re-start of the device after eNVM programming.

1.22 The I/Os State During Programming is Changed from Z to Weak Pull-Up

The I/O state during programming is changed from Z to weak pull-up in the latest die revisions. Affected die revisions (marked with "X" in Table 1) have I/Os that are tristated during programming.

1.23 For S (security) Grade Devices, User Must not Enable Write Protection for Protected 4K Regions, Also Known as Special Sectors in the eNVM

For S (security) devices, there are two or four 4 KB regions per eNVM array that can be protected for read and write, these regions are known as Protected 4K Regions or Special Sectors. If write protection is enabled for any of these regions, none of the locked pages inside the same eNVM block can be unlocked.

1.24 Users Must Not Set Page Lock in eNVM0 for the 060 Device and eNVM1 for 090/150 Devices

For 060, 090, and 150 device densities: Each eNVM memory block has a user page lock bit (see PAGE_LOCK_SET register) to lock a page and prevent accidental writing. After the page lock is set in eNVM0 for the 060 device or eNVM1 for 090/150 devices, the user will not be able to clear the lock for subsequent page updates later.

Workaround

To use page lock feature, the user can use eNVM0 of 090/150 device and set/clear page lock using the master (for example, M3 or fabric). There is no workaround for the 060 device. User must contact SoC tech support to unlock if they already used page lock in the 060 device.

1.25 Avoid eNVM Page Lock and Unlock if Code is Being Executed from eNVM both in Release and Debug Mode

Updating eNVM protected sectors requires a preliminary unlocking of the eNVM. In the time between unlocking and re-locking, no reads from eNVM are allowed.

Workaround

If the linker script places M3 code into eNVM, where it will execute-in-place, then the user should avoid eNVM page lock and unlock API's in both release mode and debug mode.

2. Usage Guidelines for SmartFusion2 Devices

The following section details the usage guidelines for SmartFusion2 devices.

2.1 Programming Support

Table 2-1. Revision 0 Devices

Programming Mode	JTAG	SPI Slave	Auto Programming	Auto Update	2-Step IAP	Programming Recovery	M3 ISP
Programming Interface	JTAG	SPI_SC	SPI_0	SPI_0	SPI_0	SPI_0	N/A
M2S005(S)	Yes	Yes	No	No	No	No	Yes
M2S010 (S,T,TS)	Yes	Yes	No	No	No	No	Yes
M2S025 (T,TS)	Yes	Yes	No	No	No	No	Yes
M2S060 (T, TS)	Yes	Yes	Yes	Yes	Yes	Yes	Yes
M2S090 (T,TS)	Yes	Yes	No	No	No	Yes[1]	Yes
M2S150 (T,TS)	Yes	Yes	No	No	No	No	Yes

Notes:

1. See Errata item 1.12. The System Controller RC Oscillator Runs at 25 MHz After a Programming Recovery Operation.
2. Package dependencies that might not expose certain programming interfaces might be present. See the PB0115: SmartFusion2 System-on-Chip FPGAs Product Brief for device/package specific features.

Table 2-2. Revision 1 Devices

Programming Mode	JTAG	SPI Slave	Auto Programming	Auto Update	2-Step IAP	Programming Recovery	M3 ISP
Programming Interface	JTAG	SC_SPI	SPI_0	SPI_0	SPI_0	SPI_0	N/A
M2S005 (S)	Yes	Yes	Yes	Yes	Yes	Yes	Yes
M2S010 (S,T,TS)	Yes	Yes	Yes	Yes	Yes	Yes[1]	Yes
M2S025 (T,TS)	Yes	Yes	Yes	Yes	Yes	Yes	Yes
M2S090 (T,TS)	Yes	Yes	Yes	Yes	Yes	Yes[1]	Yes
M2S0150 (T,TS)	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Note: See Errata item 1.12. The System Controller RC Oscillator Runs at 25 MHz After a Programming Recovery Operation.

Table 2-3. Revision 2 Devices

Programming Mode	JTAG	SPI Slave	Auto Programming	Auto Update	2-Step IAP	Programming Recovery	M3 ISP
Programming Interface	JTAG	SC_SPI	SPI_0	SPI_0	SPI_0	SPI_0	N/A
M2S005 (S)	Yes	Yes	Yes	Yes	Yes	Yes	Yes
M2S010 (S,T,TS)	Yes	Yes	Yes	Yes	Yes	Yes[1]	Yes
M2S025 (T,TS)	Yes	Yes	Yes	Yes	Yes	Yes	Yes
M2S090 (T,TS)	Yes	Yes	Yes	Yes	Yes	Yes[1]	Yes

.....continued

Programming Mode	JTAG	SPI Slave	Auto Programming	Auto Update	2-Step IAP	Programming Recovery	M3 ISP
M2S150 (T,TS)	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Note: See Errata item 1.12. The System Controller RC Oscillator Runs at 25 MHz After a Programming Recovery Operation.

Table 2-4. Revision 3 Devices

Programming Mode	JTAG	SPI Slave	Auto Programming	Auto Update	2-Step IAP	Programming Recovery	M3 ISP
Programming Interface	JTAG	SC_SPI	SPI_0	SPI_0	SPI_0	SPI_0	N/A
M2S010 (T, TS)	Yes	Yes	Yes	Yes	Yes	Yes	Yes
M2S090 (T,TS)	Yes	Yes	Yes	Yes	Yes	Yes	Yes

2.2 SHA-256 System Service

Microchip recommends the message required to be on byte boundary when using SHA-256 System Service for the SmartFusion2 devices.

2.3 MSS Reset Mode

To keep the MSS in reset during normal operation, it is necessary to wait for the device to power up, and then apply the reset. The US_POR_B signal from the MSS (the power-on-reset for the FPGA fabric) can be used to check the device's powered up state.

2.4 Accessing the PCIe Bridge Register in the High-Speed Serial Interface

The PCIe Bridge registers must not be accessed before the PHY is ready. Wait for the PHY_READY signal (which indicates when PHY is ready) to be asserted before updating the PCIe Bridge registers.

The PHY_READY signal is normally asserted within 200 µs after the device is powered up, so wait for 200 µs before accessing the PCIe Bridge registers.

3. Revision History

Revision	Date	Description
B	04/2023	The following is the summary of changes in revision B: • Added 1.25. Avoid eNVM Page Lock and Unlock if Code is Being Executed from eNVM both in Release and Debug Mode
A	10/2021	The following is the summary of changes in revision A: • The document was updated to Microchip template. • The document number was changed from 55900196 to DS80000978. • Updated content in 1.11. Arm® Cortex®-M3 Register Corruption Under Very Specific Literal Loads from eNVM and Cache Miss/Hit Sequences section.
1.5	9/16	Updated text for item 1.11. Arm® Cortex®-M3 Register Corruption Under Very Specific Literal Loads from eNVM and Cache Miss/Hit Sequences.
1.4	7/16	Updated text for item 1.22. The I/Os State During Programming is Changed from Z to Weak Pull-Up.
1.3	4/16	Added Errata items 1.23. For S (security) Grade Devices, User Must not Enable Write Protection for Protected 4K Regions, Also Known as Special Sectors in the eNVM and 1.24. Users Must Not Set Page Lock in eNVM0 for the 060 Device and eNVM1 for 090/150 Devices.
1.2	12/15	The following items are added in revision 1.2 of this document: • Updated Table 1 to include the M2S010 device in revision 3. • Added errata items Disable Cortex-M3 when programming eNVM only and The I/Os state during programming is changed from Z to weak pull-up. • Updated Table 2-4 to include the M2S010 (T, TS) device. • Added solution for item 1.7. Programming of the eNVM Must Only Occur as Part of a Bitstream also Containing the FPGA Fabric.
1.1	5/15	Updated M2S060 revision from ES to revision 0.
1.0	5/15	The following items are added in revision 1.0 of this document: • Combined M2S005, M2S010, M2S025, M2S060, M2S090, and M2S150 devices and die revisions to one centralized document. • Created a separate Errata for the M2S050 device.

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