Product Change Notification / SYST-24WWDE722

Date:

27-Mar-2023

Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ERRATA - PIC16F18156/76 Silicon Errata and Datasheet Clarifications

Affected CPNs:

SYST-24WWDE722_Affected_CPN_03272023.pdf
SYST-24WWDE722_Affected_CPN_03272023.csv

Notification Text:

SYST-24WWDE722

Microchip has released a new Errata for the PIC16F18156/76 Silicon Errata and Datasheet Clarifications of devices. If you are using one of these devices please read the document located at PIC16F18156/76 Silicon Errata and Datasheet Clarifications.

Notification Status: Final

Description of Change:
Initial release of this document. Includes silicon 1.1.1 and 1.1.2 (Analog-to-Digital Converter with Computation) and 1.2.1 (Digital-to-Analog Converter).

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 27 Mar 2023

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

PIC16F18156/76 Silicon Errata and Datasheet Clarifications

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

PIC16F18156-I/SP
PIC16F18156-I/SS
PIC16F18176-I/MP
PIC16F18176-I/P
PIC16F18156-I/STX
PIC16F18176-I/PT

PIC16F18156/76

PIC16F18156/76 Silicon Errata and Data Sheet Clarifications

The PIC16F18156/76 devices that you have received conform functionally to the current device data sheet (DS40002484**A**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC16F18156/76 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID
		B0
PIC16F18156	0x3113	0xA040
PIC16F18176	0x3114	0xA040

Important: Refer to the **Device/Revision ID** section in the device data sheet for more detailed information on Device Identification and Revision IDs for your specific device.

Silicon Issue Summary

Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions
				B0
Analog-to-Digital Converter with Computation (ADCC)	Acquisition Time	1.1.1	Acquisition time cannot be changed through either the ADACQ or the ADPRE registers.	X
Analog-to-Digital Converter with Computation (ADCC)	ADC Voltage Reference	1.1.2	RA2 is not working as V_{REF}- in Single-Ended Mode.	X
Digital-to-Analog Converter (DAC)	DAC Auto Enable	1.2.1	Mid-ban voltage spike at code 128 may occur when DACAUTOEN is enabled and the application is incrementing the DACxDATL register from 127 to 129.	X
Note: Only those issues indicated in the last column apply to the current silicon revision.				

1. Silicon Errata Issues

CAUTION

Notice: This document summarizes all silicon errata issues from all revisions of silicon, previous and current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1 Module: Analog-to-Digital Converter with Computation (ADCC)

1.1.1 Acquisition time cannot be changed through either the ADACQ or the ADPRE registers

ADC acquisition (sample) time cannot be modified by writing to either the ADPRE or ADACQ registers. Writes to the ADPRE or ADACQ registers will correctly delay the next conversion, but will have no affect on increasing the actual sample time of the current conversion. For example, if the ADCRC is used as the clock source, the sample time will be nominally 3.33 µs, regardless of the values in either of the ADACQ or ADPRE registers.

Work around

There's essentially no work around for increasing the sample times via the ADPRE or ADACQ registers however there are various work-arounds and/or techniques that can be implemented to acquire a more accurate ADC measurement.

- If the ADC is using the F_{OSC}, reducing the clock speed at the time of measurement will increase the overall sampling time
  - Use the NOSC/NDIV bits of OSCCON1 to reduce the oscillator speed
  - Adjust the ADCLK divider value to reduce the oscillator speed.
  - Switch the ADC clock to the ADCRC
- The source input impedance (R_S) directly effects the amount of time it takes to charge the C_{HOLD} capacitor. Reducing the input impedance to a minimum will help reduce the sample time needed for the ADC measurement.

Affected Silicon Revisions

B0							
X							

1.1.2 RA2 Is Not Working As V_{REF}- In Single-Ended Mode

V_{REF}- cannot be connected externally to the V_{REF}- pin (RA2) in Single-Ended Mode (IC = 0). V_{REF}- can only be connected to the external V_{REF}- pin in Differential Mode (IC = 1)

Work around

No workaround available for Single-Ended Mode.

Affected Silicon Revisions

B0							
X							

1.2 Module: Digital-to-Analog Converter (DAC)

1.2.1 Mid-ban voltage spike at code 128 may occur when $\overline{\text{DACAUTOEN}}$ is enabled and the application is incrementing the DACxDATL register from 127 to 129

When the $\overline{\text{DACAUTOEN}}$ bit is enabled, a voltage glitch on the DACxOUT pin may occur at code 128 when the application is incrementing the DACxDATL register from 127 to 129 and the alternate DACxOUT pin is either tied to GND or V_{DD}. If the alternate pin is tied to V_{DD}, the glitch with be positive; if the pin is tied to GND, the glitch will be negative.

Work around
None.

Affected Silicon Revisions

B0							
X							

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40002484**A**):

Note:
Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1 None

There are no known data sheet clarifications as of this publication date.

3. Appendix A: Revision History

Doc Rev.	Date	Comments
A	3/2023	Initial release of this document. Includes silicon 1.1.1 and 1.1.2 (Analog-to-Digital Converter with Computation) and 1.2.1 (Digital-to-Analog Converter).

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