Product Change Notification / SYST-15UJOP885

Date:

16-Mar-2023

Product Category:

32-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ERRATA - PIC32CM MC00 Family Silicon Errata and Data Sheet Clarifications

Affected CPNs:

SYST-15UJOP885_Affected_CPN_03162023.pdf
SYST-15UJOP885_Affected_CPN_03162023.csv

Notification Text:

SYST-15UJOP885

Microchip has released a new Errata for the PIC32CM MC00 Family Silicon Errata and Data Sheet Clarifications of devices. If you are using one of these devices please read the document located at PIC32CM MC00 Family Silicon Errata and Data Sheet Clarifications.

Notification Status: Final

Description of Change:
This revision contains numerous typographical updates throughout the document along with the updates listed here. Obsolete Data Sheet Clarifications were removed for this revision.

• The following Errata were added in this revision:
– SERCOM USART: 1.6.1 LIN Host Delays
– SERCOM USART: 1.6.2 Two stop bits mode in LIN Host
– OSC48M: 1.7.1 Start-Up

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity
Change Implementation Status: Complete

Date Document Changes Effective: 16 Mar 2023

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices::N/A

Attachments:

PIC32CM MC00 Family Silicon Errata and Data Sheet Clarifications

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Affected Catalog Part Numbers (CPN)

PIC32CM1216MC00032-E/RTB
PIC32CM6408MC00032-E/RTB
PIC32CM1216MC00032-E/PT
PIC32CM6408MC00032-E/PT
PIC32CM1216MC00048-E/U5B
PIC32CM6408MC00048-E/U5B
PIC32CM1216MC00048-E/Y8X
PIC32CM6408MC00048-E/Y8X
PIC32CM1216MC00032-I/RTB
PIC32CM6408MC00032-I/RTB
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PIC32CM6408MC00032-I/PT
PIC32CM1216MC00048-I/U5B
PIC32CM1216MC00048-I/U5BESU
PIC32CM6408MC00048-I/U5B
PIC32CM1216MC00048-I/Y8X
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PIC32CM1216MC00032T-I/RTB
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PIC32CM6408MC00048T-E/Y8X

PIC32CM MC00 Family Silicon Errata and Data Sheet Clarifications

PIC32CM MC00 Family Errata

The PIC32CM MC00 family of devices that you have received conforms functionally to the current Device Data Sheet (DS60001638), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the following table.

The errata described in this document will be addressed in future revisions of the PIC32CM MC00 family of devices.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Data Sheet clarifications and corrections (if applicable) are located in Data Sheet Clarifications, following the discussion of silicon issues.

Table 1. PIC32CM MC00 Family Silicon Device Identification

Devices	Device ID (DID[31:0])	Silicon Revision ID (DID.REVISION[3:0])	
		A1	A2
PIC32CM1216MC00032	0x11070x00	0x0	0x1
PIC32CM6408MC00032	0x11070x01	0x0	0x1
PIC32CM1216MC00048	0x11070x06	0x0	0x1
PIC32CM6408MC00048	0x11070x07	0x0	0x1

Note:

1. Refer to the *"Device Service Unit"* chapter in the current Device Data Sheet (DS60001638) for a detailed information on Device Identification and Revision IDs for a specific device.

Silicon Errata Summary

Module	Feature	Errata Number	Issue Summary	Affected Revisions	
				A1	A2
NVMCTRL	DATA FLASH	1.1.1	CPU writes to any memory or register while a write or erase operation is ongoing in the Data Flash address space will stall the AHB bus for the duration of the write or erase operation. CPU reads are not impacted.	X	
NVMCTRL	CEHL	1.1.2	The CEHL feature is not functional.	X	
SERCOM I2C	Repeated Start	1.2.1	For Host Write operations (excluding High-Speed mode) in 10-bit addressing mode, writing CTRLB.CMD = 0x1 does not correctly issue a Repeated Start command.	X	X
SERCOM I2C	Repeated Start	1.2.2	For High-Speed Host Write operations, writing CTRLB.CMD = 0x1 issues a STOP command instead of a Repeated Start, making repeated start not possible in that mode.	X	X
SERCOM I2C	NACK and Repeated Start	1.2.3	For High-Speed Host Read operations, sending a NACK (CTRLB.CMD = 0x2) forces a STOP to be issued, making repeated start not possible in that mode.	X	X
SERCOM I2C	RXNACK	1.2.4	The RXNACK status bit is invalid during the first DRDY interrupt.	X	X
OSCCTRL	FDPLL Unlock	1.3.1	Spurious DPLL unlocks may be detected during operation.	X	X
OSCCTRL	FDPLL ONDEMAND	1.3.2	The FDPLL96M On Demand mode (DPLLCTRLA.ONDEMAND = 1) is not functional in Standby Sleep mode.	X	X
AC	INTREF	1.4.1	For AC reference voltage do not use the INTREF.	X	X
PDEC	STATUS	1.5.1	When the INTFLAG.ERR is rising the associated STATUS.xERR is set after a delay.	X	X
PDEC	STATUS	1.5.2	When the INTFLAG.DIR is rising the associated STATUS.DIR is set after a delay.	X	X
PDEC	HALL MODE	1.5.3	In Hall mode, a spurious WINERR can be reported at start command or when leaving standby.	X	X
PDEC	HALL MODE	1.5.4	In Hall mode, when rotation is very slow or stopped then several WINERR interrupts can occur.	X	X
SERCOM USART	LIN Host Delays	1.6.1	In SERCOM USART LIN Host mode, when break, sync, and identifier fields are automatically transmitted when data is written with the identifier, the LIN Host Header Delay between the sync and the ID transmission fields is not correct.	X	X
SERCOM USART	Two stop bits mode in LIN Host	1.6.2	Two stop bits mode is not supported in SERCOM USART LIN Host mode when break, sync, and identifier fields are automatically transmitted when data is written with the identifier.	X	X
OSC48M	Start-Up	1.7.1	In some very rare cases, the OSC48M internal oscillator may not start at power-up or may not re-start during runtime after having been turned off manually or automatically by the system.	X	X

Table of Contents

1. PIC32CM MC00 Errata Issues

The following issues apply to the PIC32CM MC00 family of devices.

1.1 Non-Volatile Memory Controller (NVMCTRL)

1.1.1 DATA FLASH

CPU writes to any memory or register while a write or erase operation is ongoing in the Data Flash address space will stall the AHB bus for the duration of the write or erase operation. CPU reads are not impacted.

The stall duration will be up to the maximum time of the Flash write or erase operation:

Page Write time: 2.5 ms

Row Erase time: 6 ms

Sector Erase time: 8 ms

Workaround

Perform Data Flash modify operations in a safe region of the application where CPU writes are not required.

Affected Silicon Revisions

A1	A2			
X				

1.1.2 CEHL

The Chip Erase Hard Lock (CEHL) feature is not functional and will not provide any code protection capabilities. The Secure Bit (SB) is not affected and can be used for code protection.

Workaround

None.

Affected Silicon Revisions

A1	A2			
X				

1.2 SERCOM I^2C

1.2.1 Repeated Start

For Host Write operations (excluding High-Speed mode) in 10-bit Addressing mode, writing CTRLB.CMD = 0x1 does not correctly issue a Repeated Start command.

Workaround

Write the same 10-bit address with the same direction bit to the ADDR.ADDR register to generate a Repeated Start.

Affected Silicon Revisions

A1	A2			
X	X			

1.2.2 Repeated Start

For High-Speed Host Write operations, writing CTRLB.CMD = 0x1 issues a STOP command instead of a Repeated Start, making repeated start not possible in that mode.

Workaround
None.

Affected Silicon Revisions

A1	A2			
X	X			

1.2.3 NACK and Repeated Start

For High-Speed Host Read operations, sending a NACK (CTRLB.CMD = 0x2) forces a STOP to be issued, making repeated start not possible in that mode.

Workaround
None.

Affected Silicon Revisions

A1	A2			
X	X			

1.2.4 RXNACK

The RXNACK status bit is invalid during the first DRDY interrupt.

Workaround
Use a software flag to track when to ignore RXNACK and reset this flag in the I2CS_AMATCH interrupt handler (workaround not applicable when AACKEN = 1).

Affected Silicon Revisions

A1	A2			
X	X			

1.3 OSCCTRL

1.3.1 FDPLL Unlock

When using FDPLL at temperatures below 25°C, spurious DPLL unlocks (OSCCTRL.DPLLSTATUS.LOCK = 0) may be detected while the FDPLL still adheres to the electrical characteristics metrics defined in section 43.16 of the data sheet. During these unlock periods, the DPLL output clock is halted and then restarts.

Workaround
When using FDPLL at temperatures below 25°C, enable the lock bypass (OSCCTRL.DPLLCTRLB.LBYPASS = 1) to avoid losing FDPLL clock output during a false unlock status. The workaround does not avoid false unlock indications, but it disables the gating of the FDPLL clock output by the lock status; therefore, the clock is issued even if the FDPLL status shows unlocked.

Pseudo Code

Set OSCCTRL.DPLLCTRLB.LBYPASS = 1

Set DPLLCTRLA.ENABLE = 1

Wait (OSCCTRL.DPLLSTATUS.CLKRDY = 1)

Set Source for GCLK with DPLL

Affected Silicon Revisions

A1	A2			
X	X			

1.3.2 FDPLL ONDEMAND

The FDPLL96M On Demand mode (DPLLCTRLA.ONDEMAND = 1) is not functional in Standby Sleep mode.

Workaround

Set the DPLLCTRLA.ONDEMAND = 0 which makes the FDPLL96M always run in Standby Sleep mode.

Affected Silicon Revisions

A1	A2			
X	X			

1.4 AC

1.4.1 INTREF

When using the AC module, do not use the INTREF (AC.COMPCTRLx.MUXNEG = INTREF) as an internal reference voltage.

Workaround

Use the DAC (AC.COMPCTRLx.MUXNEG = DAC) for the internal reference of the AC module.

Affected Silicon Revisions

A1	A2			
X	X			

1.5 PDEC

1.5.1 STATUS

When the INTFLAG.ERR is rising the associated STATUS.xERR is set after a delay.

Workaround

Poll the STATUS register until the ERR bit is set.

Affected Silicon Revisions

A1	A2			
X	X			

1.5.2 STATUS

When the INTFLAG.DIR is rising the associated STATUS.DIR is set after a delay. It is not recommended to use the INTFLAG.DIR and STATUS.DIR in conjunction with each other.

Workaround
None.

Affected Silicon Revisions

A1	A2			
X	X			

1.5.3 HALL MODE

In Hall mode, a spurious WINERR can be reported at the Start command or when leaving standby.

Workaround
Ignore WINERR in Hall mode at the Start command or when leaving standby.

Affected Silicon Revisions

A1	A2			
X	X			

1.5.4 HALL MODE

In Hall mode, when rotation is very slow or stopped several WINERR interrupts can occur.

Workaround
When a stop or low speed is indicated by the WINERR interrupt, disable the Hall error interrupts until the error condition has disappeared.

Affected Silicon Revisions

A1	A2			
X	X			

1.6 SERCOM USART

1.6.1 LIN Host Delays

In SERCOM USART LIN Host mode (CTRLA.FORM = 0x2), when break, sync, and identifier fields are automatically transmitted when data is written with the identifier (CTRLB.LINCMD = 0x2), the LIN Host Header Delay between the sync and the ID transmission fields is not correct for the following cases:

- CTRLC.HDRDLY = 0x2: Where the delay between sync and ID transmission fields is 8-bit time instead of 4-bit time.
- CTRLC.HDRDLY = 0x3: Where the delay between sync and ID transmission fields is 14-bit time instead of 4-bit time.

Workaround
None.

Affected Silicon Revisions

A1	A2			
X	X			

1.6.2 Two stop bits mode in LIN Host

Two Stop Bits mode (CTRLB.SBMODE = 0x1) is not supported in SERCOM USART LIN Host mode (CTRLA.FORM = 0x2) when break, sync, and identifier fields are automatically transmitted when data is written with the identifier (CTRLB.LINCMD = 0x2). One stop bit is only supported.

Workaround

None.

Affected Silicon Revisions

A1	A2			
X	X			

1.7 OSC48M

1.7.1 Start-Up

In some very rare cases, the OSC48M internal oscillator may not start at power-up or may not re-start during runtime after having been turned off manually or automatically by the system.

Workaround

Failures at power-up can be solved by power cycling the unit.

Failures at runtime can be addressed by keeping the OSC48M always enabled (OSC48MCTRL.ENABLE = 1, OSC48MCTRL.ONDEMAND = 0, OSC48MCTRL.RUNSTDBY = 1).

Affected Silicon Revisions

A1	A2			
X	X			

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001638D):

Note: Corrections in tables, registers, and text are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

There are no data sheet clarifications to report.

3. Appendix A: Revision History

Revision F - 03/2023
This revision contains numerous typographical updates throughout the document along with the updates listed here.

Obsolete Data Sheet Clarifications were removed for this revision.

- The following Errata were added in this revision:
  - SERCOM USART: 1.6.1 LIN Host Delays
  - SERCOM USART: 1.6.2 Two stop bits mode in LIN Host
  - OSC48M: 1.7.1 Start-Up

Revision E - 06/2021
This revision contains numerous typographical updates throughout the document along with the updates listed here.

The I^2C, SPI and I^2S standards use the terminology "Master" and "Slave". The equivalent Microchip terminology used in this document is "Host" and "Client" respectively.

- The following Errata were added in this revision:
  - SERCOM I^2C: 1.2.4 RXNACK
  - PDEC: STATUS 1.5.1
  - PDEC: STATUS 1.5.2
  - PDEC: HALL MODE 1.5.3
  - PDEC: HALL MODE 1.5.4
- The following Data Sheet Clarifications were added:
  - Absolute Maximum Ratings
  - Internal 48MHz RC Oscillator (OSC48M)
  - I/O Pin Electrical Characteristics
  - SERCOM SPI Host/Client

Revision D - 04/2021
This revision contains numerous typographical updates throughout the document along with the updates listed here.

The I^2C, SPI and I^2S standards use the terminology "Master" and "Slave". The equivalent Microchip terminology used in this document is "Host" and "Client" respectively.

- The following Errata were added in this revision:
  - AC: INTREF 1.4.1
  - OSCCTRL: FDPLL ONDEMAND 1.3.2

Revision C - 02/2021
The following update was performed for this revision:

- Added Silicon Issue OSCCTRL FDPLL Unlock 1.3.1

Revision B - 11/2020
The following updates were performed for this revision:

- Updated Silicon Die Revision from A0 to A1
- Updated the errata numbering schema

Revision A - 07/2020
This is the initial released version of this document.

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