Product Change Notification / SYST-08EQTH372

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10-Mar-2023

Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ERRATA - ATtiny212/214/412/414/416 Silicon Errata and Data Sheet Clarification

Affected CPNs:

SYST-08EQTH372_Affected_CPN_03102023.pdf
SYST-08EQTH372_Affected_CPN_03102023.csv

Notification Text:

SYST-08EQTH372

Microchip has released a new Errata for the ATtiny212/214/412/414/416 Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at ATtiny212/214/412/414/416 Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change:• Document:
– Editorial updates

• Silicon Errata Issue added:
– NVMCTRL: 2.6.1. Wrong Reset Value of NVMCTRL.CTRLA Register

• Silicon Errata Issues updated:
– Device: 2.2.2. Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values
– RTC: 2.8.1. Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler
– TWI: 2.12.1. TIMEOUT Bits in the TWI.MCTRLA Register are Not Accessible

• Silicon Errata Issue removed:
– USART: Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode

• Added new data sheet clarification:
– SLPCTRL: 3.1.1. Sleep Mode Activity Overview
– ADC: 3.2.1. VREFA

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 10 Mar 2023

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

ATtiny212/214/412/414/416 Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

ATTINY212-SSF
ATTINY212-SSF
ATTINY212-SSN
ATTINY212-SSN
ATTINY212-SSNR
ATTINY212-SSNR
ATTINY212-SSFR
ATTINY212-SSFR
ATTINY214-SSF
ATTINY214-SSF
ATTINY214-SSN
ATTINY214-SSN
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ATTINY412-SSFR
ATTINY412-SSFR
ATTINY412-SSFRA0
ATTINY416-SF
ATTINY416-SF
ATTINY416-MF
ATTINY416-MF
ATTINY416-SN
ATTINY416-SN
ATTINY416-MN
ATTINY416-MN
ATTINY416-SNR
ATTINY416-SNR
ATTINY416-MNR
ATTINY416-MNRPE
ATTINY416-MNR

ATTINY416-MNRPE
ATTINY416-SFR
ATTINY416-SFR
ATTINY416-MFR
ATTINY416-MFR

ATtiny212/214/412/414/416

ATtiny212/214/412/414/416 Silicon Errata and Data Sheet Clarification

The ATtiny212/214/412/414/416 devices you have received conform functionally to the current device data sheet (www.microchip.com/DS40002287), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the ATtiny212/214/412/414/416 devices.

Notes:

- This document summarizes all the silicon errata issues from all the silicon revisions, previous and current
- Refer to the Device/Revision ID section in the current device data sheet (www.microchip.com/DS40002287) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

1. Silicon Issue Summary

Legend

- **-** Erratum is not applicable.
- **X** Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision		
		Rev. A	Rev. B	Rev. C
Device	2.2.1. The Temperature Sensor is Not Calibrated on Parts with Date Code 727, 728 and 1728 (Year 2017, Week 27/28)	-	X	-
	2.2.2. Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values	X	X	X
AC	2.3.1. AC Interrupt Flag Not Set Unless Interrupt is Enabled	X	-	-
	2.3.2. False Triggers May Occur Under Certain Conditions	X	-	-
ADC	2.4.1. One Extra Measurement Performed After Disabling ADC Free-Running Mode	X	X	X
	2.4.2. Changing ADC Control Bits During Free-Running Mode not Working	X	-	-
	2.4.3. ADC Wake-Up with WCMP	X	-	-
	2.4.4. SAMPDLY and ASDV Does Not Work Together With SAMPLEN	X	-	-
	2.4.5. ADC Functionality Cannot be Ensured with CLKADC Above 1.5 MHz and a Setting of 25% Duty Cycle	X	X	X
	2.4.6. ADC Performance Degrades with CLKADC Above 1.5 MHz and VDD < 2.7V	X	X	X
	2.4.7. ADC Interrupt Flags Cleared When Reading RESH	X	-	-
	2.4.8. Pending Event Stuck When Disabling the ADC	X	X	X
CCL	2.5.1. Connecting LUTs in Linked Mode Requires OUTEN Set to '1'	X	X	X
	2.5.2. D-latch is Not Functional	X	X	X
	2.5.3. The CCL Must be Disabled to Change the Configuration of a Single LUT	X	X	X
NVMCTRL	2.6.1. Wrong Reset Value of NVMCTRL.CTRLA Register	X	X	X
PORTMUX	2.7.1. Selecting Alternative Output Pin for TCA0 Waveform Output 0-2 also Changes Waveform Output 3-5	X	X	X
RTC	2.8.1. Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler	X	X	X
	2.8.2. Disabling the RTC Stops the PIT	X	X	X
TCA	2.9.1. Restart Will Reset Counter Direction in NORMAL and FRQ Mode	X	X	X

.....continued

Peripheral	Short Description	Valid for Silicon Revision		
		Rev. A	Rev. B	Rev. C
TCB	2.10.1. Minimum Event Duration Must Exceed the Selected Clock Period	X	X	X
	2.10.2. The TCB Interrupt Flag is Cleared When Reading CCMPH	X	-	-
	2.10.3. TCB Input Capture Frequency and Pulse-Width Measurement Mode Not Working with Prescaled Clock	X	-	-
	2.10.4. The TCA Restart Command Does Not Force a Restart of TCB	X	X	X
	2.10.5. CCMP and CNT Registers Act as 16-Bit Registers in 8-Bit PWM Mode	X	X	X
TCD	2.11.1. Asynchronous Input Events Not Working When TCD Counter Prescaler is Used	X	X	X
TWI	2.12.1. TIMEOUT Bits in the TWI.MCTRLA Register are Not Accessible	X	-	-
	2.12.2. TWI Smart Mode Gives Extra Clock Pulse	X	-	-
	2.12.3. TWI Host Mode Wrongly Detects the Start Bit as a Stop Bit	X	-	-
	2.12.4. The TWI Host Enable Quick Command is Not Accessible	X	-	-
USART	2.13.1. TXD Pin Override Not Released When Disabling the Transmitter	X	X	X
	2.13.2. Frame Error on a Previous Message May Cause False Start Bit Detection	X	X	X
	2.13.3. Full Range Duty Cycle Not Supported When Validating LIN Sync Field	X	X	X
	2.13.4. Open-Drain Mode Does Not Work When TXD is Configured as Output	X	X	X

2. Silicon Errata Issues

2.1 Errata Details

-	Erratum is not applicable.
X	Erratum is applicable.

2.2 Device

2.2.1 The Temperature Sensor is Not Calibrated on Parts with Date Code 727, 728 and 1728 (Year 2017, Week 27/28)

The temperature sensor is not calibrated on parts with date code 727/728 (used on QFN packages) and 1728 (used on SOIC packages).

Work Around
If temperature sensor calibration data is required, devices with the affected date code may be returned through the Microchip RMA service. Devices with this date code are no longer shipped by Microchip.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
-	X	-

2.2.2 Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values

Writing the OSCLOCK fuse in FUSE.OSCCFG to '1' prevents the automatic loading of calibration values from the signature row. The device will run with an uncalibrated OSC20M oscillator.

Work Around
Do not use OSCLOCK for locking the oscillator calibration value. The oscillator calibration value can be locked by writing LOCKEN in CLKCTRL.MCLKLOCK to '1' when using the OSC20M oscillator as the Main Clock source.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

2.3 AC - Analog Comparator

2.3.1 AC Interrupt Flag Not Set Unless Interrupt is Enabled

ACn.STATUS.CMP is not set if the ACn.INTCTRL.CMP is not set.

Work Around
Enable ACn.INTCTRL.CMP or use ACn.STATUS.STATE for polling.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	-	-

2.3.2 False Triggers May Occur Under Certain Conditions

False triggers may occur on falling input pin:

- For common-mode voltage below 0.5V
- For common-mode voltage above 0.5V if the slew rate is greater than 1 V/µs

Work Around

None.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	-	-

2.4 ADC - Analog-to-Digital Converter

2.4.1 One Extra Measurement Performed After Disabling ADC Free-Running Mode

The ADC may perform one additional measurement after clearing ADCn.CTRLA.FREERUN.

Work Around

Write ADCn.CTRLA.ENABLE to '0' to stop the Free-Running mode immediately.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

2.4.2 Changing ADC Control Bits During Free-Running Mode not Working

If control signals are changed during Free-Running mode, the new configuration is not properly taken into account in the next measurement. This is valid for the ADC.CTRLB, ADC.CTRLC, ADC.SAMPCTRL registers, and the ADC.MUXPOS, ADC.WINLT, and ADC.WINHT registers.

Work Around

Disable ADC Free-Running mode before updating the ADC.CTRLB, ADC.CTRLC, ADC.SAMPCTRL, ADC.MUXPOS, ADC.WINLT, or ADC.WINHT registers.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	-	-

2.4.3 ADC Wake-Up with WCMP

When waking up from Standby sleep mode with ADC WCMP interrupt, the ADC is disabled for a few cycles before the device enters Active mode. A new INITDLY is required before the next conversion.

Work Around

Use INITDLY before the next conversion.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	-	-

2.4.4 SAMPDLY and ASDV Does Not Work Together With SAMPLEN

Using SAMPCTRL.SAMPLEN at the same time as CTRLD.SAMPDLY or CTRLD.ASDV will cause an unpredictable sampling length.

Work Around
When setting SAMPCTRL.SAMPLEN greater than `0x0`, the CTRLD.SAMPDLY and CTRLD.ASDV must be cleared.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	-	-

2.4.5 ADC Functionality Cannot be Ensured with CLK_{ADC} Above 1.5 MHz and a Setting of 25% Duty Cycle

The ADC functionality cannot be ensured if CLK_{ADC} > 1.5 MHz with ADCn.CALIB.DUTYCYC set to '`1`'.

Work Around
If ADC is operated with CLK_{ADC} > 1.5 MHz, ADCn.CALIB.DUTYCYC must be set to '`0`' (50% duty cycle).

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

2.4.6 ADC Performance Degrades with CLK_{ADC} Above 1.5 MHz and V_{DD} < 2.7V

The ADC INL performance degrades if CLK_{ADC} > 1.5 MHz and ADCn.CALIB.DUTYCYC set is to '`0`' for V_{DD} < 2.7V.

Work Around
None.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

2.4.7 ADC Interrupt Flags Cleared When Reading RESH

ADCn.INTFLAGS.RESRDY and ADCn.INTFLAGS.WCOMP are cleared when reading ADCn.RESH.

Work Around
In 8-bit mode, read ADCn.RESH to clear the flag or clear the flag directly.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	-	-

2.4.8 Pending Event Stuck When Disabling the ADC

If the ADC is disabled during an event-triggered conversion, the event will not be cleared.

Work Around

Clear ADC.EVCTRL.STARTEI and wait for the conversion to complete before disabling the ADC.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

2.5 CCL - Configurable Custom Logic

2.5.1 Connecting LUTs in Linked Mode Requires OUTEN Set to '1'

Connecting the LUTs in linked mode requires LUTnCTRLA.OUTEN set to '1' for the LUT providing the input source.

Work Around

Use an event channel to link the LUTs, or do not use the corresponding I/O pin for other purposes.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

2.5.2 D-latch is Not Functional

The CCL D-latch is not functional.

Work Around

None.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

2.5.3 The CCL Must be Disabled to Change the Configuration of a Single LUT

To reconfigure a LUT, the CCL peripheral must first be disabled (write ENABLE in CCL.CTRLA to '0'). Writing ENABLE to '0' will disable all the LUTs, and affects the LUTs not under reconfiguration.

Work Around

None.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

2.6 NVMCTRL - Nonvolatile Memory Controller

2.6.1 Wrong Reset Value of NVMCTRL.CTRLA Register

In some cases, the NVMCTRL.CTRLA reset value will not be '0x00'. Even reserved bits can be read as '1' after Reset.

Work Around
Ignore the initial value.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

2.7 PORTMUX - Port Multiplexer

2.7.1 Selecting Alternative Output Pin for TCA0 Waveform Output 0-2 also Changes Waveform Output 3-5

Selecting the alternative output pin for TCA0 in PORTMUX.CTRLC does not work as described when TCA0 operates in split mode.

- Writing PORTMUX.CTRLC bit 0 to '1' will shift the pin position for both WO0 and WO3
- Writing PORTMUX.CTRLC bit 1 to '1' will shift the pin position for both WO1 and WO4
- Writing PORTMUX.CTRLC bit 2 to '1'will shift the pin position for both WO2 and WO5

PORTMUX.CTRLC[5:3] are non-functional.

Work Around
None.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

Note: Not applicable to 8-pin devices.

2.8 RTC - Real-Time Counter

2.8.1 Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler

Any write to the RTC.CTRLA register resets the 15-bit prescaler counter. The next count occurs ½ prescaler period after the reset, resulting in a period length of 0.5 to 1.5 times the expected period depending on when the reset occurs.

Work Around
None.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C

X	X	X

2.8.2 Disabling the RTC Stops the PIT

Writing RTC.CTRLA.RTCEN to '0' will stop the PIT.

Writing RTC.PITCTRLA.PITEN to '0' will stop the RTC.

Work Around

Do not disable the RTC or the PIT if any of the modules are used.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

2.9 TCA - Timer/Counter A

2.9.1 Restart Will Reset Counter Direction in NORMAL and FRQ Mode

When the TCA is configured to the NORMAL or FRQ mode (WGMODE in TCAn.CTRLB is '0x0' or '0x1'), a RESTART command or Restart event will reset the direction to default. The default is counting upwards.

Work Around

None.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

2.10 TCB - Timer/Counter B

2.10.1 Minimum Event Duration Must Exceed the Selected Clock Period

Event detection will fail if TCBn receives an input event with a high/low period shorter than the period of the selected clock source (CLKSEL in TCBn.CTRLA). This applies to the TCB modes (CNTMODE in TCBn.CTRLB) *Time-Out Check* and *Input Capture Frequency and Pulse-Width Measurement*.

Work Around

Ensure that the high/low period of input events is equal to or longer than the selected clock source (CLKSEL in TCBn.CTRLA) period.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

2.10.2 The TCB Interrupt Flag is Cleared When Reading CCMPH

TCBn.INTFLAGS.CAPT is cleared when reading TCBn.CCMPH instead of CCMPL.

Work Around

Read both TCBn.CCMPL and TCBn.CCMPH.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	-	-

2.10.3 TCB Input Capture Frequency and Pulse-Width Measurement Mode Not Working with Prescaled Clock

The TCB Input Capture Frequency and Pulse-Width Measurement mode may lock to Freeze state if CLKSEL in TCB.CTRLA is set to any other value than `0x0`.

Work Around

Only use CLKSEL equal to `0x0` when using Input Capture Frequency and Pulse-Width Measurement mode.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	-	-

2.10.4 The TCA Restart Command Does Not Force a Restart of TCB

The TCA restart command does not force restarting the TCB when TCB is running in SYNCUPD mode. TCB is restarted only after a TCA OVF.

Work Around

None.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

2.10.5 CCMP and CNT Registers Act as 16-Bit Registers in 8-Bit PWM Mode

When the TCB operates in 8-bit PWM mode (CNTMODE in TCBn.CTRLB is '`0x7`'), the low and high bytes for the CCMP and CNT registers act as 16-bit registers for read and write. They cannot be read or written independently.

Work Around

Use 16-bit register access. Refer to the data sheet for further information.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

2.11 TCD - Timer/Counter D

2.11.1 Asynchronous Input Events Not Working When TCD Counter Prescaler is Used

When configuring the TCD to use asynchronous input events (CFG in TCDn.EVCTRLx is '`0x2`') and the TCD Counter Prescaler (CNTPRES in TCDn.CTRLA) is different from '`0x0`' events can be missed.

Work Around
Use the TCD Synchronization Prescaler (SYNCPRES in TCDn.CTRLA) instead of the TCD Counter Prescaler. Alternatively, use synchronous input events (CFG in TCDn.EVCTRLx is not '0x2') if the input events are longer than one CLK_TCD_CNT cycle.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

2.12 TWI - Two-Wire Interface

2.12.1 TIMEOUT Bits in the TWI.MCTRLA Register are Not Accessible

The TIMEOUT bits in the TWI.MCTRLA register are not accessible from the software.

Work Around
When initializing TWI, set BUSSTATE in TWI.MSTATUS to an IDLE state by writing 0x1.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	-	-

2.12.2 TWI Smart Mode Gives Extra Clock Pulse

TWI Host with Smart mode enabled gives an extra clock pulse on the SCL line after sending NACK.

Work Around
None.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	-	-

2.12.3 TWI Host Mode Wrongly Detects the Start Bit as a Stop Bit

If TWI is enabled in Host mode followed by an immediate write to the MADDR register, the bus monitor recognizes the Start bit as a Stop bit.

Work Around
Wait for a minimum of two clock cycles from TWI.MCTRLA.ENABLE until TWI.MADDR is written.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	-	-

2.12.4 The TWI Host Enable Quick Command is Not Accessible

TWI.MCTRLA.QCEN is not accessible from the software.

Work Around
None.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	-	-

2.13 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.13.1 TXD Pin Override Not Released When Disabling the Transmitter

The USART will not release the TXD pin override if:

- The USART transmitter is disabled by writing the TXEN bit in USART.CTRLB to '0' while the USART receiver is disabled (RXEN in USART.CTRLB is '0')
- Both the USART transmitter and receiver are disabled at the same time by writing the TXEN and RXEN bits in USART.CTRLB to '0'

Work Around

There are two possible work arounds:

- Make sure the receiver is enabled (RXEN in USART.CTRLB is '1') while disabling the transmitter (writing TXEN in USART.CTRLB to '0')
- Writing to any register in the USART after disabling the transmitter will start the USART for long enough to release the pin override of the TXD pin

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

2.13.2 Frame Error on a Previous Message May Cause False Start Bit Detection

A false start bit detection will trigger if receiving a frame with RXDATAH.FERR set and reading the RXDATAL before the RxD line goes high.

Work Around

Wait for the RXD pin to go high before reading RXDATA by, for instance, polling the bit in PORTn.IN where the RXD pin is located.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

2.13.3 Full Range Duty Cycle Not Supported When Validating LIN Sync Field

For the LIN sync field, the USART validates each bit to be within ±15% instead of the time between falling edges as described in the LIN specification, which allows a minimum duty cycle of 43.5% and a maximum duty cycle of 57.5%.

Work Around

None.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

2.13.4 Open-Drain Mode Does Not Work When TXD is Configured as Output

When the USART TXD pin is configured as an output, it can drive the pin high regardless of whether the Open-Drain mode is enabled or not.

Work Around

Configure the TXD pin as an input by writing the corresponding bit in PORTx.DIR to '0' when using Open-Drain mode.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

3. Data Sheet Clarifications

Note the following typographic corrections and clarifications for the latest version of the device data sheet (www.microchip.com/DS40002287).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 Sleep Controller (SLPCTRL)

3.1.1 Sleep Mode Activity Overview

A clarification has been made to Table 11-3 *Sleep Mode Wake-up Sources*. Functional changes are shown in **bold**.

Table 3-1. Sleep Mode Wake-Up Sources

Wake-Up Sources	Active in Sleep Mode		
	Idle	Standby	Power-Down
PORTx Pin interrupt	X	X	X(1)
BOD VLM interrupt	X	X	X
RTC interrupts	X	X(2,3)	X(3)
TWIn Address Match interrupt	X	X	X
USARTn Start-of-Frame interrupt	**-**	**X**	-
TCBn interrupts	X	X(2)	-
ADCn interrupts	X	X(2)	-
ACn interrupts	**X**	**X(4)**	-
All other interrupts	X	-	-

Notes:

1. The I/O pin must be configured according to *Asynchronous Sensing Pin Properties* in the PORT section.
2. For the peripheral to run in Standby sleep mode, the RUNSTDBY bit of the corresponding peripheral must be set.
3. In Standby sleep mode, only the RTC functionality requires the RUNSTDBY bit to be set. In Power-Down sleep mode, only the PIT functionality is available.
4. **When the RUNSTDBY bit is set, the AC will operate without updating its Status register or triggering interrupts. If another peripheral has requested CLK_PER, the AC will use the clock to update the Status register and trigger interrupts.**

3.2 Analog-to-Digital Converter (ADC)

3.2.1 VREFA

Documentation related to an external reference (VREFA) is removed from the ADC sections listed below, as the ATtiny212/214/412/414/416 devices do not have a VREFA pin:

- **Features**
- **Overview**
- **Signal Description**
- **ADC Voltage Reference**
- **REFSEL in ADCn.CTRLC**

The affected ADC sections are listed below, with corrections shown in **bold**:

Features

- 10-Bit Resolution
- 0V to V_{DD} Input Voltage Range
- Multiple Internal ADC Reference Voltages
- ~~**External Reference Input**~~
- Single Conversion Mode
- Interrupt Available on Conversion Complete
- Optional Interrupt on Conversion Results
- Temperature Sensor Input Channel
- Optional Event-Triggered Conversion
- Window Comparator Function for Accurate Monitoring or Defined Thresholds
- Accumulation of up to 64 Samples per Conversion

Overview

The Analog-to-Digital Converter (ADC) peripheral produces 10-bit results. The ADC input can either be internal (e.g., a voltage reference) or external through the analog input pins. The ADC is connected to an analog multiplexer, which allows the selection of multiple single-ended voltage inputs. The single-ended voltage inputs refer to 0V (GND).

The ADC supports sampling in bursts where a configurable number of conversion results are accumulated into a single ADC result (Sample Accumulation). Further, a sample delay can be configured to tune the ADC sampling frequency associated with a single burst. This is to tune the sampling frequency away from any harmonic noise aliased with the ADC sampling frequency (within the burst) from the sampled signal. An automatic sampling delay variation feature can be used to randomize this delay to slightly change the time between samples.

The ADC input signal is fed through a sample-and-hold circuit that ensures that the input voltage to the ADC is held at a constant level during sampling.

The voltage reference can be selected from the internal Voltage Reference (VREF) peripheral or the V_{DD} supply voltage.

~~**The selectable voltage references from the internal Voltage Reference (VREF) peripheral, are V_{DD} supply voltage, or external VREF pin (VREFA).**~~

A window compare feature is available for monitoring the input signal. This feature can be configured to only trigger an interrupt on user-defined thresholds for under, over, inside, or outside a window, with minimum software intervention required.

Signal Description

Pin Name	Type	Description
AIN[n:0]	Analog input	Analog input pin
~~**VREFA**~~	~~**Analog input**~~	~~**External voltage reference pin**~~

ADC Voltage Reference

The reference voltage for the ADC (V_{REF}) controls the conversion range of the ADC. Input voltages that exceed the selected V_{REF} will be converted to the maximum result value of the ADC. For an ideal 10-bit ADC, this value is `0x3FF`.

V_{REF} can be selected by writing the Reference Selection (REFSEL) bits in the Control C (ADCn.CTRLC) register as either V_{DD}~~**, external reference V_{REFA},**~~ or an internal reference from the VREF peripheral. V_{DD} is connected to the ADC through a passive switch.

~~**When using the external reference voltage V_{REFA}, configure ADCnREFSEL[0:2] in the corresponding VREF.CTRLn register to the value that is closest, but above the applied reference voltage. For external references higher than 4.3V, use ADCnREFSEL[0:2] = `0x3`.**~~

The internal reference is generated from an internal band gap reference through an internal amplifier controlled by the Voltage Reference (VREF) peripheral.

REFSEL in ADCn.CTRLC
Bit 5:4 - REFSEL Reference Selection

This bit field selects the voltage reference for ADC.

Value	Name	Description
0x0	INTERNAL	Internal reference
0x1	VDD	V_{DD}
~~**0x2**~~	~~**VREFA**~~	~~**External reference V_{REFA}**~~
Other	-	Reserved

4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc Rev.	Date	Comments
B	03/2023	• Document: – Editorial updates • Silicon Errata Issue added: – NVMCTRL: 2.6.1. Wrong Reset Value of NVMCTRL.CTRLA Register • Silicon Errata Issues updated: – Device: 2.2.2. Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values – RTC: 2.8.1. Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler – TWI: 2.12.1. TIMEOUT Bits in the TWI.MCTRLA Register are Not Accessible • Silicon Errata Issue removed: – USART: Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode • Added new data sheet clarification: – SLPCTRL: 3.1.1. Sleep Mode Activity Overview – ADC: 3.2.1. VREFA
A	12/2020	• Initial document release The content of the document has been restructured from: • ATtiny212/412 Silicon Errata and Data Sheet Clarification • ATtiny214/414/814 Silicon Errata and Data Sheet Clarification • ATtiny416/816 Silicon Errata and Data Sheet Clarification to: • **ATtiny212/214/412/414/416 Silicon Errata and Data Sheet Clarification (this document)** Refer to 4.2. Appendix - Obsolete Revision History for further details. • The following item is referring to changes between the latest revisions of the obsolete documents and this document: – Added *Pending Event Stuck When Disabling the ADC* erratum

4.2 Appendix - Obsolete Revision History

Notes: Due to document structure change from pin organized documents, the following document history is provided as a reference.

- ATtiny212/412 Silicon Errata and Data Sheet Clarification (DS40002114C)
- ATtiny214/414/814 Silicon Errata and Data Sheet Clarification (DS40002115C)
- ATtiny416/816 Silicon Errata and Data Sheet Clarification (DS40002116C)

4.2.1 Obsolete Document DS40002114C

Doc. Rev.	Date	Comments
C	11/2020	• Added die revision C • Added new errata: – Device: *Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values* – ADC: *ADC Interrupt Flags Cleared When Reading RESH* – CCL: *The CCL Must be Disabled to Change the Configuration of a Single LUT* – TCA: *Restart Will Reset Counter Direction in NORMAL and FRQ Mode* – TCB: *CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode* – TCD: *Asynchronous Input Events Not Working When TCD Counter Prescaler is Used* – USART: • *Full Range Duty Cycle Not Supported When Validating LIN Sync Field* • *Open-Drain Mode Does Not Work When TXD is Configured as Output* • *Start-of-Frame Detection Can Unintentionally be Enabled in Active Mode when RXCIF is '0'*
B	10/2019	• Updated document template • The ADC errata, **ADC Functionality Cannot be Ensured with ADCCLK Above 1.5 MHz for All Conditions**, has been split into two separate erratas and rewritten
A	06/2019	Initial document release

4.2.2 Obsolete Document DS40002115C

Doc. Rev.	Date	Comments
C	11/2020	• Added die revision C for ATtiny214 and ATtiny414 • Updated *Affected Silicon Revisions* for *ADC Interrupt Flags Cleared When Reading RESH* • Added new errata: – Device: *Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values* – CCL: *The CCL Must be Disabled to Change the Configuration of a Single LUT* – TCA: *Restart Will Reset Counter Direction in NORMAL and FRQ Mode* – TCB: *CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode* – TCD: *Asynchronous Input Events Not Working When TCD Counter Prescaler is Used* – USART: • *Full Range Duty Cycle Not Supported When Validating LIN Sync Field* • *Open-Drain Mode Does Not Work When TXD is Configured as Output* • *Start-of-Frame Detection Can Unintentionally be Enabled in Active Mode when RXCIF is '0'*
B	10/2019	• Updated document template • The ADC errata, **ADC Functionality Cannot be Ensured with ADCCLK Above 1.5 MHz for All Conditions**, has been split into two separate erratas and rewritten
A	06/2019	Initial document release

4.2.3 Obsolete Document DS40002116C

Doc. Rev.	Date	Comments
C	11/2020	• Added die revision C for ATtiny416 • Updated *Affected Silicon Revisions* for *ADC Interrupt Flags Cleared When Reading RESH* • Added new errata: – Device: *Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values* – CCL: *The CCL Must be Disabled to Change the Configuration of a Single LUT* – TCA: *Restart Will Reset Counter Direction in NORMAL and FRQ Mode* – TCB: *CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode* – TCD: *Asynchronous Input Events Not Working When TCD Counter Prescaler is Used* – USART: • *Full Range Duty Cycle Not Supported When Validating LIN Sync Field* • *Open-Drain Mode Does Not Work When TXD is Configured as Output* • *Start-of-Frame Detection Can Unintentionally be Enabled in Active Mode when RXCIF is '0'*
B	10/2019	• Updated document template • The ADC errata, **ADC Functionality Cannot be Ensured with ADCCLK Above 1.5 MHz for All Conditions**, has been split into two separate erratas and rewritten
A	06/2019	Initial document release

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