Information note

N° 10396AERRA

Dear customer,

With this Infineon Technologies AG information note, we would like to inform you about the following

Errata Advance Information 2023-01 affecting TC3xx Microcontrollers

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Information note

N° 10396AERRA

▶ **Products affected**	Please refer to attached affected product list "INF_10396AERRA_[*customer-no*].pdf"

▶ **Detailed change information**

Subject	Errata Advance Information 2023-01 affecting TC3xx Microcontrollers	
Reason	Functional Problems, Application Hints, Documentation Updates	
Description	**Old**	**New**
	■ Not applicable (initial version)	■ Errata Advance Information TC3xx_Errata_Advance_Info_2023_01_v1_0_10396AERRA

▶ **Product identification**	Not applicable (no change of product)
▶ **Impact of change**	Assessment in Application required!
▶ **Attachments**	INF_10396AERRA_[*customer-no*].pdf affected product list 3_cip1096.pdf TC3xx_Errata_Advance_Info_2023_01 myICP link: https://myicp.infineon.com/sites/microcontrollers%2Daurix_customer_doc/Lists/defaultdoclib/AURIX%20TC3xx/00%20AURIX%20TC3xx%20General/00%20Hardware%20Documentation/04%20Errata%20Sheet/Errata%20Advance%20Information/TC3xx_Errata_Advance_Info_2023_01_v1_0_10396AERRA.pdf **In case you don't have access, please contact your local Sales/ FAE.**
▶ **Intended start of delivery**	Not applicable

If you have any questions, please do not hesitate to contact your local sales office.

Errata Advance Information

Rel. 1.0, 2023-02-17

Device **TC3xx**

Marking/Step **see Table 1**

10396AERRA

Infineon is providing you with product information not previously addressed in the product data sheets or other documentation for the devices listed above. The enclosed information describes device behavior which may affect your current or prior use of the product. As our customers use these products in a number of different applications, Infineon is not in a position to assess the consequences of this device behavior in your specific application(s). Therefore, you should review the enclosed information and evaluate its effect, if any, on your current or prior use of the product in your application(s), including whether there are any safety concerns requiring further action and/or regulatory reporting.

New/updated errata/ApHint text modules - Advance information 2023-01

The following text modules have been compiled and internally reviewed by the Microcontroller Division of Infineon Technologies after the latest TC3xx errata sheet release cycle (2022-11-11) and TC3xx errata advance information 2022-12. They are provided here as advance information, and shall be integrated into the TC3xx errata sheets in the next quarterly release cycle.

Table 1 New/updated TC3xx errata/ApHint text modules - 2023-01

Text module	Short description	Affected devices	Change	Page
CCU_TC.P001	Back-up clock accuracy after trimming - Disregard datasheet footnote	All TC3xx	New	3
GTM_AI.408	(A)TOM-RTL: Missing edge on output signal (A)TOM_OUT when CN0 is reset with force update event	All TC3xx except TC35x, TC33xEXT	Update	3

Table 1 New/updated TC3xx errata/ApHint text modules - 2023-01

Text module	Short description	Affected devices	Change	Page
GTM_AI.421	GTM_AEI: Changing BRIDGE_MODE.MSK_WR_RSP in pipeline mode can lead to violation of pipeline protocol	All TC3xx except TC35x, TC33xEXT	New	5
GTM_AI.H473	SPEC-FIFO: Wrong description of FIFO flush operation	All TC3xx except TC35x, TC33x/32x, TC33xEXT	New	5
GTM_AI.H480	SPEC-TIM: Wrong action description for TPIM mode	All TC3xx except TC35x, TC33xEXT	New	7
GTM_AI.H481	SPEC-TIM: Wrong description for TBCM mode	All TC3xx except TC35x, TC33xEXT	New	10
GTM_AI.487	GTM_AEI: Changing BRIDGE_MODE[2:0] in pipeline mode can lead to violation of pipeline protocol	All TC3xx except TC35x, TC33xEXT	New	12
GTM_AI.488	GTM_AEI: Turning off BRIDGE_MODE.MSK_WR_RSP in asynchronous mode might lead to following transactions being corrupted	All TC3xx except TC35x, TC33xEXT	New	13
GTM_AI.490	TOP: Interrupt lines from DPLL not detected in MCS0	All TC3xx except TC35x, TC33x/32x, TC33xEXT	New	13

Table 1 New/updated TC3xx errata/ApHint text modules - 2023-01

Text module	Short description	Affected devices	Change	Page
GTM_AI.492	DPLL: Wrong value of DPLL_INC_CNT1.INC_CNT1 upon switching to normal mode	All TC3xx except TC35x, TC33x/32x, TC33xEXT	New	14
SCR_TC.016	DUT response to first telegram has incorrect C_START value	All TC3xx	Update	16
SCU_TC.H026	Unexpected alarm ALM0[1] during warm reset	All TC3xx	Update	16

CCU_TC.P001 Back-up clock accuracy after trimming - Disregard datasheet footnote

The following text in the footnote on parameter “Back-up clock accuracy after trimming” in table “Back-up Clock” of the current TC3xx datasheets cannot be met under all operating conditions:

- A short term trimming providing the accuracy required by LIN communication is possible by periodic trimming every 2 ms for temperature and voltage drifts up to temperatures of 125° Celsius

This footnote shall be disregarded.

GTM_AI.408 (A)TOM-RTL: Missing edge on output signal (A)TOM_OUT when CN0 is reset with force update event

Description

The channel is configured in continuous up-counter mode. Then a new period is started with a force update event and reset of CN0 is activated.

Configuration for TOM:

TOM[i]_CH[x]_CTRL.UDMODE=0

TOM[i]_TGC[g]_FUPD_CTRL.FUPD_CTRL[k]=10

TOM[i]_TGC[g]_FUPD_CTRL.RSTCN0_CH[k]=10_B

Configuration for ATOM:

ATOM[i]_CH[x]_CTRL.MODE=10_B (SOMP mode)

ATOM[i]_CH[x]_CTRL.UDMODE=0

ATOM[i]_AGC_FUPD_CTRL.FUPD_CTRL[k]=10_B

ATOM[i]_AGC_FUPD_CTRL.RSTCN0_CH[k]=10_B

Expected behavior:

After the counter (A)TOM[i]_CH[x]_CN0.CN0 has been reset and therefore a new period has to be started and the output signal (A)TOM_OUT has to be set immediately to the SL value (ATOM[i]_CH[x]_CTRL_SOMP.SL, TOM[i]_CH[x]_CTRL.SL), and after the counter reaches (A)TOM[i]_CH[x]_CM1.CM1, an edge on (A)TOM_OUT to the inverted SL value (ATOM[i]_CH[x]_CTRL_SOMP.SL, TOM[i]_CH[x]_CTRL.SL) is expected.

Observed behavior:

An edge on the output signal (A)TOM_OUT to the SL value (ATOM[i]_CH[x]_CTRL_SOMP.SL, TOM[i]_CH[x]_CTRL.SL) at the beginning of the new period does not happen. Instead, the output signal (A)TOM_OUT holds its last value.

A second observation is in case the SL value (ATOM[i]_CH[x]_CTRL_SOMP.SL, TOM[i]_CH[x]_CTRL.SL) changes synchronously together with the force update event, an edge on (A)TOM_OUT to the inverted SL value (ATOM[i]_CH[x]_CTRL_SOMP.SL, TOM[i]_CH[x]_CTRL.SL) when (A)TOM[i]_CH[x]_CN0.CN0 reaches (A)TOM[i]_CH[x]_CM1.CM1 does not happen.

Scope

TOM, ATOM

Effects

Missing edge and false output signal level on (A)TOM_OUT

Workaround

No workaround available.

GTM_AI.421 GTM_AEI: Changing BRIDGE_MODE.MSK_WR_RSP in pipeline mode can lead to violation of pipeline protocol

Description

In pipeline mode, a reconfiguration of the BRIDGE_MODE.MSK_WR_RSP directly after another write transaction can lead to a hang of following write transactions by not setting the AEI_READY.

Note: Please also check on errata GTM_AI.487 and GTM_AI.488.

Scope

GTM_AEI

Effects

Transaction not terminated according to protocol, user might be stuck waiting for AEI_READY to be set.

Workaround

Make sure the transaction preceding the write of BRIDGE_MODE.MSK_WR_RSP is a read transaction.

GTM_AI.H473 SPEC-FIFO: Wrong description of FIFO flush operation

Description

FLUSH bit-field description of register FIFO[i]_CH[x]_CTRL (GTM4.1 spec.: FIFO_585):

The specification describes that the FIFO[i]_CH[x]_FILL_LEVEL.LEVEL, the FIFO[i]_CH[x]_RD_PTR.ADDR, and FIFO[i]_CH[x]_WR_PTR.ADDR will be reset to their initial values.

This is valid for FIFO[i]_CH[x]_FILL_LEVEL.LEVEL but not for FIFO[i]_CH[x]_RD_PTR.ADDR and FIFO[i]_CH[x]_WR_PTR.ADDR, which are set to the value of FIFO[i]_CH[x]_START_ADDR.ADDR on a FIFO flush operation.

Also it should be mentioned in the specification that the status bits EMPTY, FULL, LOW_WM and UP_WM of register FIFO[i]_CH[x]_STATUS are set to EMPTY=1, FULL=0, LOW_WM and UP_WM depending on the values programmed into FIFO[i]_CH[x]_LOWER_WM.ADDR and FIFO[i]_CH[x]_UPPER_WM.ADDR.

UP_WM bit-field description of register FIFO[i]_CH[x]_STATUS (GTM4.1 spec.: FIFO_628):

The condition for the UP_WM bit-field of the register FIFO[i]_CH[x]_STATUS is not correct in case the register for FIFO[i]_CH[x]_UPPER_WM.ADDR is programmed to 0 and afterward a FIFO flush is requested. In this case the bit UP_WM will signal 0 in RTL, but the evaluation due to the specification expects a 1.

To overcome this inconsistency between RTL and the specification, the value 0 for FIFO[i]_CH[x]_UPPER_WM.ADDR has to be excluded in the specification (see Note in the ADDR bit-field description of register FIFO[i]_CH[x]_UPPER_WM, GTM4.1 spec.: FIFO_609), as this value does not make sense from an application point of view.

Prose text in the Overview chapter of FIFO (GTM4.1 spec.: FIFO_836):

It is mentioned that the read and write pointer and also the fill level of the corresponding FIFO channel will be reset.

Here the word reset is used in context with the flush. Typically reset is combined with setting the initial values, but this is not true here. Instead of “reset” another term should be used, for example: “set to previously configured values”.

Following note is missing in the specification:

A FIFO flush operation does not influence the state of the FIFO[i]_CH[x]_IRQ_NOTIFY register.

Scope

FIFO

Effects

- Effect 1: The value of FIFO[i]_CH[x]_RD_PTR.ADDR and FIFO[i]_CH[x]_WR_PTR.ADDR are not set to the initial value as described in the specification.
- Effect 2: False value of FIFO[i]_CH[x]_STATUS.UP_WM after a flush request in case FIFO[i]_CH[x]_UPPER_WM.ADDR is programmed to 0.

Recommendation

Please apply either 1 or 2:

1. Configure FIFO[i]_CH[x]_START_ADDR.ADDR to its initial value before executing the flush operation.
2. Do not configure value 0 for FIFO[i]_CH[x]_UPPER_WM.ADDR.

GTM_AI.H480 SPEC-TIM: Wrong action description for TPIM mode

Description

Note: Register names in the text follow the TC3xx syntax conventions.
Correlation of register names:

- **TC3xx**: TIM[i]_CH[x]_CTRL
- **TC4xx**: CLSi_TIM_CHx_CTRL

In TIM Pulse Integration Mode (TPIM) with External Capture (TIM[i]_CH[x]_CTRL.EXT_CAP_EN = 1), the capture is done only with the external capture signal and not with the rising or falling edge of the TIM input signal.

Therefore in the chapter describing the TPIM mode the action description in the table “Operation depending ...“ (GTM4.1 spec.: TIM_2138) rows 2 and 4 are wrong.

In both rows it is described that if inc_cnt == true, a capture as well as a TIM_NEWVAL_IRQ has to be executed.

But this is not the case and has to be removed. Only the last line in both rows of the table (“inc_cnt = false”) is correct.

The result is the following table for TC3xx:

Table 2 TC3xx - Operation depending on CMU clock, DSL and the input signal value (inc_cnt = false if TIM channel is enabled)

Input signal F_OUTx	Selected CMU clock	External capture	ISL	DSL	Action description
Falling edge	-	0	-	0	inc_cnt = true
Rising edge	-	0	-	0	inc_cnt = false
Rising edge	-	0	-	1	inc_cnt = true
Falling edge	-	0	-	1	inc_cnt = false
-	1	0	-	-	If inc_cnt == true then CNT++
-	-	Rising edge	-	-	Do capture GPRx, CNTS; issue NEWVAL_IRQ; CNT=0
-	0	0	-	-	No

The result is the following table for TC4xx:

Table 3 TC4xx - Operation depending on CMU clock, CLSi_TIM_CHx_CTRL.DSL and the input signal value (inc_cnt = false if cluster i TIM channel x is enabled)

Input signal F_OUT[x:x]	Selected CMU clock	External capture	CLSi_TIM_CHx_CTRL.ISL	CLSi_TIM_CHx_CTRL.DSL	Action description
Falling edge	-	0	-	0	inc_cnt = true
Rising edge	-	0	-	0	inc_cnt = false
Rising edge	-	0	-	1	inc_cnt = true
Falling edge	-	0	-	1	inc_cnt = false

Table 3 TC4xx - Operation depending on CMU clock, CLSi_TIM_CHx_CTRL.DSL and the input signal value (inc_cnt = false if cluster i TIM channel x is enabled) (cont'd)

Input signal F_OUT[x:x]	Selected CMU clock	External capture	CLSi_TIM_CHx_CTRL.ISL	CLSi_TIM_CHx_CTRL.DSL	Action description
-	1	0	-	-	If inc_cnt == true then CLSi_TIM_CHx_CNT++
-	-	Rising edge	-	-	Do capture CLSi_TIM_CHx_GPR0, CLSi_TIM_CHx_GPR1, CLSi_TIM_CHx_CNTS; issue TIM_NEWVAL_IRQ; CLSi_TIM_CHx_CNT=0
-	0	0	-	-	No

Scope

TIM

Effects

Contrary to the description, neither a capture nor an interrupt is triggered by a rising or falling edge of the input signal.

Recommendation

Consider the information in the corresponding table above.

GTM_AI.H481 SPEC-TIM: Wrong description for TBCM mode

Description

Note: Register names in the text follow the TC3xx syntax conventions.
Correlation of register names:

- **TC3xx**: TIM[i]_CH[x]_CTRL
- **TC2xx**: TIMi_CHx_CTRL
- **TC4xx**: CLSi_TIM_CHx_CTRL

In TIM Bit Compression Mode with External Capture (TIM[i]_CH[x]_CTRL.EXT_CAP_EN=1), the capture is done only with the external capture signal without dependency to the input signal level. Therefore the bit-field TIM[i]_CH[x]_CTRL.ISL must be set to 1. The value 0 for TIM[i]_CH[x]_CTRL.ISL is prohibited. The bit-field TIM[i]_CH[x]_CTRL.DSL is not relevant.

The following parts in section “External capture Bit Compression Mode (TBCM)” in the TBCM chapter have to be adapted as follows:

- In the prose text
  - “If external capture is enabled, capturing is done for TIM[i]_CH[x]_CTRL.ISL=1 as defined in the next table. The value 0 for TIM[i]_CH[x]_CTRL.ISL is prohibited.”
- In the table
  - In the action description of row 1 the part “TIM[i]_CH[x]_CNT++” has to be removed
  - All rows starting with row 3 have to be replaced with only one row where the content for the column of TIM[i]_CH[x]_CTRL.ISL has to be filled with “0 - prohibited”. All other columns in row 3 have to be marked with “-” (don't care)

The result is the following table for TC3xx and TC2xx:

Table 4 TC3xx - Capturing depended on the DSL, ISL and the input signal value, if external capture is enabled TC2xx - TIM Input Event Mode

Input signal F_OUTx	External capture	ISL	DSL	Action description
-	Rising edge	1	-	do capture; issue NEWVAL_IRQ
-	0	1	-	No
-	-	0 - prohibited	-	-

The result is the following table for TC4xx:

Table 5 TC4xx - Capturing depended on the CLSi_TIM_CHx_CTRL (i=0;x=0-7).DSL, CLSi_TIM_CHx_CTRL (i=0;x=0-7).ISL and the input signal value, if external capture is enabled

Input signal F_OUT[x:x]	External capture	CLSi_TIM_CHx_CTRL.ISL	CLSi_TIM_CHx_CTRL.DSL	Action description
-	Rising edge	1	-	do capture; issue TIM_NEWVAL_IRQ
-	0	1	-	No
-	-	0 - prohibited	-	-

Scope

TIM

Effects

The input signal level defined by TIM[i]_CH[x]_CTRL.DSL with TIM[i]_CH[x]_CTRL.ISL = 0 is not taken into account.

Recommendation

Consider the information given above. Do not configure TIM[i]_CH[x]_CTRL.ISL to 0.

GTM_AI.487 GTM_AEI: Changing BRIDGE_MODE[2:0] in pipeline mode can lead to violation of pipeline protocol

Description

The issue from erratum GTM_AI.421 (“GTM_AEI: Changing BRIDGE_MODE.MSK_WR_RSP in pipeline mode can lead to violation of pipeline protocol”) not only appears when BRIDGE_MODE.MSK_WR_RSP changes, but also when it stays '1' while the other configuration bit fields in BRIDGE_MODE.BYPASS_SYNC and/or BRIDGE_MODE.BRG_MODE change.

Please also check on erratum GTM_AI.488

Scope

GTM_AEI

Effects

Transaction not terminated according to protocol, user might be stuck waiting for AEI_READY to be set.

Workaround

Make sure the transaction preceding the write of the mentioned BRIDGE_MODE bit fields is a read transaction.

This workaround matches the workaround from GTM_AI.421.

GTM_AI.488 GTM_AEI: Turning off BRIDGE_MODE.MSK_WR_RSP in asynchronous mode might lead to following transactions being corrupted

Description

If the AEI bridge operates in asynchronous mode and in pipelined protocol, with Mask-Write-Response turned on (BRIDGE_MODE[2:0]==011_B) and the BRIDGE_MODE.MSK_WR_RSP is turned off (by writing BRIDGE_MODE[2:0]=001_B), the following transaction might be corrupted by the AEI_READY not being set.

This is an issue like in GTM_AI.421 and GTM_AI.487 but a different workaround is needed.

Scope

GTM_AEI

Effects

Transaction not terminated according to protocol, user might be stuck waiting for AEI_READY to be set.

Workaround

Change BRIDGE_MODE.MSK_WR_RSP together with setting the software reset (pipeline writing BRIDGE_MODE[16:0]=10001_H).

GTM_AI.490 TOP: Interrupt lines from DPLL not detected in MCS0

Description

Some of the DPLL interrupt lines can be detected in the internal registers DSTA and DSTAX of MCS0.

If the clock divider of cluster 0 is configured to 10_B (2:1 clock ratio) inside GTM_CLS_CLK_CFG.CLS0_CLK_CFG and DPLL_IRQ_MODE.IRQ_MODE is configured to 01_B, 10_B, or 11_B, the interrupt pulse cannot be detected inside MCS0 due to a connectivity failure on GTM_IP toplevel and gets lost.

Scope

MCS, DPLL, TOP

Effects

Interrupt from DPLL cannot be detected in MCS0.

Workaround 1

Use interrupt level mode in DPLL by setting of DPLL_IRQ_MODE.IRQ_MODE = 00_B.

Workaround 2

Configure the cluster clock divider of cluster 0 to 1 by setting of GTM_CLS_CLK_CFG.CLS0_CLK_CFG = 01_B.

GTM_AI.492 DPLL: Wrong value of DPLL_INC_CNT1.INC_CNT1 upon switching to normal mode

Description

DPLL_CTRL_0.RMO 1 -> 0:

Upon switching from emergency to normal mode (with DPLL_CTRL_1.SGE1 set to 1), DPLL_INC_CNT1.INC_CNT1 increments by DPLL_MLS1.MLS1 micro ticks every time an active STATE input is encountered till the first active TRIGGER input is encountered. The extra micro ticks accumulated in DPLL_INC_CNT1.INC_CNT1 will only be generated after encountering the first active TRIGGER.

The described behavior is not intended because the STATE input is not supposed to contribute to the pulse generation in normal mode

Scope

DPLL

Effects

1. DPLL_CTRL_0.RMO: 1 -> 0

The generation of the extra micro ticks accumulated in DPLL_INC_CNT1.INC_CNT1 after encountering the first active TRIGGER input ultimately leads to wrong angle clock (manifests in wrong CCM[0]_TBU_TS1) and wrong PMT calculations (due to incorrect DPLL_PSTC.PSTC).

Further effect, which is only applicable to GTM v4.1.0 devices:

The value of PLL_INC_CNT1.INC_CNT1 is not assigned to DPLL_MP_T.MP_T on the first active TRIGGER input (in contrast to what is specified in MP_T description in “DPLL_MP_T” (GTM4.1 specs: DPLL_16159)).

Further observations without malicious effects:

The value of the current position stamp is not assigned to DPLL_PSSM.PSSM at the active STATE input (in contrast to what is specified in “State description of the State Machine Table” step 21 (GTM4.1 spec.: DPLL_6908)). This is, however, insignificant because DPLL_PSSM.PSSM is deemed invalid in normal mode (see PSSM description in “Memory DPLL_PSSM” (GTM4.1 spec.: DPLL_6370)) and therefore should not be used/relied on.

2. DPLL_CTRL_0.RMO: 0 -> 1

Upon switching from normal to emergency mode (with DPLL_CTRL_1.SGE1 set to 1), the value of the current position stamp is not assigned to DPLL_PSTM.PSTM at the active TRIGGER input “State description of the State Machine Table” step 1 (GTM4.1 spec.: DPLL_6908)). This is, however, insignificant because DPLL_PSTM.PSTM is deemed invalid in emergency mode (see PSTM description in “Memory DPLL_PSTM” (GTM4.1 spec.: DPLL_6360)) and therefore should not be used/relied on.

No effect is associated with not assigning the current position stamp to DPLL_PSSM.PSSM in normal mode and DPLL_PSTM.PSTM in emergency mode.

Workaround

Two possible workarounds for DPLL_CTRL_0.RMO: 1 -> 0

1. Defer setting DPLL_CTRL_1.SGE1 to 1 till the first DPLL_TASI interrupt is encountered (signaling the arrival of the first active TRIGGER)

2. Make sure that DPLL_MLS1.MLS1 is set to zero upon switching the mode. The user may then alter it on encountering the first DPLL_TASI interrupt

SCR_TC.016 DUT response to first telegram has incorrect C_START value

Note: This problem is only relevant for tool development, not for application development.

The C_START value returned by the SCR OCDS of the DUT (device under test) in response to a first telegram is wrong.

Each monitor processed command starts with sending a telegram containing the CMD (e.g. READ_BYTE). The response to this telegram should be a telegram containing the C_START value of 0x1.

Instead, the value sent by the DUT is a random value.

Workaround

Do not evaluate the return value of the first telegram from the DUT. Even though the returned C_START is wrong, the returned checksum is correct, and should be checked with the theoretical C_START value of 0x01.

SCU_TC.H026 Unexpected alarm ALM0[1] during warm reset

Description

For any warm reset, the shutdown request handler described in section “Shutdown request handler” in the Firmware chapter of the TC3xx User’s manual requires access to a specific region in the DSPR of CPU0.

For the following configuration

- access to a specific region of CPU0 DSPR (see recommendation below) is disabled for one or all n of the implemented CPUs (CPUx, x = 0..n-1) in registers SPR_SPROT_RGNACCENAi_W and SPR_SPROT_RGNACCENAi_R, which means the access enable bits for the corresponding master TAG IDs are ‘0’

an unexpected alarm ALM0[1] (CPU0 Bus-level MPU violation/Access Protection violation) will occur when an application reset, system reset or warm PORST is requested, and the corresponding flag DF1 in register SMU_AD0 will remain set after the reset if it was a system or application reset.

Recommendation

To avoid these effects, enable read and write access for all available CPUs in the address range 0x70000200 - 0x700003EF in registers SPR_SPROT_RGNACCENAi_W and SPR_SPROT_RGNACCENAi_R.

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Affected products sold to FUTURE ELECTRONICS INC. (4000624)

Sales name	SP number	OPN	Package	Customer part number
SAK-TC367DP-64F300S AA	SP001694656	TC367DP64F300SAAKXUMA1	PG-LFBGA-292-11	
SAK-TC377TP-96F300S AA	SP001694648	TC377TP96F300SAAKXUMA1	PG-LFBGA-292-11	TC377TP96F300SAAKXUMA1
SAK-TC397XA-256F300S BD	SP005351382	TC397XA256F300SBDKXUMA1	PG-LFBGA-292-12	
SAK-TC397XP-256F300S BC	SP002739600	TC397XP256F300SBCKXUMA1	PG-LFBGA-292-10	TC397XP256F300SBCKXUMA1
SAK-TC397XP-256F300S BD	SP005351385	TC397XP256F300SBDKXUMA1	PG-LFBGA-292-10	
SAL-TC364DP-64F300F AA	SP001724134	TC364DP64F300FAALXUMA1	PG-TQFP-144-27	
SAL-TC377TP-96F300S AA	SP001724092	TC377TP96F300SAALXUMA1	PG-LFBGA-292-11	TC377TP96F300SAALXUMA1

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Affected products sold to FUTURE ELECTRONICS INC. (4048203)

Sales name	SP number	OPN	Package	Customer part number
SAK-TC364DP-64F300F AA	SP001713956	TC364DP64F300FAAKXUMA1	PG-TQFP-144-27	TC364DP64F300FAAKXUMA, TC364DP64F300FAAKXUMA1
SAK-TC397XA-256F300S BD	SP005351382	TC397XA256F300SBDKXUMA1	PG-LFBGA-292-12	TC397XA256F300SBDKXUMA1

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Affected products sold to FUTURE ELECTRONICS LTD. (4049887)

Sales name	SP number	OPN	Package	Customer part number
SAK-TC333LP-32F200F AA	SP001724318	TC333LP32F200FAAKXUMA1	PG-TQFP-100-23	
SAK-TC367DP-64F300S AA	SP001694656	TC367DP64F300SAAKXUMA1	PG-LFBGA-292-11	
SAK-TC387QP-160F300S AE	SP005351247	TC387QP160F300SAEKXUMA1	PG-LFBGA-292-11	