



Product Change Notification / SYST-28NGOB303

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02-Mar-2023

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8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ERRATA - ATmega640/1280/1281/2560/2561 Silicon Errata and Data Sheet Clarification

Affected CPNs:

[SYST-28NGOB303_Affected_CPN_03022023.pdf](#)

[SYST-28NGOB303_Affected_CPN_03022023.csv](#)

Notification Text:

SYST-28NGOB303

Microchip has released a new Errata for the ATmega640/1280/1281/2560/2561 Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at [ATmega640/1280/1281/2560/2561 Silicon Errata and Data Sheet Clarification](#).

Notification Status: Final

Description of Change:The initial release of this document

- Errata content moved from the data sheet and restructured to the new document template
- Data sheet clarifications added:
 - Packaging Information: 3.2.1. 100-Ball CBGA
 - System Clock and Clock Options: 3.3.1. System Clock and Clock Options
 - Output Compare Modulator: 3.4.1. Output Compare Modulator in ATmega640/1280/1281/2560/2561
 - Interrupts: 3.5.1. Interrupt Vectors in ATmega640/1280/1281/2560/2561

Impacts to Data Sheet: None

Change Implementation Status: Complete

Date Document Changes Effective:02 Mar 2023

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices:N/A

Attachments:

[ATmega640/1280/1281/2560/2561 Silicon Errata and Data Sheet Clarification](#)

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ATmega640/1280/1281/2560/2561 Silicon Errata and Data Sheet Clarification

Silicon Errata and Data Sheet Clarification

Introduction

The ATmega640/1280/1281/2560/2561 devices you have received conform functionally to the current device data sheet (ww1.microchip.com/downloads/aemDocuments/documents/OTH/ProductDocuments/DataSheets/ATmega640-1280-1281-2560-2561-Datasheet-DS40002211A.pdf), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the ATmega640/1280/1281/2560/2561 devices.

Note:

- This document summarizes all the silicon errata issues from all silicon revisions, previous and current

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Silicon Issue Summary

1. Silicon Issue Summary

- Erratum is not applicable.
- X Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision							
		ATmega640		ATmega1280/1281		ATmega2560/2561			
		Rev. A (1)	Rev. B	Rev. A (1)	Rev. B	Rev. A(1)	Rev. C	Rev. E	Rev. F
Device	2.2.1. Device Does Not Work with VCC Under 2.4V	-	-	-	-	X	-	-	-
Memory	2.3.1. EEPROM Read From Application Code Does Not Work in Lock Bit Mode 3	-	-	-	-	X	-	-	-
	2.3.2. IN/OUT Instructions May Be Executed Twice When Stack Is In External RAM	-	-	-	-	X	-	-	-
Power Management	2.4.1. High Current Consumption In Sleep Mode	X	X	X	X	-	X	-	-
Analog to Digital Converter	2.5.4. Inaccurate ADC Conversion in Differential Mode with 200x Gain	X	X	X	-	-	-	-	-
	2.5.1. Incorrect ADC Reading in Differential Mode	-	-	-	-	X	-	-	-
	2.5.2. Internal ADC Reference Has Too Low Value	-	-	-	-	X	-	-	-
	2.5.3. ADC Differential Input Amplification By 46 dB (200x) is Not Functional	-	-	-	-	-	-	-	X
Boot Loader	2.6.1. Non-Read-While-Write Area of Flash Not Functional	-	-	-	-	X	-	-	-

Note:

1. This revision is the initial release of the silicon.

The following silicon revisions were never released to production:

- ATmega640
 - Rev. C-F
- ATmega1280/1281
 - Rev. C-F
- ATmega2560/2561
 - Rev. B, D

2. Silicon Errata Issues

2.1 Errata Details

- Erratum is not applicable.
- X Erratum is applicable.

2.2 Device

2.2.1 Device Does Not Work with V_{CC} Under 2.4V

The device does not execute code correctly with V_{CC} below 2.4V.

Work Around

Do not use the device at V_{CC} voltages below 2.4V.

Affected Silicon Revisions

ATmega2560/2561			
Rev. A	Rev. C	Rev. E	Rev. F
X	-	-	-

2.3 Memory

2.3.1 EEPROM Read From Application Code Does Not Work in Lock Bit Mode 3

EEPROM read doesn't work from the application code when the memory Lock Bits LB2 and LB1 are programmed to mode 3.

Work Around

Do not set Lock Bit Protection Mode 3 when the application code needs to read from EEPROM.

Affected Silicon Revisions

ATmega2560/2561			
Rev. A	Rev. C	Rev. E	Rev. F
X	-	-	-

2.3.2 IN/OUT Instructions May Be Executed Twice When Stack Is In External RAM

If an IN or an OUT instruction is executed directly before an interrupt occurs, and the stack pointer is located in external RAM, the instruction will be executed twice. In some cases, this will cause a problem, for example:

- If reading SREG, it will appear that the I-flag is cleared
- If writing to the PIN registers, the port will toggle twice
- If reading registers with interrupt flags, the flags will appear to be cleared

Work Around

There are two application workarounds; either one of them will avoid the issue:

- Replace IN and OUT with LD/LDS/LDD and ST/STS/STD instructions
- Use internal RAM for the stack pointer

Affected Silicon Revisions

ATmega2560/2561			
Rev. A	Rev. C	Rev. E	Rev. F
X	-	-	-

2.4 Power Management

2.4.1 High Current Consumption In Sleep Mode

The current consumption will increase during sleep when executing the SLEEP instruction directly after an SEI instruction if a pending interrupt cannot wake the device from the selected sleep mode.

Work Around

Before entering sleep, the interrupts not used to wake the device from sleep mode may be disabled.

Affected Silicon Revisions

ATmega640	
Rev. A	Rev. B
X	X

ATmega1280/1281	
Rev. A	Rev. B
X	X

ATmega2560/2561			
Rev. A	Rev. C	Rev. E	Rev. F
-	X	-	-

2.5 Analog to Digital Converter

2.5.1 Incorrect ADC Reading in Differential Mode

The ADC has high noise in differential mode. It can give up to seven LSBs of error.

Work Around

Use only the seven MSBs of the result when using the ADC in differential mode.

Affected Silicon Revisions

ATmega2560/2561			
Rev. A	Rev. C	Rev. E	Rev. F
X	X	-	-

2.5.2 Internal ADC Reference Has Too Low Value

The internal ADC reference has a value lower than specified.

Work Around

- Use AVCC or external reference
- Measure the actual reference value by applying a known voltage to the ADC when using the internal reference. The result, when doing later conversions, can then be calibrated.

Affected Silicon Revisions

ATmega2560/2561			
Rev. A	Rev. C	Rev. E	Rev. F
X	X	-	-

2.5.3 ADC Differential Input Amplification By 46 dB (200x) is Not Functional

ADC differential input amplification by 46 dB (200x) is not functional.

Work Around

None.

Affected Silicon Revisions

ATmega2560/2561			
Rev. A	Rev. C	Rev. E	Rev. F
-	-	-	X

2.5.4 Inaccurate ADC Conversion in Differential Mode with 200x Gain

With AVCC < 3.6V, random conversions will be inaccurate. The typical absolute accuracy may reach 64 LSBs.

Work Around

Use AVCC ≥ 3.6V.

Affected Silicon Revisions

ATmega640	
Rev. A	Rev. B
X	X

ATmega1280/1281	
Rev. A	Rev. B
X	-

2.6 Boot Loader

2.6.1 Non-Read-While-Write Area of Flash Not Functional

The Non-Read-While-Write area of the Flash is not working as expected. The problem relates to the device speed when reading the Flash in this area.

Work Around

- Only use the first 248 KB of the Flash
- If boot functionality is needed, run the code in the Non-Read-While-Write area at a maximum of 1/4th of the maximum device frequency at any given voltage by writing the CLKPR register before entering the boot section in the code.

Affected Silicon Revisions

ATmega2560/2561			
Rev. A	Rev. C	Rev. E	Rev. F
X	-	-	-

3. Data Sheet Clarifications

Note the following typographic corrections and clarifications for the latest version of the device data sheet (ww1.microchip.com/downloads/aemDocuments/documents/OTH/ProductDocuments/DataSheets/ATmega640-1280-1281-2560-2561-Datasheet-DS40002211A.pdf).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 Errata Section in Data Sheet is no Longer Valid

A clarification for the Errata section in the device data sheet has been made.

The errata content has been moved to a separate document, *ATmega640/1280/1281/2560/2561 Silicon Errata and Data Sheet Clarifications* (this document).

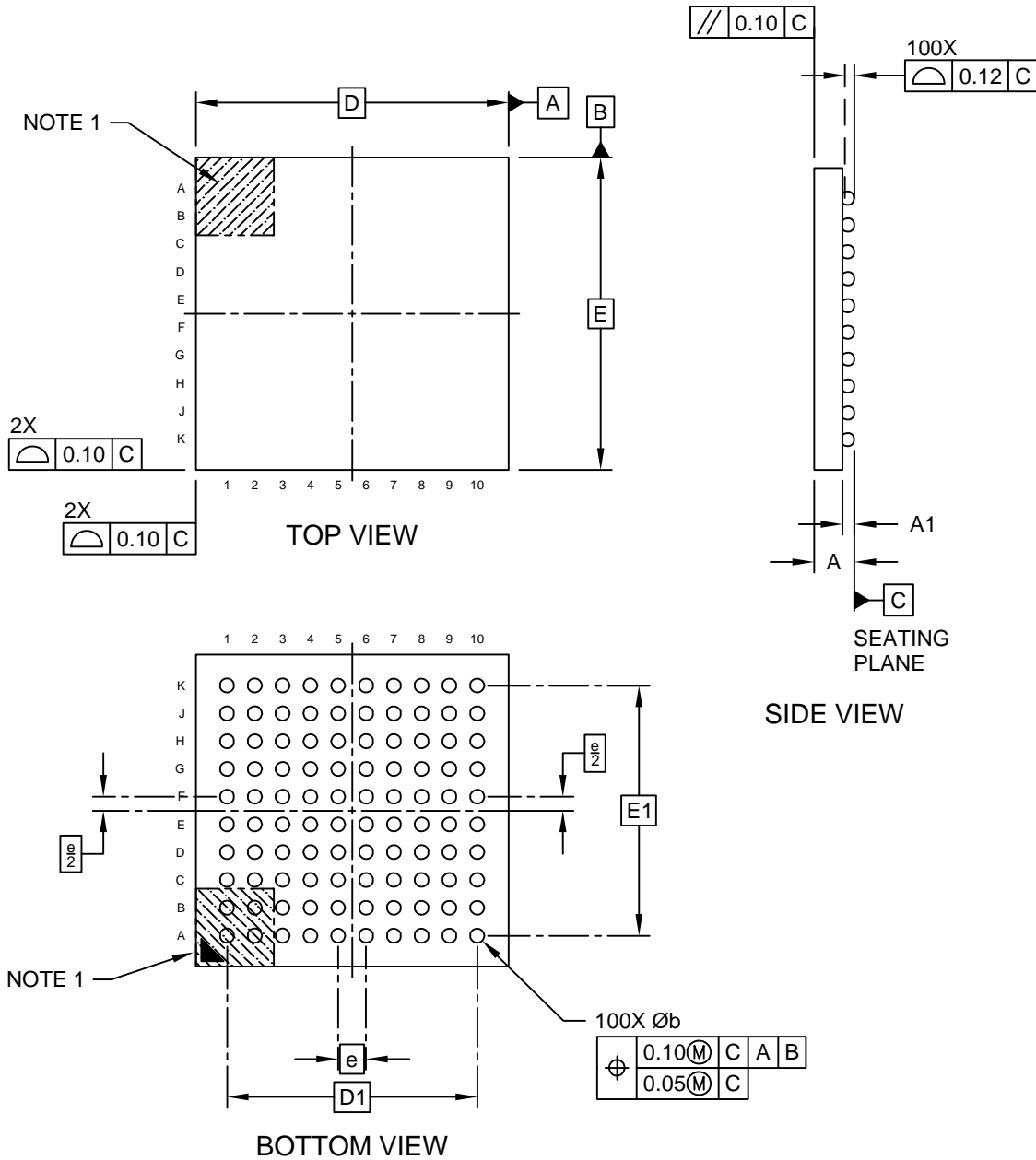
See the *Silicon Errata Issues* section of this document for the latest errata.

3.2 Packaging Information

3.2.1 100-Ball CBGA

100-Ball Ceramic Ball Grid Array Package (A3B) - 9x9 mm Body [CBGA] Atmel Legacy Global Package Code CPR

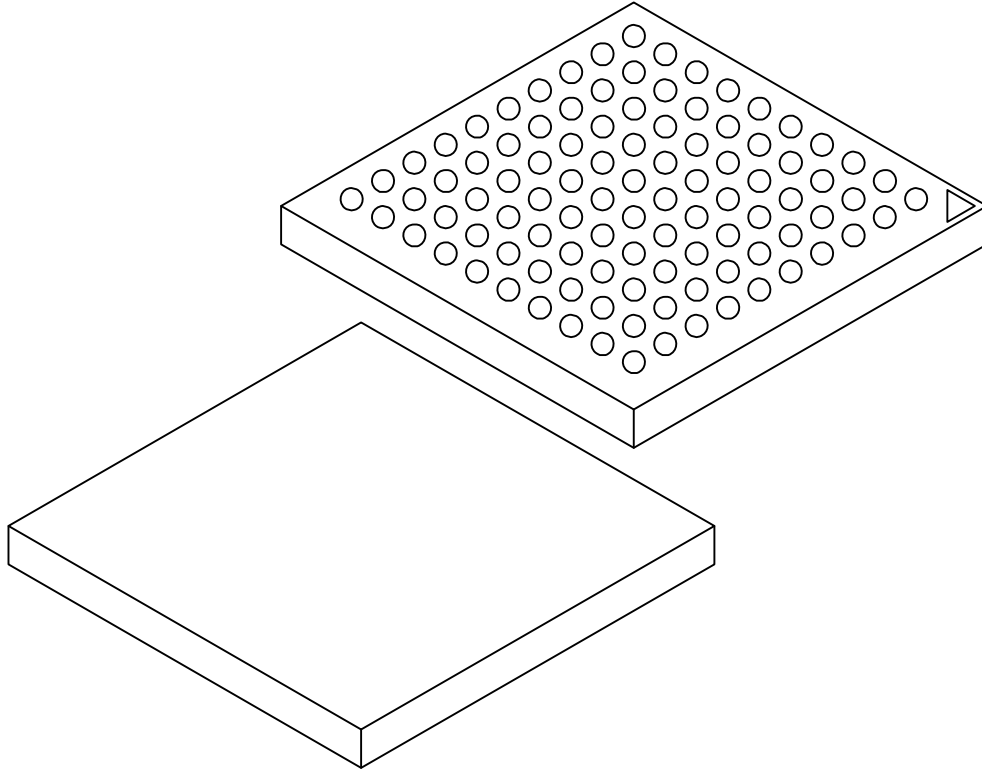
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-21111-A3B Rev A Sheet 1 of 2

100-Ball Ceramic Ball Grid Array Package (A3B) - 9x9 mm Body [CBGA] Atmel Legacy Global Package Code CPR

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	100		
Pitch	e	0.80 BSC		
Overall Height	A	1.10	-	1.20
Ball Height	A1	0.30	0.35	0.40
Overall Length	D	9.00 BSC		
Overall Pitch	D1	7.20 BSC		
Overall Width	E	9.00 BSC		
Overall Pitch	E1	7.20 BSC		
Terminal Diameter	b	0.35	0.40	0.45

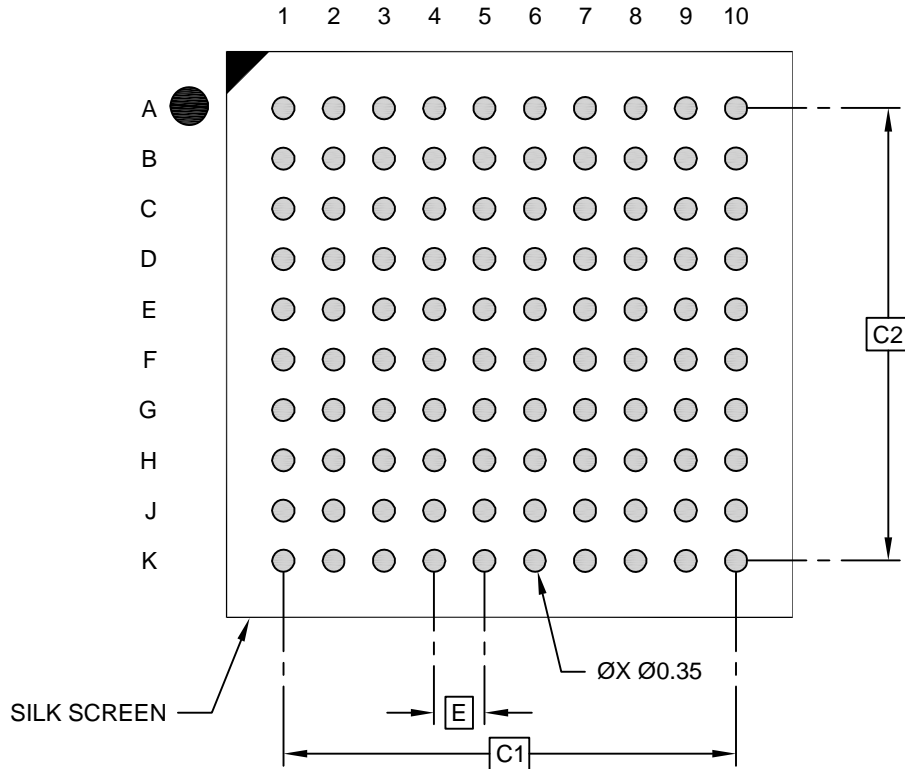
Notes:

1. Terminal A1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21111-A3B Rev A Sheet 2 of 2

100-Ball Ceramic Ball Grid Array Package (A3B) - 9x9 mm Body [CBGA] Atmel Legacy Global Package Code CPR

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.58 BSC		
Overall Pitch	C1	7.20 BSC		
Contact Pad Spacing	C2	7.20 BSC		
Contact Pad Diameter (X100)	X1			0.35

Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23111-A3B Rev A

Table 3-1. Device and Package Maximum Weight

500	mg
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Table 3-2. Package Reference

Package Outline Drawing MCHP reference	C04-2111
JESD97 Classification	E3

3.3 System Clock and Clock Options

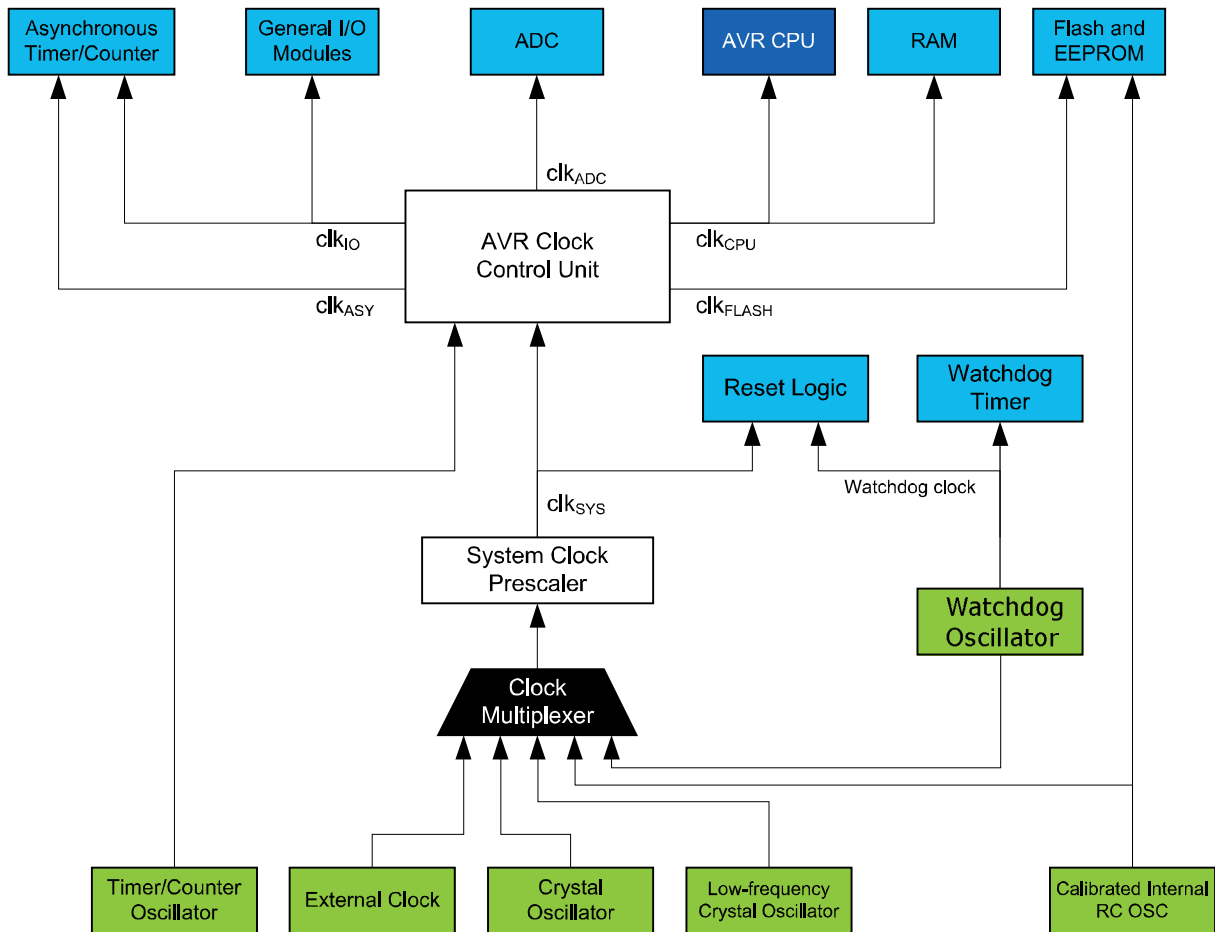
3.3.1 System Clock and Clock Options

A clarification for the “*Clock Systems and Their Distribution*” section has been made.

Figure “*Clock Distribution*” presents the different clock systems in the ATmega640/1280/1281/2560/2561 and their distribution. All of the clocks need not be active at a given time. The clocks to modules not being used can be halted using different sleep modes, as described in the “*Power management and Sleep Modes*” section, to reduce the power consumption.

Figure “*Clock Distribution*” helps select an appropriate sleep mode.

Figure 3-1. Clock Distribution



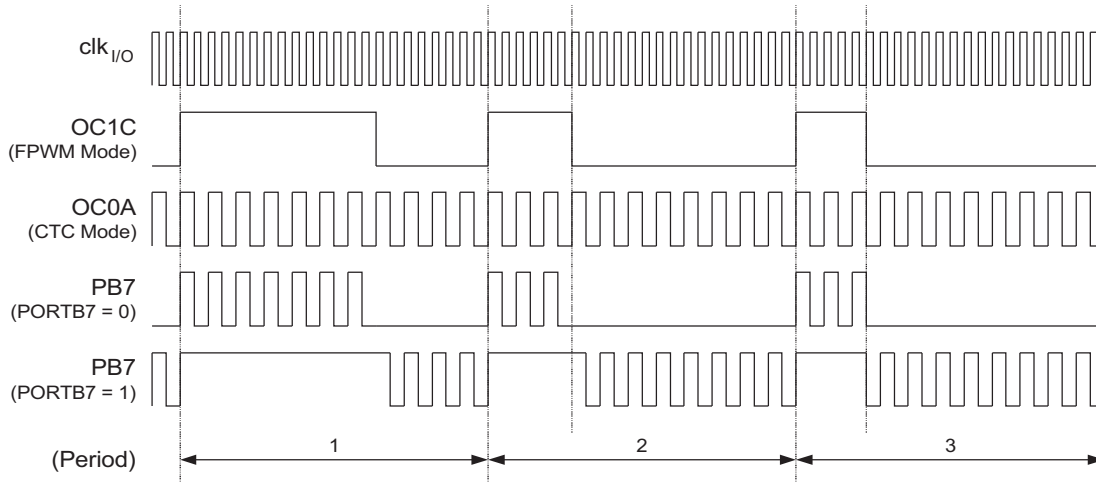
3.4 Output Compare Modulator

3.4.1 Output Compare Modulator in ATmega640/1280/1281/2560/2561

A clarification for the “Timing example in the Output Compare Modulator” has been made.

The following figure illustrates the modulator in action. In this example, the Timer/Counter1 is set to operate in fast PWM mode (non-inverted), and Timer/Counter0 uses CTC waveform mode with toggle Compare Output mode (COMnx1:0 = 1).

Figure 3-2. Output Compare Modulator, Timing Diagram



In this example, **Timer/Counter0** provides the carrier, while the modulating signal is generated by the Output Compare unit C of the Timer/Counter1.

The modulation has reduced the PWM signal (OC1C) resolution. The reduction factor is equal to the number of system clock cycles of one period of the carrier (OC0A). In this example, the resolution is reduced by a factor of two. The figure illustrates the reason for the reduction at the second and third periods of the PB7 output when PORTB7 equals zero. Period 2 high time is one cycle longer than period 3 high time, but the result on the PB7 output is equal in both periods.

3.5 Interrupts

3.5.1 Interrupt Vectors in ATmega640/1280/1281/2560/2561

A clarification for the source names of the Interrupt vectors has been made to comply with the header file naming convention.

Table 3-3. Reset and Interrupt Vectors in ATmega640/1280/1281/2560/2561

Vector No	Program Address ⁽²⁾	Source	Interrupts definition
1	0x0000 ⁽¹⁾	RESET	External pin, Power-on Reset, Brown-out Reset, Watchdog Reset and JTAG AVR Reset.
2	0x0002	INT0	External Interrupt Request 0
3	0x0004	INT1	External Interrupt Request 1
4	0x0006	INT2	External Interrupt Request 2
5	0x0008	INT3	External Interrupt Request 3
6	0x000A	INT4	External Interrupt Request 4

ATmega640/1280/1281/2560/2561 Silic...

Data Sheet Clarifications

.....continued

Vector No	Program Address ⁽²⁾	Source	Interrupts definition
7	0x000C	INT5	External Interrupt Request 5
8	0x000E	INT6	External Interrupt Request 6
8	0x0010	INT7	External Interrupt Request 7
9	0x0012	PCINT0	Pin Change Interrupt Request 0
10	0x0014	PCINT1	Pin Change Interrupt Request 1
11	0x0016 ⁽³⁾	PCINT2	Pin Change Interrupt Request 2
12	0x0018	WDT	Watchdog Time-out Interrupt
13	0x001A	TIMER2_COMPA	Timer/Counter2 Compare Match A
14	0x001C	TIMER2_COMPB	Timer/Counter2 Compare Match B
15	0x001E	TIMER2_OVF	Timer/Counter2 Overflow
16	0x0020	TIMER1_CAPT	Timer/Counter1 Capture Event
17	0x0022	TIMER1_COMPA	Timer/Counter1 Compare Match A
18	0x0024	TIMER1_COMPB	Timer/Counter1 Compare Match B
19	0x0026	TIMER1_COMPC	Timer/Counter1 Compare Match C
20	0x0028	TIMER1_OVF	Timer/Counter1 Overflow
21	0x002A	TIMER0_COMPA	Timer/Counter0 Compare Match A
22	0x002C	TIMER0_COMPB	Timer/Counter0 Compare Match B
23	0x002E	TIMER0_OVF	Timer/Counter0 Overflow
24	0x0030	SPI_STC	SPI Serial Transfer Complete
25	0x0032	USART0_RX	USART0 Receive complete
26	0x0034	USART0_UDRE	USART0 Data Register Empty
27	0x0036	USART0_TX	USART0 Transmit complete
28	0x0038	ANALOG_COMP	Analog Comparator
30	0x003A	ADC	ADC Conversion complete
31	0x003C	EE_READY	EEPROM Ready
32	0x003E	TIMER3_CAPT	Timer/Counter3 Capture Event
33	0x0040	TIMER3_COMPA	Timer/Counter3 Compare Match A
34	0x0042	TIMER3_COMPB	Timer/Counter3 Compare Match B
35	0x0044	TIMER3_COMPC	Timer/Counter3 Compare Match C
36	0x0046	TIMER3_OVF	Timer/Counter3 Overflow
37	0x0048	USART1_RX	USART1 Receive complete
38	0x004A	USART1_UDRE	USART1 Data Register Empty
39	0x004C	USART1_TX	USART1 Transmit complete
40	0x004E	TWI	2-Wire Serial Interface

.....continued

Vector No	Program Address ⁽²⁾	Source	Interrupts definition
41	0x0050	SPM_READY	Store Program Memory Ready
42	0x0052 ⁽³⁾	TIMER4_CAPT	Timer/Counter4 Capture Event
43	0x0054	TIMER4_COMPA	Timer/Counter4 Compare Match A
44	0x0056	TIMER4_COMPB	Timer/Counter4 Compare Match B
45	0x0058	TIMER4_COMPC	Timer/Counter4 Compare Match C
46	0x005A	TIMER4_OVF	Timer/Counter4 Overflow
47	0x005C ⁽³⁾	TIMER5_CAPT	Timer/Counter5 Capture Event
48	0x005E	TIMER5_COMPA	Timer/Counter5 Compare Match A
49	0x0060	TIMER5_COMPB	Timer/Counter5 Compare Match B
50	0x0062	TIMER5_COMPC	Timer/Counter5 Compare Match C
51	0x0064	TIMER5_OVF	Timer/Counter5 Overflow
52	0x0066 ⁽³⁾	USART2_RX	USART2 Receive complete
53	0x0068 ⁽³⁾	USART2_UDRE	USART2 Data Register Empty
54	0x006A ⁽³⁾	USART2_TX	USART2 Transmit complete
55	0x006C ⁽³⁾	USART3_RX	USART3 Receive complete
56	0x006E ⁽³⁾	USART3_UDRE	USART3 Data Register Empty
57	0x0070 ⁽³⁾	USART3_TX	USART3 Transmit complete

Notes:

1. When the BOOTRST fuse is programmed, the device will jump to the boot loader address at Reset. See “*Boot Loader Support – Read-While-Write Self- Programming*”.
2. When setting the IVSEL bit in MCUCR, Interrupt Vectors will be moved to the start of the boot Flash section. The address of each Interrupt Vector will then be the address in this table added to the start address of the boot Flash section.
3. Only available in ATmega640/1280/2560.

4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc Rev.	Date	Comments
B	02/2023	Section "Product Identification System" in the Back Matter is removed
A	02/2023	The initial release of this document <ul style="list-style-type: none"> • Errata content moved from the data sheet and restructured to the new document template • Data sheet clarifications added: <ul style="list-style-type: none"> – Packaging Information: 3.2.1. 100-Ball CBGA – System Clock and Clock Options: 3.3.1. System Clock and Clock Options – Output Compare Modulator: 3.4.1. Output Compare Modulator in ATmega640/1280/1281/2560/2561 – Interrupts: 3.5.1. Interrupt Vectors in ATmega640/1280/1281/2560/2561

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SYST-28NGOB303 - ERRATA - ATmega640/1280/1281/2560/2561 Silicon Errata and Data Sheet Clarification

Affected Catalog Part Numbers(CPN)

ATMEGA1280-16CU
ATMEGA1280V-8CU
ATMEGA640-16CU
ATMEGA640V-8CU
ATMEGA1280-16AU
ATMEGA1280V-8AU
ATMEGA640V-8AU
ATMEGA640-16AU
ATMEGA1280-16AU-HCM
ATMEGA1281V-8MU
ATMEGA1281-16MU
ATMEGA1281-16AU
ATMEGA1281V-8AU
ATMEGA1280-16CUR
ATMEGA1280V-8CUR
ATMEGA640-16CUR
ATMEGA640V-8CUR
ATMEGA1280-16AUR
ATMEGA1280V-8AUR
ATMEGA640V-8AUR
ATMEGA640-16AUR
ATMEGA640-16AURA0
ATMEGA1281-16MUR
ATMEGA1281V-8MUR
ATMEGA1281V-8AUR
ATMEGA1281-16AUR
ATMEGA2560-16CU
ATMEGA2560V-8CU
ATMEGA2560-16AU
ATMEGA2560V-8AU
ATMEGA2560-16AU-HCM
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ATMEGA2561V-8MU
ATMEGA2561-16AU
ATMEGA2561V-8AU
ATMEGA2560-16CUR
ATMEGA2560V-8CUR
ATMEGA2560-16AUR
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ATMEGA2561-16MUR
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