Product/Process Change Notification

N° 2022-233-A

Dear customer,

please find attached our Infineon Technologies AG PCN:

Functional Safety related PCN: Update of safety application note and data sheet affecting product 2ED2410-EM

Important information for your attention:

- Please respond to this PCN by indicating your decision on the approval form, sign it and return to your sales partner before 2023-03-23.
- Infineon aligns with the widely-recognized JEDEC STANDARD "JESD46", which stipulates:
  "Lack of acknowledgement of the PCN within 30 days constitutes acceptance of the change."
  Notwithstanding the aforesaid individual agreements shall prevail.

Your prompt reply will help Infineon to assure a smooth and well-executed transition. If Infineon does not hear from your side by the due date, we will assume your full acceptance to this proposed change and its implementation.

Your attention and response to this matter is greatly appreciated.

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Chairman of the Supervisory Board Dr. Wolfgang Eder
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Registered office Neubiberg Commercial register Amtsgericht München HRB 126492

Product/Process Change Notification

N° 2022-233-A

Products affected	Please refer to attached affected product list PCN_2022-233-A_[customer-no].pdf
Detailed change information	
Subject:	Functional Safety related PCN: Update of safety application note and data sheet affecting product 2ED2410-EM
Reason/Motivation:	Update of FIT rate in safety application note due to correction in calculation. Several updates on data sheet parameters.

Description	**Old**	**New**
ANY: Any change with impact on processability/manufacturability at customer, which is not covered in the matrix below	Safety application note Rev. 2.0	Safety application note Rev. 2.1
DATA SHEET: Change of datasheet parameters/electrical specification (min./max./typ. values) and/or AC/DC specification	Data sheet Rev. 2.00	Data sheet Rev. 2.10

Product identification	not applicable (for documentation only)
Anticipated impact of change	No change of product (neither of technology/package nor of chip design), only change of safety application note and data sheet. Assessment in application required! DeQuMa-ID(s): SEM-AN-02 / SEM-DS-01

Attachments

PCN_2022-233-A_[customer-no].pdf	affected product list
4_cip22233_A	new data sheet Rev. 2.10
safety application note	myICP link Rev. 2.1

Product/Process Change Notification

N° 2022-233-A

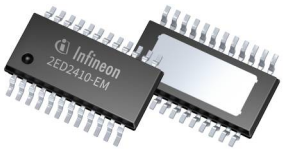
Time schedule

Final qualification report	not applicable, for documentation only
First samples available	not applicable
Intended start of delivery [1]	not applicable, valid with immediate effect
Last order date (LOD) [2]	2023-08-31
Last delivery date (LDD) [3]	2024-02-28

[1] Provided date or earlier after customer approval.
[2] Last date where orders for unchanged products will be accepted.
[3] Last date for delivery of unchanged products. Delivery of changed products can be earlier (see Intended start of delivery) and depends on approval.

If you have any questions, please do not hesitate to contact your local sales office.

12 V/24 V smart analog high-side MOSFET gate driver



RoHS

AEC Qualified

ISO 26262 ready

Features

- PRO-SIL™ ISO 26262-ready for supporting the integrator in evaluation of hardware element according to ISO 26262:2018 Clause 8-13
- One channel device with two high-side gate driver outputs
- 3 Ω pull-down, 50 Ω pull-up for fast switch on/off
- Support back-to-back MOSFET topologies (common drain and common source)
- Two bidirectional high-side analog current sense interfaces with externally adjustable gain
- Adjustable overcurrent/short-circuit protection
- Versatile comparator to implement: adjustable I-t wire protection, overvoltage/undervoltage or overtemperature protection

Potential applications

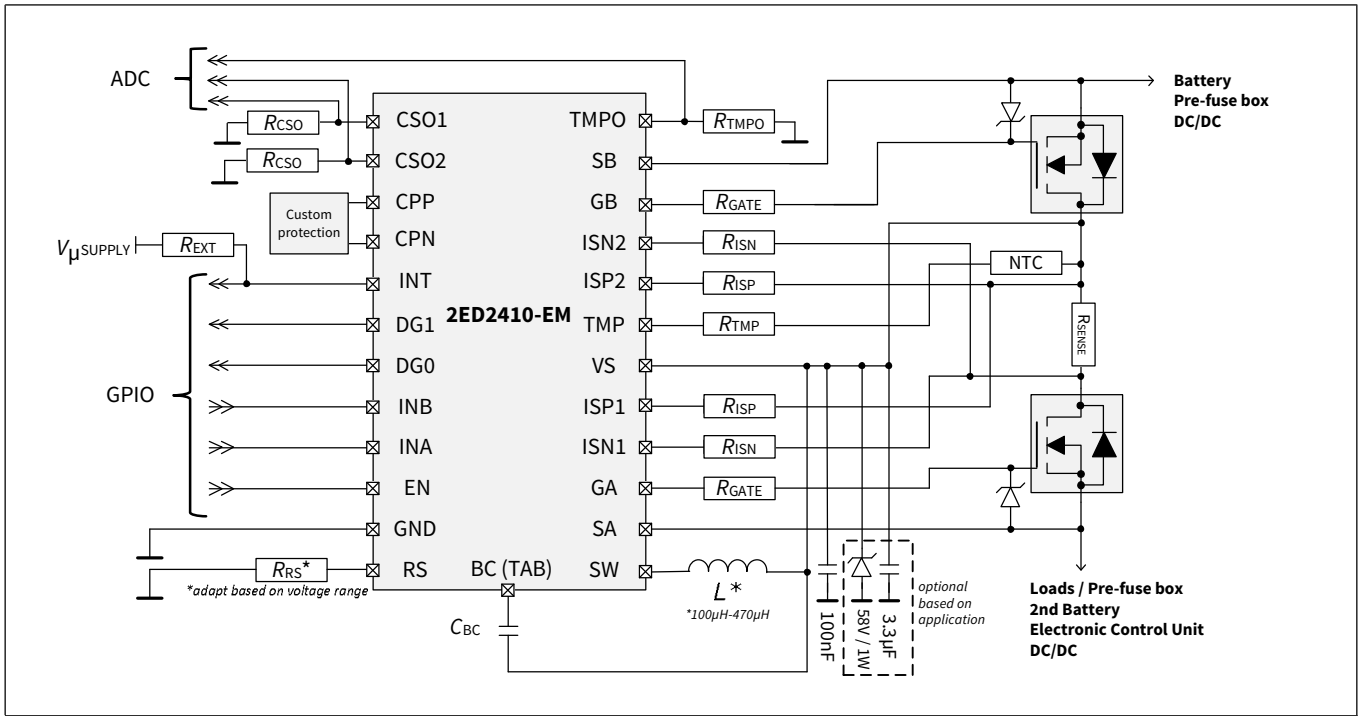
- Fail operational power supply targeting high current applications
- Connection/isolation switch between power supplies (e.g. for hybrids and electric vehicles)
- Developed to support dependable power supply and distribution

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100, Grade 1.

Description

2ED2410-EM is a one channel gate driver with two independent gate outputs for 12 / 24 V automotive applications. It offers several protection features for connecting/disconnecting loads or different power supplies.



Typical application example

Product type	Package	Marking
2ED2410-EM	PG-TSDSO-24	2ED2410-EM

Table of contents

1 Block diagrams

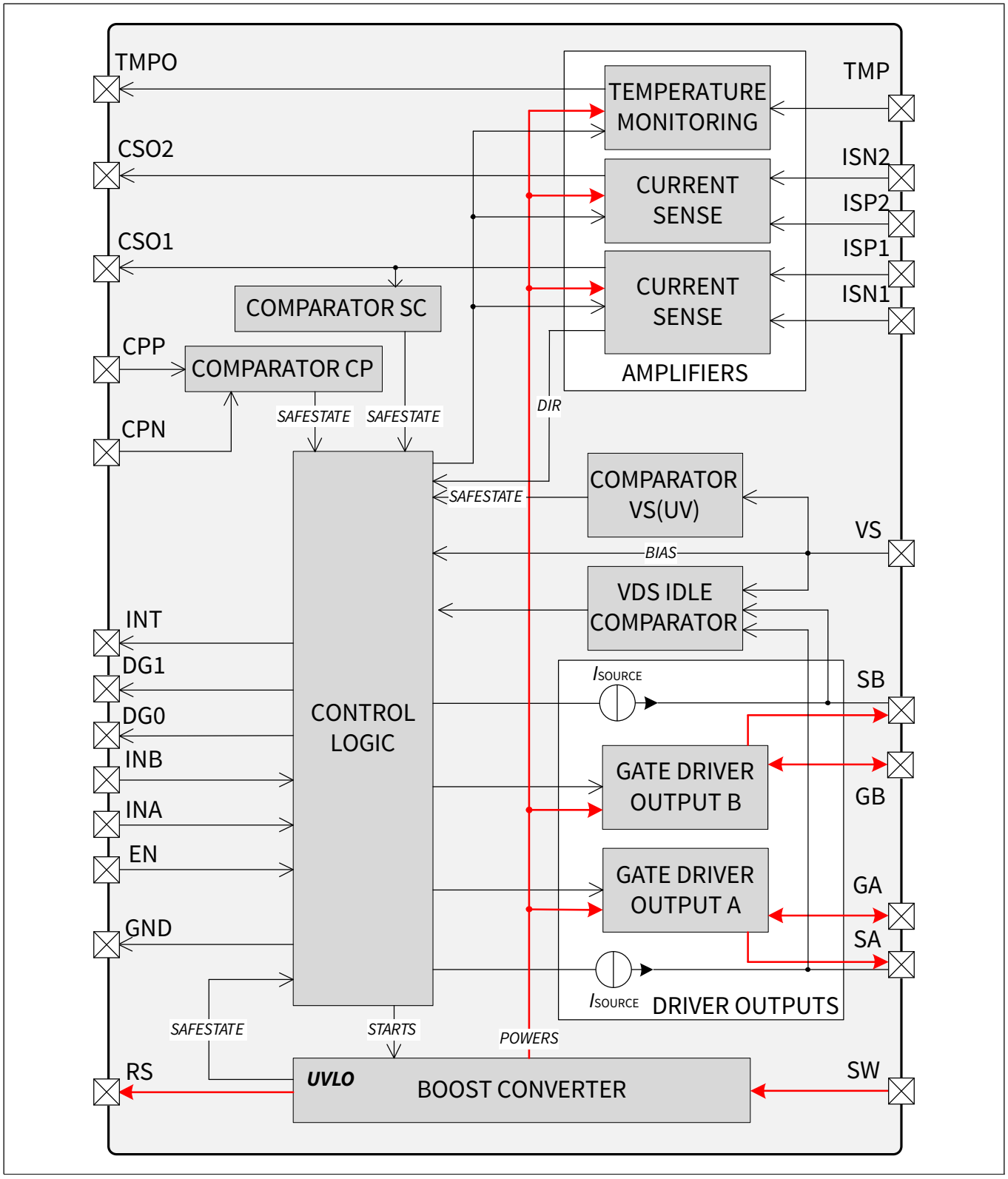


Figure 2 Functional block diagram

1 Block diagrams

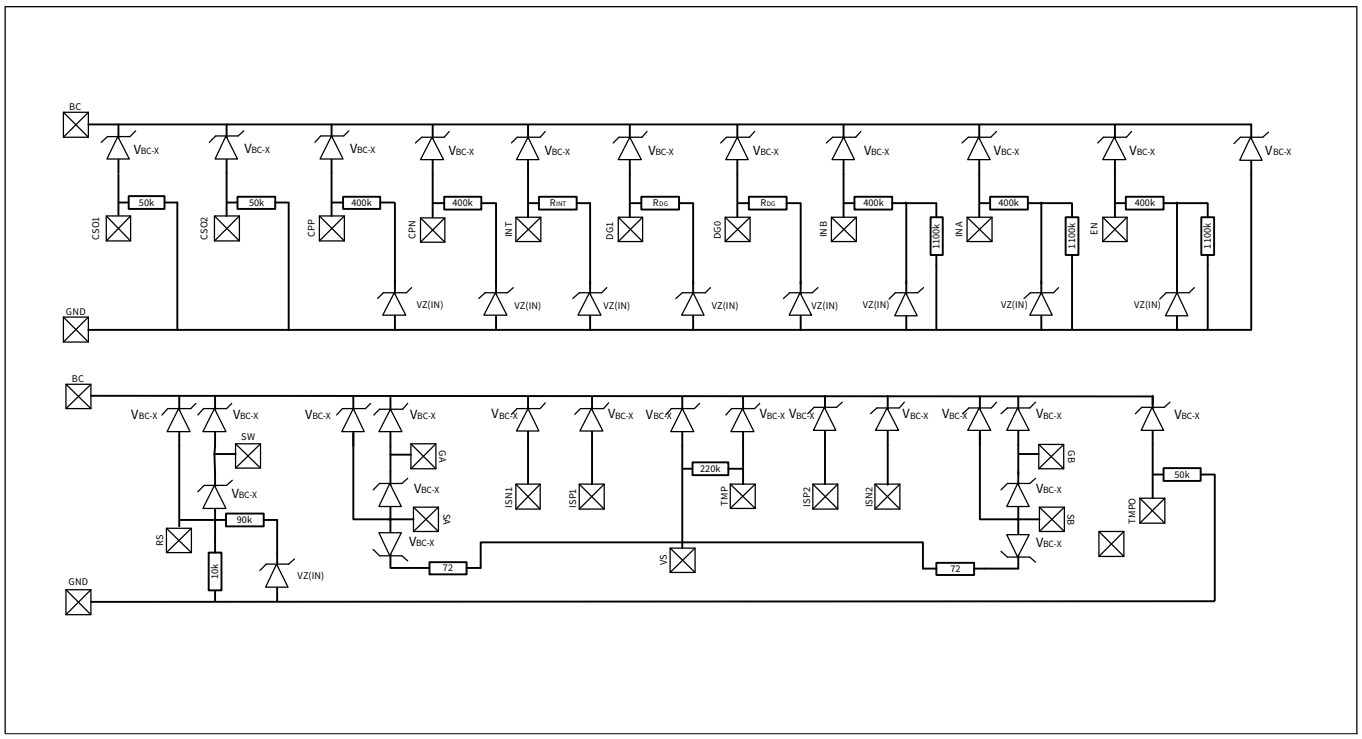


Figure 3 Diodes block diagram

2 Pin configuration

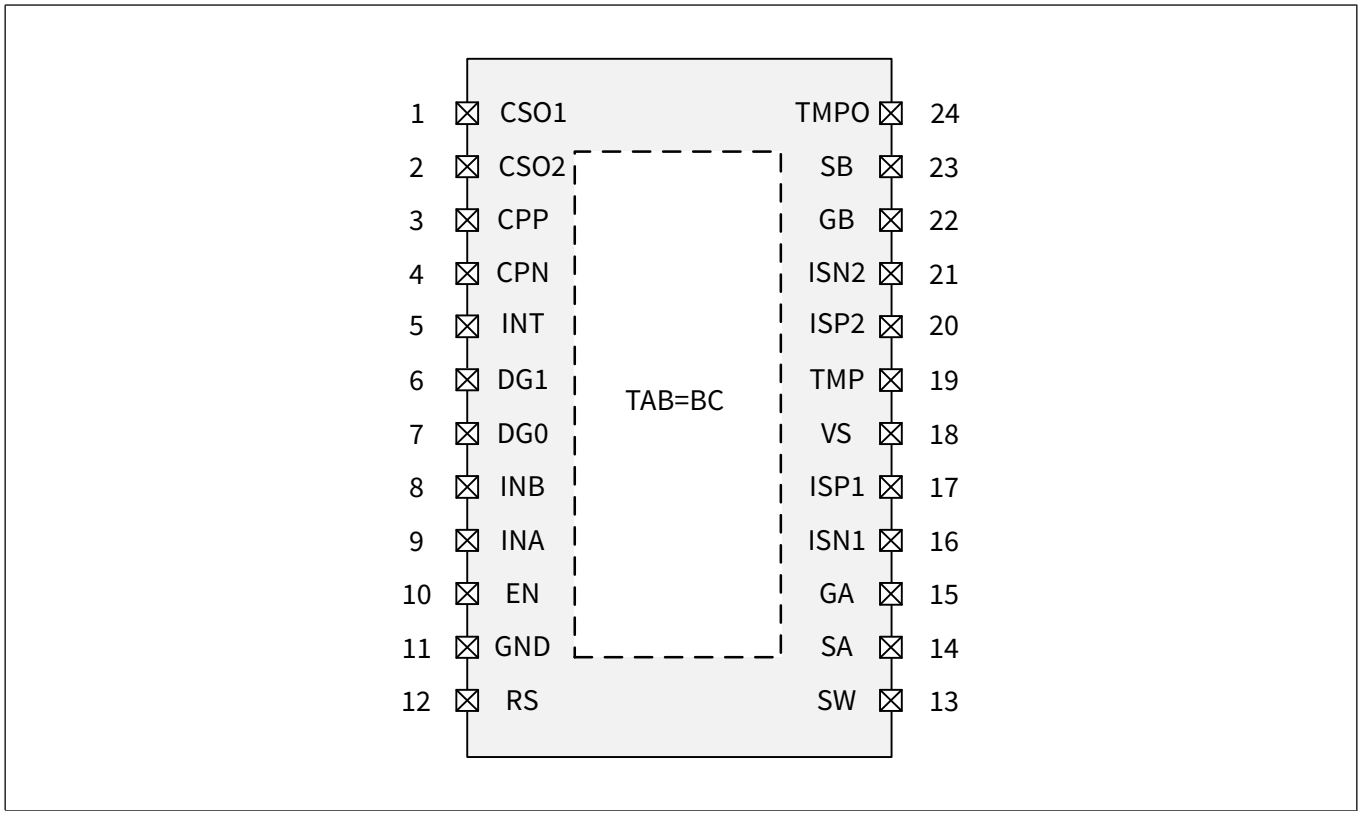


Figure 4

Table 1 Pin definitions and functions

Pin number	Symbol	I/O	Function
1	CSO1	I	Analog voltage to force SAFESTATE mode.
		O	**C**urrent **S**ense **O**utput **1**: analog voltage feedback, provides a voltage proportional to the shunt current or VDS across ISP1/ISN1.
2	CSO2	O	**C**urrent **S**ense **O**utput **2**: analog voltage feedback, provides a voltage proportional to the shunt current or VDS across ISP2/ISN2.
3	CPP	I	**C**om**p**arator **P**ositive: analog positive input of comparator.
4	CPN	I	**C**om**p**arator **N**egative: analog negative input of comparator.
5	INT	O	**Int**errupt: open drain interrupt output.

(table continues...)

Table 1 (continued) Pin definitions and functions

6	DG1	O	**D**ia**g**nostic **1:** DG1 is logic low in SLEEP mode. Digital voltage information of channel B VDS comparison to VS in IDLE mode. Digital voltage information of current flow direction in ON mode: • DG1 is logic high if current flows from ISP1 to ISN1 connection • DG1 is logic low if current flows from ISN1 to ISP1 connection Digital voltage information in SAFESTATE mode: • DG1 is logic high if SAFESTATE because of CP or SC or VS(UV) • DG1 is logic low if SAFESTATE because of UVLO
7	DG0	O	**D**ia**g**nostic **0:** DG0 is logic low in SLEEP mode. Digital voltage information of channel A VDS comparison to VS in IDLE mode. Digital voltage information of boost converter frequency in ON mode. Digital information in SAFESTATE mode: • DG0 is logic high if SAFESTATE because of CP or UVLO • DG0 is logic low if SAFESTATE because of SC or VS(UV)
8	INB	I	**In**put **B:** If INB digital logic is low, channel B switches OFF. If INB digital logic is high, channel B switches ON and gate driver is in ON mode only if pin ENABLE is logic high.
9	INA	I	**In**put **A:** If INA digital logic is low, channel A switches OFF. If INA digital logic is high, channel A switches ON and gate driver is in ON mode only if pin ENABLE is logic high.
10	EN	I	If **EN**ABLE digital logic is low, gate driver is in SLEEP mode, channels A and B are switched OFF and gate driver is RESET. If ENABLE digital logic is high, gate driver is in IDLE mode when INA and INB are both logic low.
11	GND	I/O	**G**rou**nd** connection.
12	RS	O	**R**esistor **s**ense output of boost converter: current measurement of the boost converter.
13	SW	I	**Sw**itching supply input of boost converter. Inductance connection.
14	SA	O	**S**ource **A**: output A connection to external MOSFET sources.
15	GA	I/O	**G**ate **A**: output A connection to external MOSFET gates.
16	ISN1	I	**I S**ense **N**egative 1: external shunt or VDS negative connection.
17	ISP1	I	**I S**ense **P**ositive 1: external shunt or VDS positive connection.
18	VS	I/O	**V**oltage reference, extended 3 V to 58 V.
19	TMP	I	**Tmp**erature Input: analog connection to external NTC or PTC thermistor.
20	ISP2	I	**I S**ense **P**ositive 2: external shunt or VDS negative connection.

(table continues...)

Table 1 (continued) Pin definitions and functions

21	ISN2	I	**I S**ense **N**egative 2: external shunt or VDS positive connection.
22	GB	I/O	**G**ate **B**: output B connection to external MOSFET gates.
23	SB	I	**S**ource **B**: output B connection to external MOSFET sources.
24	TMPO	O	**Temp**erature **O**utput: analog voltage feedback provides a voltage proportional to thermistor temperature.
TAB	BC	O	**B**oost **C**onverter output capacitor connection; driver supply.

Voltages are defined positive with respect to ground.
Currents are defined flowing into or from the pin depending on pins.

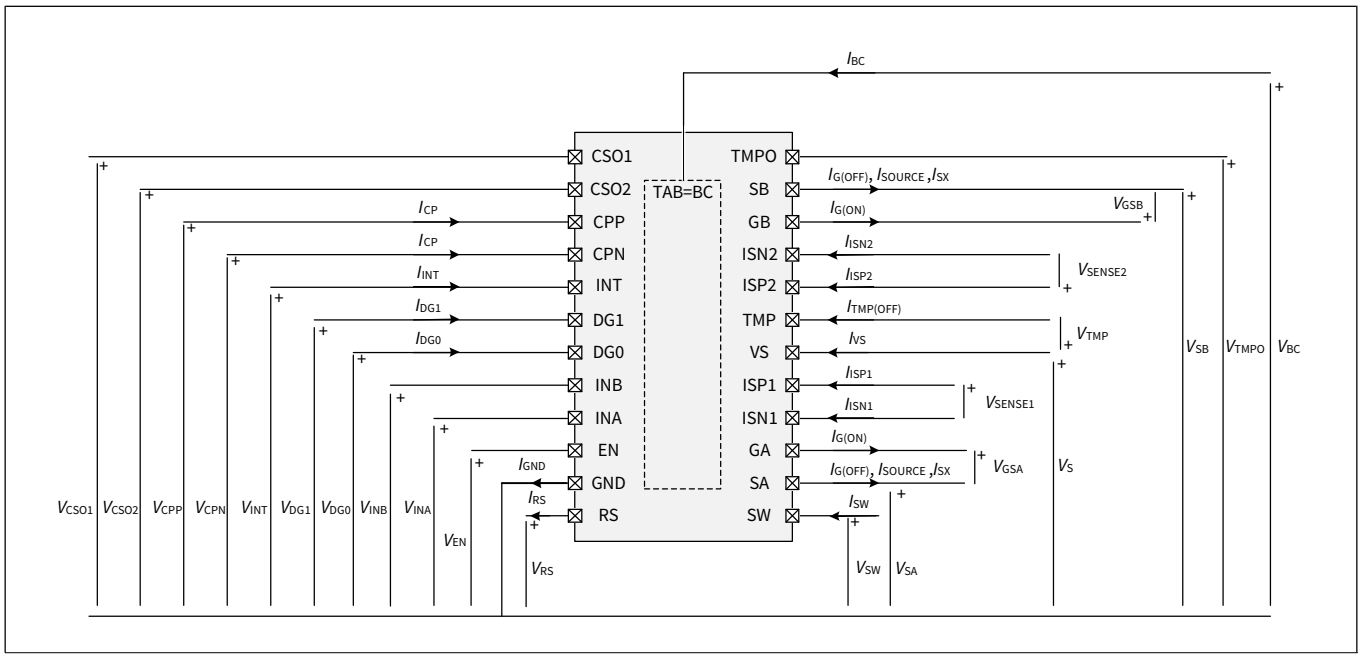


Figure 5 Voltage and current definitions – IEC 60375

3 General product characteristics

3.1 Absolute maximum ratings

T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Table 2 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Maximum voltage VBC (boost converter output) - all pins	V_{BC} - X	-0.3	–	75	V	1)	PRQ-26
Maximum drain-source voltages on each output	V_S - V_{SX}	-36	–	75	V	1)	PRQ-14
Maximum voltage between gate and source pins on each output	V_{GX} - V_{SX}	-0.3	–	75	V	1)	PRQ-331
Maximum voltage between SW and RS pin	V_{SW} - V_{RS}	-0.3	–	75	V	1)	PRQ-332
Maximum pulsed current in SW pin	I_{SW}	–	–	200	mA	1)	PRQ-16
Maximum operating junction temperature	$T_{J(MAX)}$	-40	–	150	°C	1)	PRQ-23
Storage temperature	$T_{STG(MAX)}$	-55	–	150	°C	1)	PRQ-24
ESD HBM susceptibility all pins	$V_{ESD(HBM)}$	-2	–	2	kV	1) HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)	PRQ-130
ESD CDM susceptibility all pins	$V_{ESD(CDM)}$	-500	–	500	V	1) Charged Device Model “CDM” according to ANSI/ESDA/JEDEC JS-002	PRQ-131
ESD CDM susceptibility corner pins	$V_{ESD(CDM)}$	-750	–	750	V	1) Charged Device Model “CDM” according to ANSI/ESDA/JEDEC JS-002	PRQ-132

1) Not subject to production test, specified by design

3.2 Functional ranges

T_J = -40 to 150°C, all voltages with respect to ground, typical values are given for V_S = 14 V and T_J = 25°C

Table 3 Functional ranges

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Voltage reference range for normal operation	$V_{S(NOR)}$	8	–	36	V	1)	PRQ-39
Voltage reference extended range	$V_{S(EXT)}$	3	–	58	V	1) Parameter deviations possible	PRQ-266
Voltage reference range with lower short-circuit protection	$V_{S(SC)LOW}$	3	–	8	V	1)	PRQ-40
Input pins ENABLE, INA, INB	V_{EN}, V_{INA}, V_{INB}	0	–	5.5	V	1)	PRQ-307
Diagnostic pins DG0, DG1	V_{DG0}, V_{DG1}	0	–	k_{DG}*V_{EN}	V	1) See k_{DG} parameter	PRQ-308
Interrupt pin INT	V_{INT}	0	–	5.5	V	1)	PRQ-309
Comparator reference voltage pins CPN, CPP	$V_{CP(REF)}$	1	–	5.5	V	1)	PRQ-183
Analog output pins saturation CSO 1&2, TMPO	$V_{AMP(SAT)}$	4	4.6	5.5	V	$V_S = V_{S(NOR)}$	PRQ-310
Current sense amplifiers gain range	G	10	–	200	–	1) For $G \leq 30$, use only R_{CSO} = 10 kΩ	PRQ-317
Supply voltage range for amplifier operation	V_{BC}-V_S	6	–	15	V	1)	PRQ-339
Amplifier input voltage range	V_{BC}-V_{ISxx}	6	–	15	V	1)	PRQ-341
Amplifier input voltage threshold for disconnection	$V_{ISxx-GND(TH)}$	0.2	0.7	1.5	V	1)	PRQ-340

1) Not subject to production test, specified by design

3.3 Thermal characteristics

Table 4 Thermal characteristic

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Thermal resistance junction to ambient	R_{thJA}	–	27	–	K/W	1) 2)	PRQ-38

1) Not subject to production test, specified by design
2) According to JEDEC51-2,-5,-7 at natural convection on FR4 2s2p board; the product (chip + package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. T_A = 85°C. Device is loaded with 1 W power.

4 Electrical characteristics

4.1 Static electrical characteristics

T_J = -40 to 150°C, V_S = 8 V to 36 V (unless otherwise specified), all voltages with respect to ground, positive current flowing into pin (unless otherwise specified), typical values are given for V_S = 14 V and T_J = 25°C

Table 5 Static electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Inputs pins							
Input A,B & Enable voltage high level	$V_{IN(H)}$, $V_{EN(H)}$	2.5	–	–	V	–	PRQ-74
Input A,B & Enable voltage low level	$V_{IN(L)}$, $V_{EN(L)}$	–	–	0.7	V	–	PRQ-75
Input A,B & Enable pull-down internal resistor	$R_{IN(GND)}$	0.5	1.5	2.5	MΩ	–	PRQ-318
Input zener diode for local pins	$V_{Z(IN)}$	5.5	6	6.5	V	*1)* See Figure 3	PRQ-319
Digital diagnostic pins							
Ratio diagnostic pin voltage high level over VEN	$k_{DG(H)}$	0.9	1	1.1	–	–	PRQ-84
Diagnostic pin voltage low level	$V_{DG(L)}$	–	–	0.1	V	V_{BC} = 72 V	PRQ-85
Diagnostic pin serial resistor	$R_{DG(GND)}$	5	10	20	kΩ	–	PRQ-86
Threshold for diagnostic change in IDLE mode	$V_{DS\_DIAG(TH)}$	1	2	3	V	V_S-V_{SA} (DG0) V_S-V_{SB} (DG1)	PRQ-91
Diagnostic delay in IDLE mode	$t_{DG(IDLE)}$	0	40	100	µs	IDLE mode only	PRQ-275
Delay for current direction change on DG1	t_{ISD}	0	8	18	µs	Indicates current flow direction change on CSA1 only ON mode only	PRQ-164
Interrupt pin pull-down internal resistor, SAFESTATE active	R_{INT}	7	12	17	kΩ	–	PRQ-88
Interrupt pin current leakage	$I_{INT(NOSAFESTATE)}$	–	–	0.3	µA	$V_{INT(H)} \leq$ 5.5 V	PRQ-89
Comparator (CP)							
Comparator offset	$V_{CP(OFFSET)}$	-50	–	50	mV	$V_{CP(REF)MIN} \leq V_{CP(REF)} \leq V_{CP(REF)MAX}$	PRQ-284
Comparator leakage input current	I_{CP}	-100	–	100	nA	V_{CP} = 5.5 V	PRQ-242

(table continues...)

Table 5 (continued) Static electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Temperature amplifier (TMPA)							
TMPA input current	$I_{TMP(OFF)}$	-100	–	100	nA	–	PRQ-185
TMPA input offset	$V_{TMP(OFFSET)}$	-10	0	+10	mV	–	PRQ-186
TMPA ratio	k_{TMP}	9.5	10	10.5	–	–	PRQ-187
TMPA pull-down resistor	R_{TMPO}	20	–	100	kΩ	1)	PRQ-188
Current sense amplifiers (CSA1 & CSA2)							
CSA input offset	$V_{ISx(OFFSET)}$	-50	0	50	µV	1)	PRQ-323
CSA input blind range	$V_{ISx(BLIND)}$	-500	0	500	µV	–	PRQ-324
CSA delay maximum accuracy	$t_{CSA(ACC)}$	0	200	400	µs	–	PRQ-325
CSA settling time	$t_{CSA(SET)}$	1	10	20	µs	1) Step 25% G=100	PRQ-328
CSA output pull-down resistor	R_{CSOx}	10	20	50	kΩ	1)	PRQ-326
CSA gain intrinsic error	$\varepsilon_{(G)}$	-1	0	1	%	1) G = 10..200	PRQ-327
PSRR - CSA power supply rejection ratio	$PSRR_{1kHz}$	–	105	–	dB	2) f = 1 kHz, G = 100, R_{CSO} = 20 k see Figure 34	PRQ-336
CMRR - CSA common mode rejection ratio	$CMRR_{1kHz}$	–	116	–	dB	2) f = 1 kHz, G = 100, R_{CSO} = 20 k see Figure 34	PRQ-337
Noise - CSA Voltage noise, RTI	$Noise$	–	180	–	nV_{RMS}	2) G = 100, R_{CSO} = 20 k RTI	PRQ-338

1) Not subject to production test, specified by design
2) Not subject to production test, specified by characterization.

4.2 Protection characteristics

T_J = -40 to 150°C, V_S = 8 V to 36 V (unless otherwise specified), all voltages with respect to ground, positive current flowing into pin (unless otherwise specified), typical values are given for V_S = 14 V and T_J = 25°C

Table 6 Protection characteristics

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Protection thresholds							
Current shutdown internal threshold ratio from Enable pin voltage	$k_{CSO1(TH)}$	0.71	0.74	0.77	–	V_S = 8 V to 58 V ON mode, CSA1 only See Chapter 8.1	PRQ-168
Under voltage threshold	$V_{S(UV)}$	0.5	1	1.5	V	V_S - GND ON mode only	PRQ-66
Protection delays							
Delay between short circuit and CSO1 high	$t_{DSCCSO1(H)}$	0.2	1.5	6	µs	1) G = 100 V_{EN}=3.3V	PRQ-181
Delay between CSO1 high and INT = low	$t_{DCSO1(H)INT(L)}$	0.5	5	10	µs	1) G = 100	PRQ-182
Delay between CP high and INT	$t_{DCP(H)INT(L)}$	1	9	17	µs	$V_{CP(REF)MIN} \le V_{CP(REF)} \le V_{CP(REF)MAX}$	PRQ-184
Delay between UV on VS and INT = low	$t_{DUV(H)INT(L)}$	8	22	40	µs	–	PRQ-320
Delay between INT = low and gate 80%	$t_{DINT(L)G(L)}$	–	3	5	µs	1) $C_{G(EQ)}$ = 100 nF	PRQ-136
Delay between short circuit and gate 80%	$t_{DSCG(L)}$	0.7	5.5	10	µs	1) G = 100 V_{EN} = 3.3 V $C_{G(EQ)}$ = 100 nF	PRQ-330
Time to reset	t_{RESET}	3	–	30	µs	Reset from SAFESTATE: $V_{EN} < V_{EN(L)}$ for t_{RESET} duration	PRQ-94

1) Sum of PRQ-181, PRQ-182,PRQ-136 max. does match max. of the sum PRQ-330 due to silicon process and variation.

4.3 Driver outputs electrical characteristics

T_J = -40 to 150°C, V_S = 8 V to 36 V (unless otherwise specified), all voltages with respect to ground, current positive while flowing out of pin (unless otherwise specified), typical values are given for V_S = 14 V and T_J = 25°C

Table 7 Driver outputs electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Source pre-charge current	I_{SOURCE}	6	15	25	mA	$V_S - V_{Sx} \ge V_{DS\_DIAG(TH)}$	PRQ-56

(table continues...)

Table 7 (continued) Driver outputs electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Delay between Enable = high and Source pre-charge current active	$t_{DSOURCE}$	4	-	100	µs	IDLE mode only	PRQ-210
Power on input delay	t_{POI}	0	2	5	µs	Time to activate protections before turn-on after INx = high	PRQ-158
Turn-on delay	$t_{D(ON)}$	1	4	7	µs	$C_{G(EQ)}$ = 100 nF	PRQ-50
Rise time on gate 20% to 80% of VBC - VS	t_R	0	7	15	µs	$C_{G(EQ)}$ = 100 nF	PRQ-51
Gate turn on short circuit pulsed current per gate	$I_{G(ON)}$	50	175	–	mA	V_{GX} - V_{SX} = 0 V	PRQ-52
Turn-off delay	$t_{D(OFF)}$	1	4	7	µs	$C_{G(EQ)}$ = 100 nF	PRQ-53
Fall time on gate 80% to 20% of VBC - VS	t_F	0	2	5	µs	$C_{G(EQ)}$ = 100 nF	PRQ-54
Gate turn-off short circuit pulsed current per gate	$I_{G(OFF)}$	350	1400	–	mA	V_{GX} - V_{SX} = 14 V	PRQ-276

4.4 Boost converter (BC) characteristics

T_J = -40 to 150°C, V_S = 8 V to 36 V (unless otherwise specified), all voltages with respect to ground, typical values are given for V_S = 14 V and T_J = 25°C

Table 8 Boost converter (BC) characteristics

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
BC Boost capacitor	C_{BC}	20 * $C_{G(EQ)}$	–	–	F	1) $C_{G(EQ)}$ = external MOSFET equivalent gate source capacitance	PRQ-137
BC switching current limitative resistor	R_{RS}	10	–	30	Ω	1) Use 1/2 W resistor min.	PRQ-138
BC output VBC - VS regulation voltage	$V_{BC(TH)}$	11.5	12.5	14	V	–	PRQ-139
VBC(TH) to UVLO regulation gap	$V_{BC(RG)}$	1.9	2.5	–	V	–	PRQ-141
BC undervoltage lockout voltage	*UVLO*	9.5	10	11	V	–	PRQ-140

(table continues...)

Table 8 (continued) Boost converter (BC) characteristics

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Delay between UVLO and INT = low	$t_{DUVLO(H)INT(L)}$	0	10	40	µs	–	PRQ-142
RS deactivation threshold	$V_{RS(TH)}$	0.7	1	1.4	V	–	PRQ-147
Forward voltage of BC diode	V_{FBC}	0	0.9	1.1	V	I_F = 100 mA	PRQ-148
On-state resistance of BC switch	$R_{DS(ON)K1(25)}$	1	11	15	Ω	I = 100 mA; T_J = 25°C	PRQ-150
Boost converter off-time	$t_{BC(OFF)}$	1	4	5	µs	–	PRQ-152
Time to reach RS deactivation threshold	$t_{RS(TH)}$	–	920	–	ns	2) V_S = 12 V; R_{RS} = 10 Ω; L = 100 µH / 1.7 Ω; T_J = 25°C	PRQ-154
Turn-off delay of K1	$t_{D(OFF)K1}$	0.05	0.2	0.3	µs	–	PRQ-155
Boost power-on delay	t_{POD}	–	960	–	µs	3) V_S = 12 V; R_{RS} = 10 Ω; L = 100 µH / 2 Ω ; C_{BC} = 1µF; T_J = 25°C See AppNote Getting Started with 2ED2410-EM	PRQ-157

1) Not subject to production test, specified by design
2) Not subject to production test, specified by calculation.
3) Not subject to production test, specified by characterization.

4.5 Current consumptions

T_J = -40 to 150°C, V_S = 8 V to 36 V (unless otherwise specified), all voltages with respect to ground, positive current flowing into pin (unless otherwise specified), typical values are given for V_S = 14 V and T_J = 25°C

Table 9 Current consumptions

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
GND pin current in SLEEP mode	$I_{GND+RS(SLEEP)}$	1	6	15	µA	V_S = 24 V V_{BC} = V_S	PRQ-68
Sources leakage current in SLEEP mode	$I_{SX(SLEEP)}$	0.1	0.5	4	µA	V_{BAT} = 24 V V_S - V_{SX} = V_{BAT}	PRQ-285
VS pin current in IDLE mode	$I_{VS(IDLE)}$	-15	-6	-2	µA	V_S = 24 V V_{SX} = V_S	PRQ-69
VS pin current in IDLE mode, 25°C	$I_{VS(IDLE)25}$	-10	-6	-2	µA	T_J = 25°C	PRQ-294

(table continues...)

Table 9 (continued) Current consumptions

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
BC current in IDLE mode	$I_{BC(IDLE)}$	5	10	50	µA	V_S = 24 V V_{BC}-V_S = 14 V	PRQ-144
BC current in IDLE mode, 25°C	$I_{BC(IDLE)25}$	5	10	20	µA	T_J = *25°C*	PRQ-297
VS pin current in ON mode	$I_{VS(ON)}$	-20	-4	0	µA	–	PRQ-72
VS pin current in ON mode, 25°C	$I_{VS(ON)25}$	-10	-4	-1	µA	T_J = 25°C	PRQ-295
BC current in ON mode	$I_{BC(ON)}$	10	55	150	µA	V_{BC} - V_S = 14 V	PRQ-145
BC current in ON mode, 25°C	$I_{BC(ON)25}$	10	55	90	µA	T_J = 25°C	PRQ-298
BC current in ON mode, 25°C, one CSA disconnected	$I_{BC(ON)25\_1CSA(OFF)}$	10	45	70	µA	*1)* T_J = 25°C CSA 1 **or** 2 not used see Chapter 7	PRQ-300
BC current in ON mode, 25°C, all amplifiers disconnected	$I_{BC(ON)25\_2CSA(OFF)}$	6	20	35	µA	*1)* T_J = 25°C CSA 1 and 2 not used see Chapter 7	PRQ-301
BC current in ON mode, ≤ 85°C, one CSA disconnected	$I_{BC(ON)\le85\_1CSA(OFF)}$	10	45	85	µA	*1)* $T_J \le 85$°C CSA 1 **or** 2 not used see Chapter 7	PRQ-302
BC current in ON mode, ≤ 85°C, all amplifiers disconnected	$I_{BC(ON)\le85\_2CSA(OFF)}$	6	20	45	µA	*1)* $T_J \le 85$°C CSA 1 and 2 not used see Chapter 7	PRQ-303
VS pin current in SAFESTATE mode	$I_{VS(SAFESTATE)}$	-20	-4	0	µA	–	PRQ-73
BC current in SAFESTATE mode	$I_{BC(SAFESTATE)}$	10	55	150	µA	V_{BC} - V_S = 14 V	PRQ-146

1) Not subject to production test, specified by design

5 General operation

5.1 Operating modes

2ED2410-EM works with 4 operating modes: SLEEP, IDLE, ON and SAFESTATE, selected by a combination of inputs INA, INB and ENABLE pins, and in the case of SAFESTATE, by protection features or force signal.

INPUTS			Operating mode		OUTPUTS										
EN	INA	INB			Boost converter output V_{BC} - V_S	INT	DG0	DG1	V_{CSO1}	V_{CSO2}	V_{TMPO}	V_{GA}-V_{SA}	V_{GB}-V_{SB}	I_{SOURCE}	*comments*
0	X	X	**SLEEP**		0	1*	0	0	0	0	0	0	0	0	*once reset is done, provided that pull-up voltage is available
1	0	0	**IDLE**		$V_{BC(TH)}$	1	V_S - V_{SA}*	V_S - V_{SB}*	0	0	0	0	0	active[1)]	*DG_X = 0 if V_S - V_{SX} > $V_{DS\_DIAG(TH)}$ for each output, else DG_X = 1 if V_S - V_{SX} ≤ $V_{DS\_DIAG(TH)}$
1	1	0	**ON**		$V_{BC(TH)}$	1	pulse when K1 activated*	direction of current CSA1*	active	active	active	$V_{BC(TH)}$	0	active[1)]	*high level: see V_{DG0}, V_{DG1} in Functional ranges Table
	0	1										0	$V_{BC(TH)}$		
	1	1										$V_{BC(TH)}$	$V_{BC(TH)}$		
1	X	X	**SAFESTATE**	SC or UV	$V_{BC(TH)}$	0	0	1	active	active	active	0	0	active[1)]	NB: if several faults occurs in series, only first fault is indicated by DG1 and DG0 *depends on UVLO root cause
				UVLO	≤ $V_{BC(TH)}$*		1	0							
				CP	$V_{BC(TH)}$		1	1							

Figure 6 Inputs, modes and outputs states

(1) See Chapter 6.

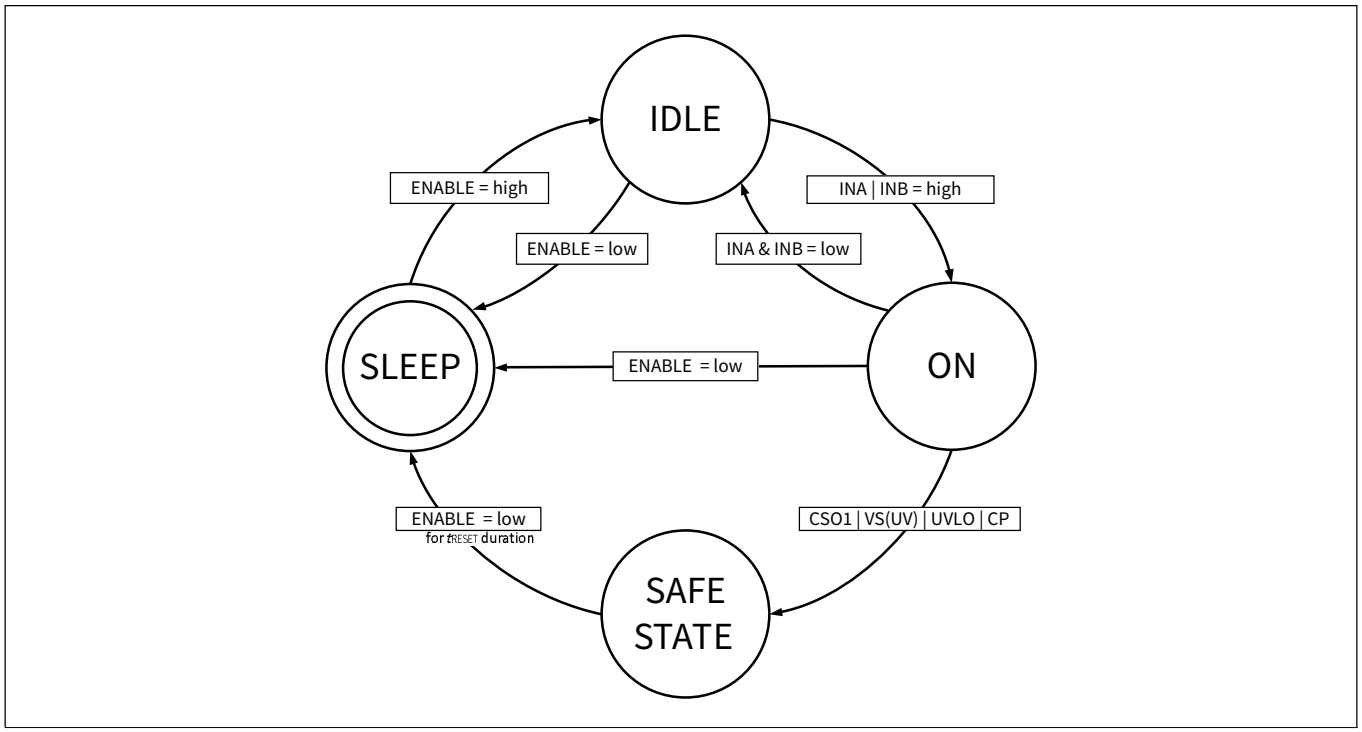


Figure 7 State machine of 2ED2410-EM

5.2 Current consumption

The current consumption of the driver from the system battery(or power supply), also named quiescent current (I_q) of 2ED2410-EM, depends on:

- the mode the driver is in.
- the external components used for the boost converter, which is both the driver supply and the external MOSFET gate supply.
- for SLEEP mode, it also depends on the MOSFET structure used.

In this datasheet are only given consumption at driver level, not at system battery/power supply level.

Details of quiescent current calculation from the battery are given in the application note "Getting started with 2ED2410-EM".

5.3 Timing diagram

The following diagram shows digital inputs, digital outputs, the boost converter output and gate outputs from SLEEP to ON until short-circuit event occurs, and the reset procedure back to SLEEP mode.

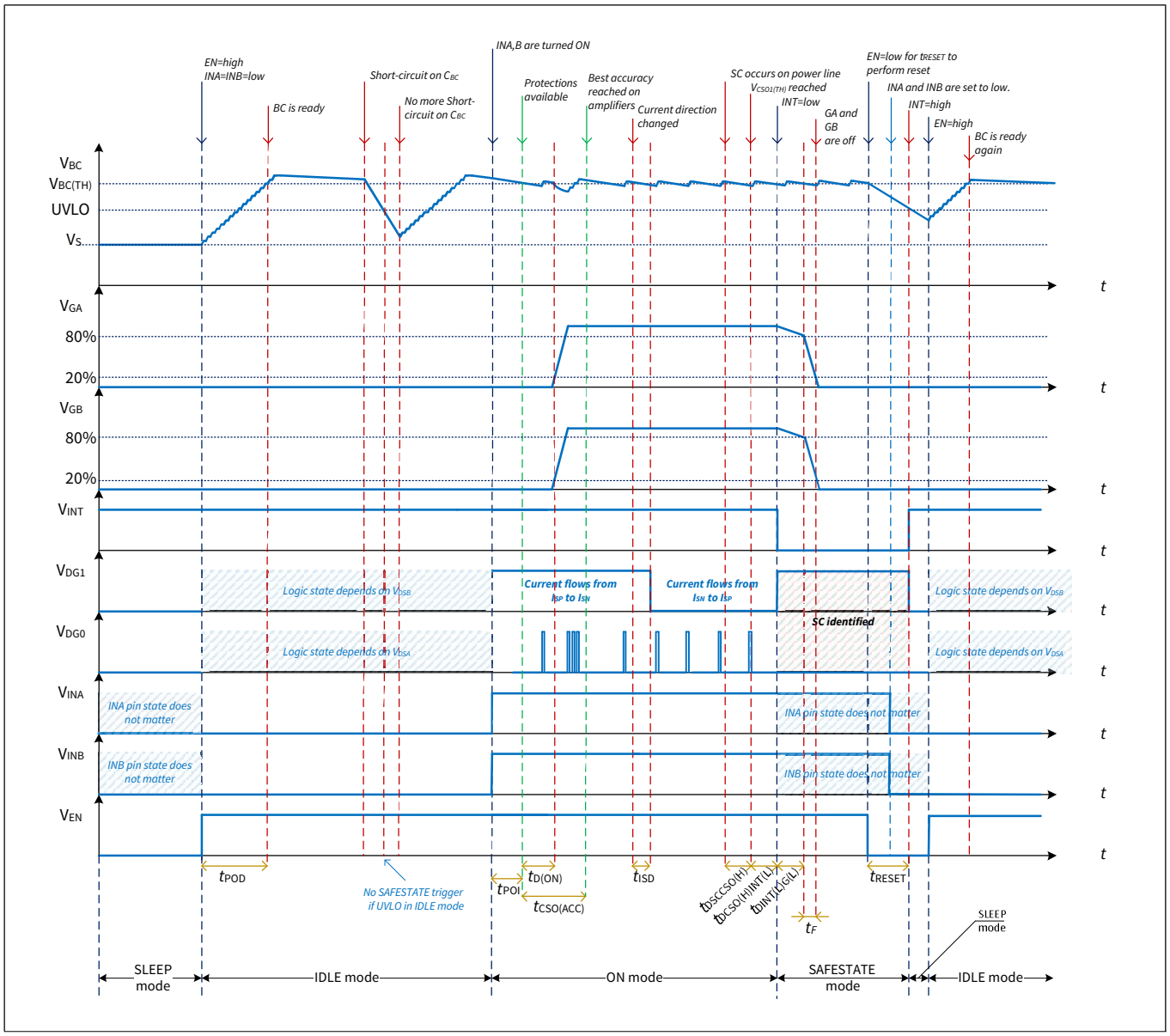


Figure 8 **Timings diagram with IDLE mode, ON mode with short-circuit event and SAFESTATE with reset – *Note: time and voltages are not to scale***

5.4 Logic pins

Logic pins are compatible to 5 V and 3.3 V microcontrollers. They can be connected directly to a microcontroller output without the need of an additional component. There is an internal series and pull-down resistor [PRQ-318]. A RC network for stabilizing voltage on EN pin can be used, since EN voltage is used for internal reference in the logic.

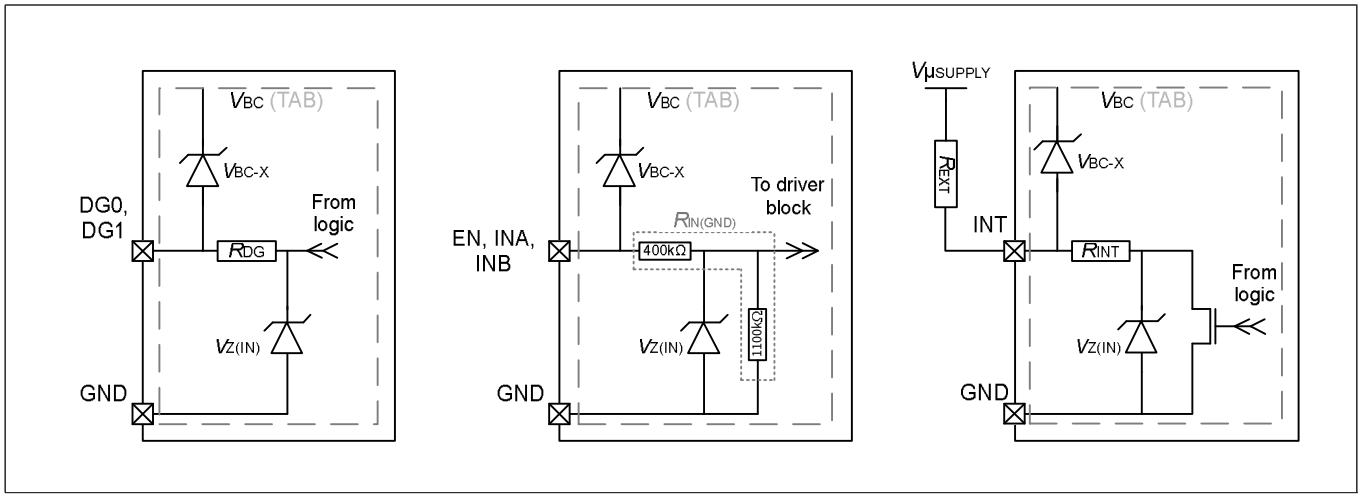


Figure 9 Digital I/O

The inputs control circuitry drives the output gate driver stage. They are pulled-down to GND with a $R_{IN(GND)}$ resistor to avoid unintended switch-on.

The inputs circuitry are set to logic high when $V_{INX} > V_{IN(H)}$ or $V_{EN} > V_{IN(H)}$.

The ENABLE pin controls the ON/OFF of the boost converter and biases all analog logic.

ENABLE = 1 sets V_{BC}-$V_S \geq V_{BC(TH)}$ after a time t_{POD}.

The INx pins directly control the gate outputs therefore INA = 1 sets GA = 1 and INB = 1 sets GB = 1. The inputs/outputs A and B are independent

If ENABLE and at least one of the INx pins are set high together, protections and measurements are turned ON but gates will turn-on only when V_{BC}-$V_S \geq V_{BC(TH)}$.

When driver enters ON mode by INx = 1, protections are ready after a time t_{POI} and amplifiers get maximum accuracy after a time $t_{CSA(ACC)}$ (see Chapter 4.1).

The INx and ENABLE pins are set to logic low when $V_{INX} < V_{IN(L)}$ or $V_{EN} < V_{IN(L)}$.

The digital outputs give back either a low or high logic level signal. The output high voltage level is based on V_{EN} and is given in the electrical characteristics table as a ratio between V_{DGx} and V_{EN}. See parameter k_{DG} in Chapter 4.1.

DG0 and DG1 in a low logic state have a value ≤ $V_{DG(L)}$. The state of the diagnostic depends the operating mode the driver is in, refer to Chapter 5.1.

In ON mode, DG0 reflects the activation of boost converter switch K1 (see Chapter 9): each time K1 is activated, DG0 = 1.

In ON mode, DG1 reflects the current direction on CSA1: DG1 = 0 if current is flowing from ISP1 to ISN1, DG1 = 1 if current is flowing from ISN1 to ISP1 (see Chapter 7).

INT pin is an open-drain output. The intent is to deliver an interrupt signal to relevant surrounding devices, such as microcontroller or power supply management chip (e.g. Infineon SBC).

INT needs to be externally pulled-up, e.g. to the microcontroller supply $V\mu_{SUPPLY}$. The value of V_{INT} when SAFESTATE is triggered, is the result of the voltage divider between the external resistor R_{EXT} and R_{INT}.

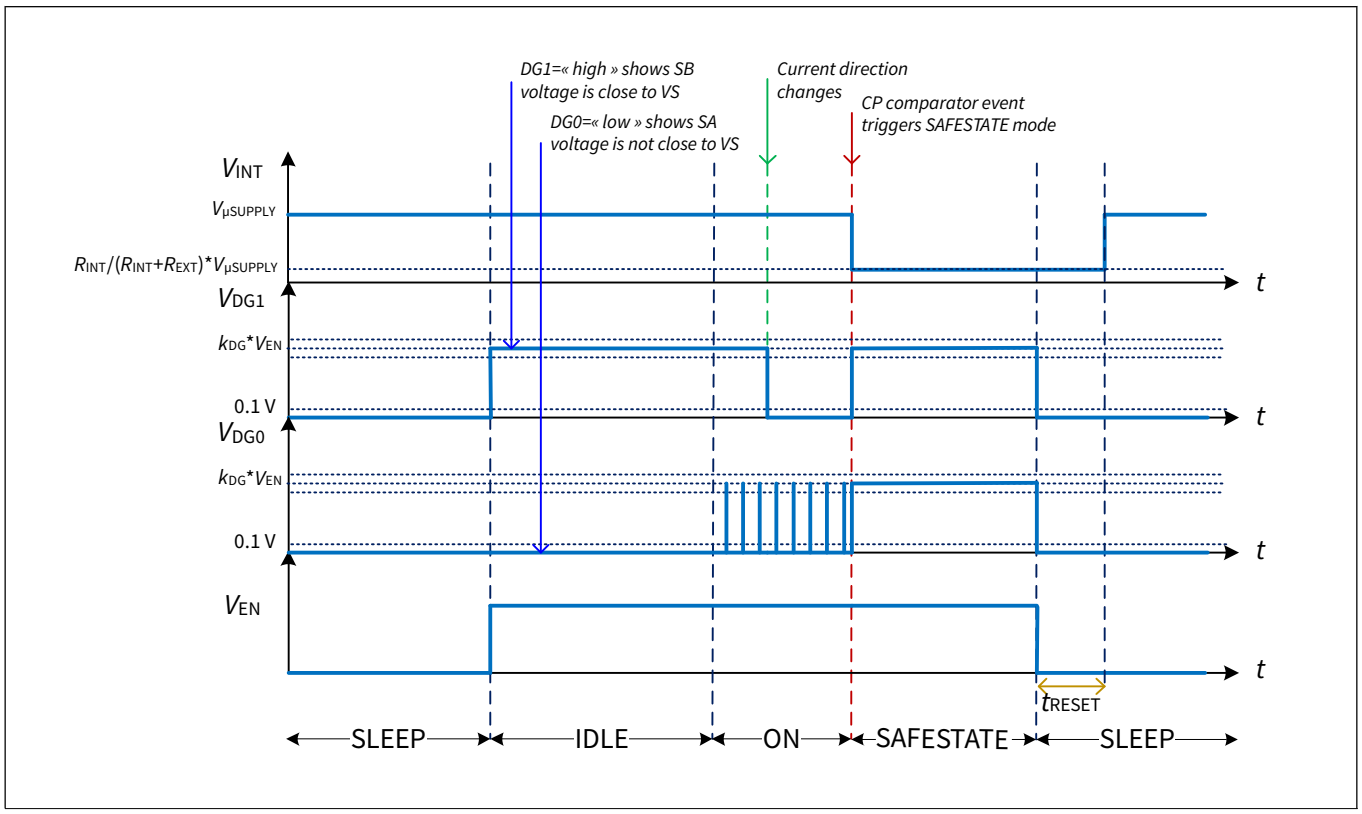


Figure 10 Diagnostics behavior

5.5 Gate outputs

2ED2410-EM features two identical gate outputs GA and GB working with source pins SA and SB respectively.

These outputs are activated by setting the corresponding digital input INA or INB to a high logic level.

The structure of these outputs is a push-pull and the logic ensures by design that both MOSFET K2x and K3x will not be ON at the same time (no shoot-through).

K2x are P-channel enhancement MOSFET and K3x are N-channel enhancement MOSFET.

The current to switch ON the external MOSFET connected to the gate driver is delivered by boost converter capacitor C_{BC}, through K2x to the gate pins Gx.

The current to switch OFF the external MOSFET is sunk from gate pins Gx through K3x to the source pins Sx.

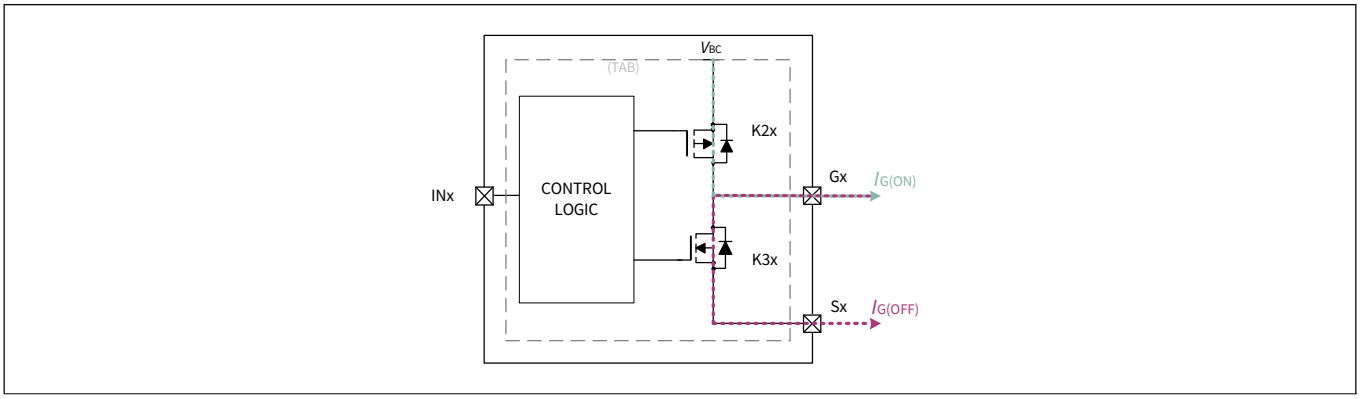


Figure 11 Gate output structure

When the first input is switched on, a time delay t_{POI} needs to be considered. This time delay, power-on-input, is needed to make sure protections are activated before sending gate signal activation, so 2ED2410-EM never switches the MOSFET on without current sense and temperature amplifiers. If these functions are not used, t_{POI} still needs to be considered.

If V_{BC}-$V_S \leq V_{BC(TH)}$ when the input signals INx are set high, the driver will be in ON mode but the gate outputs will remain OFF until $V_{BC(TH)}$ is reached on boost converter output.

If V_{BC}-$V_S \leq V_{BC(TH)}$ occurs when the gates are ON, this under-voltage on the boost converter will trigger the lock-out of the gates and the driver will enter SAFESTATE, consequently turning and keeping off the gates. See Chapter 8.4 and refer to Chapter 9 to see how gate outputs and the boost converter are connected.

The timings for the gate outputs are described in Figure 12.

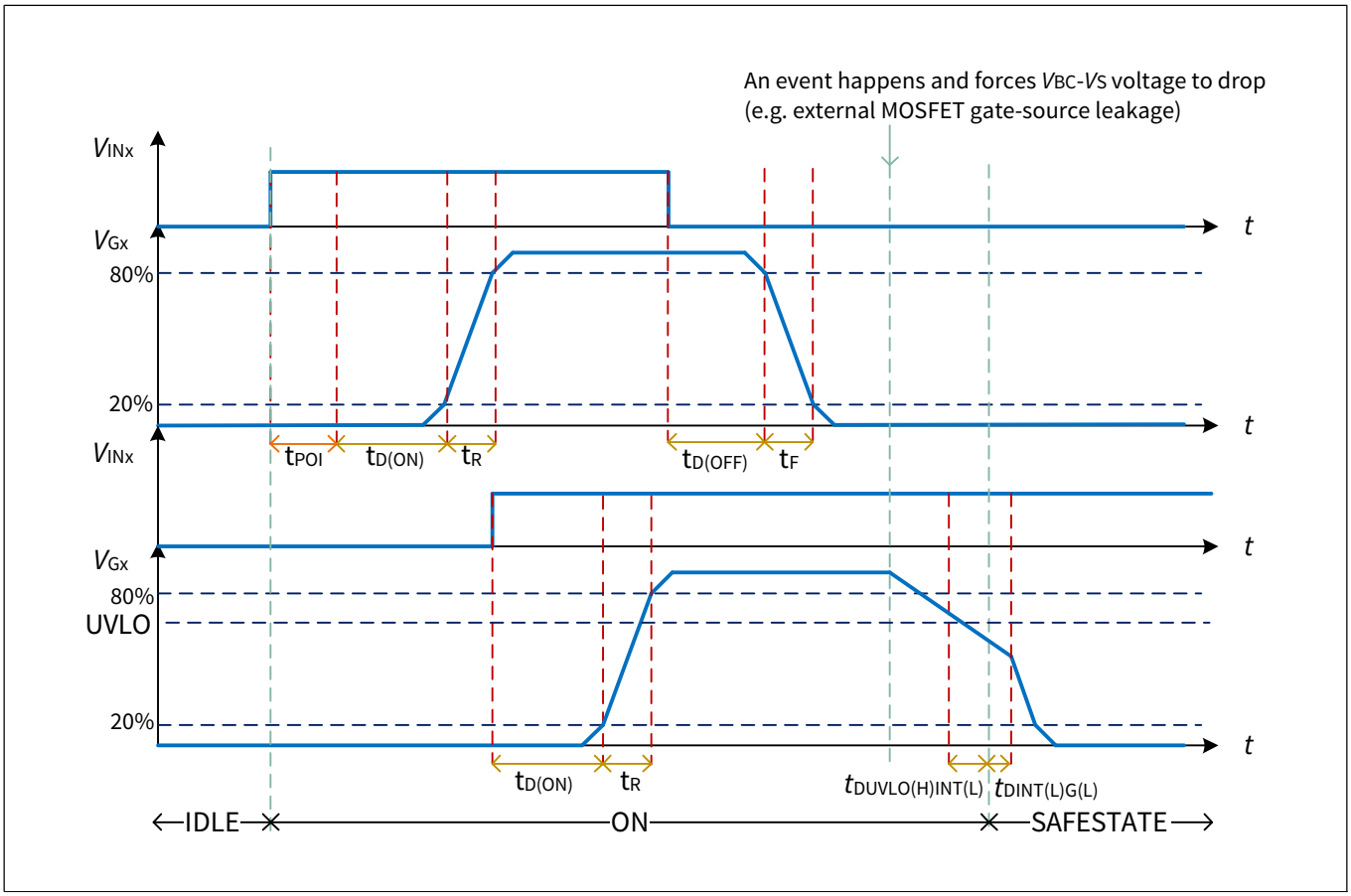


Figure 12 Gate timings (not to scale, for understanding purposes only)

5.6 Ground loss protection: module level

MOSFET K3 (see Figure 11, chapter 5.5) is turned on by default on each output as long as VS present.

If GND board/ECU connection is lost, K3 remains on or is turned on as long as the below conditions are true.

As a result gate-source is pulled-down in the following conditions:

- VS pin is connected to battery line
- GND board/ECU disconnected
- SLEEP, IDLE, ON or SAFESTATE modes

In ON mode, if GND board/ECU is connected back, driver outputs will be turned on again (and therefore K3 switch off) without necessary reset from pin ENABLE.

6 Low by-pass current feature

When in IDLE mode, 2ED2410-EM can sink a low current from VS pin to its source pins SA and/or SB and from SA to SB or SB to SA.

The activation is autonomous.

Up to $V_{SX} = V_S - V_{DS\_DIAG(TH)}$, I_{SOURCE} is delivered with typical value [see PRQ-56]. When $V_S - V_{DS\_DIAG(TH)}$ threshold [see PRQ-91] is reached on the corresponding source the I_{SOURCE} decreases gradually and is turned-off when $V_{SA} = V_{SB} = V_S$.

As a consequence, 2ED2410-EM is able to supply a current I_{SOURCE} to supply ECU idle mode currents, while keeping its self-consumption very low.

It can also be used to pre-charge ECU input capacitors in the downstream power-net, and keep them charged in car park mode with minimal current consumption.

If a short-circuit occurs at ECU side during the driver's IDLE mode, I_{SOURCE} is still supplied, however V_{DSX} is constantly monitored and the corresponding DGx is set to low. This allows, for example, detection of a short-circuit before turn-on. See Chapter 7.1 for diagnostics behaviour in IDLE mode.

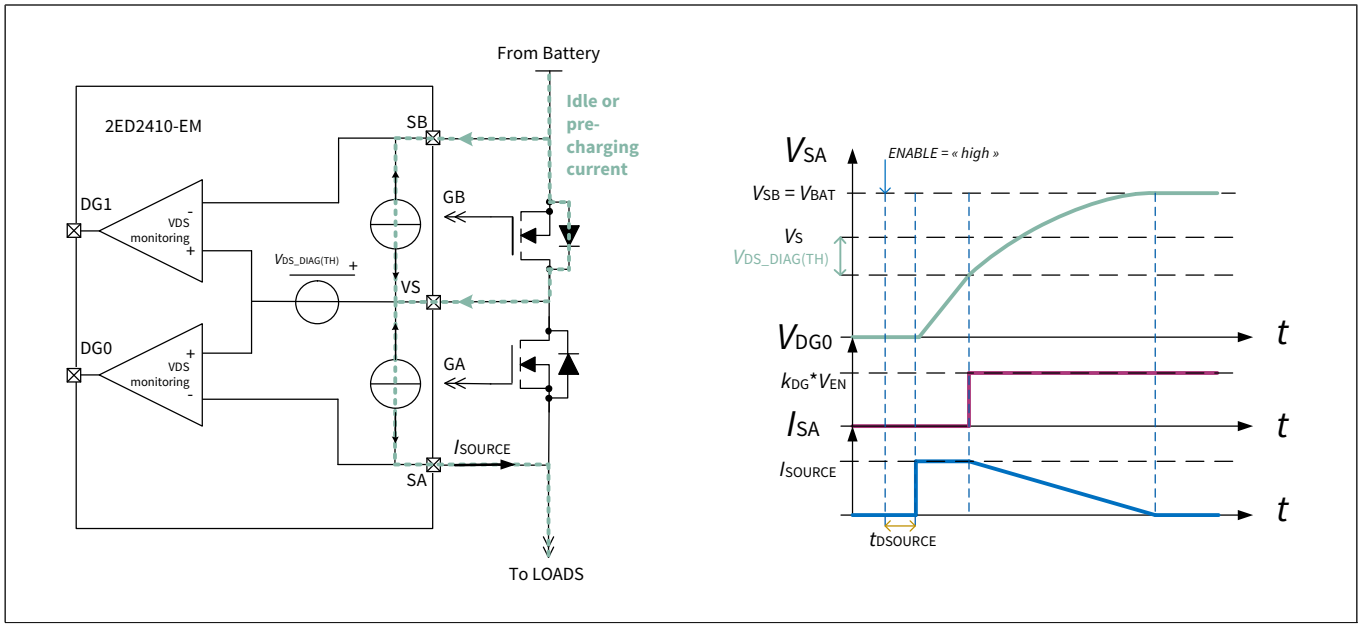


Figure 13 Low by-pass current principle of operation and timing diagram (not to scale)

7 Measurement features

7.1 VDS monitoring in IDLE mode

The VDS monitoring function can be read on DGx pins in IDLE mode.

DG0 and DG1 respectively monitor V_{DSA} (V_S - VSA) and V_{DSB} (V_S - V_{SB}), provided that MOSFET drains are connected to VS pin.

If V_{DSA} (or V_{DSB}) > V_S - $V_{DS\_DIAG(TH)}$ => DG0 (or DG1) = high level ($I_{source\ B}$ active, see Chapter 6).

If V_{DSA} (or V_{DSB}) < V_S - $V_{DS\_DIAG(TH)}$ => DG0 (or DG1) = low level ($I_{source\ B}$ active, see Chapter 6).

MOSFET sources are compared to an internal reference voltage V_S - $V_{DS\_DIAG(TH)}$ (see parameter $V_{DS\_DIAG(TH)}$).

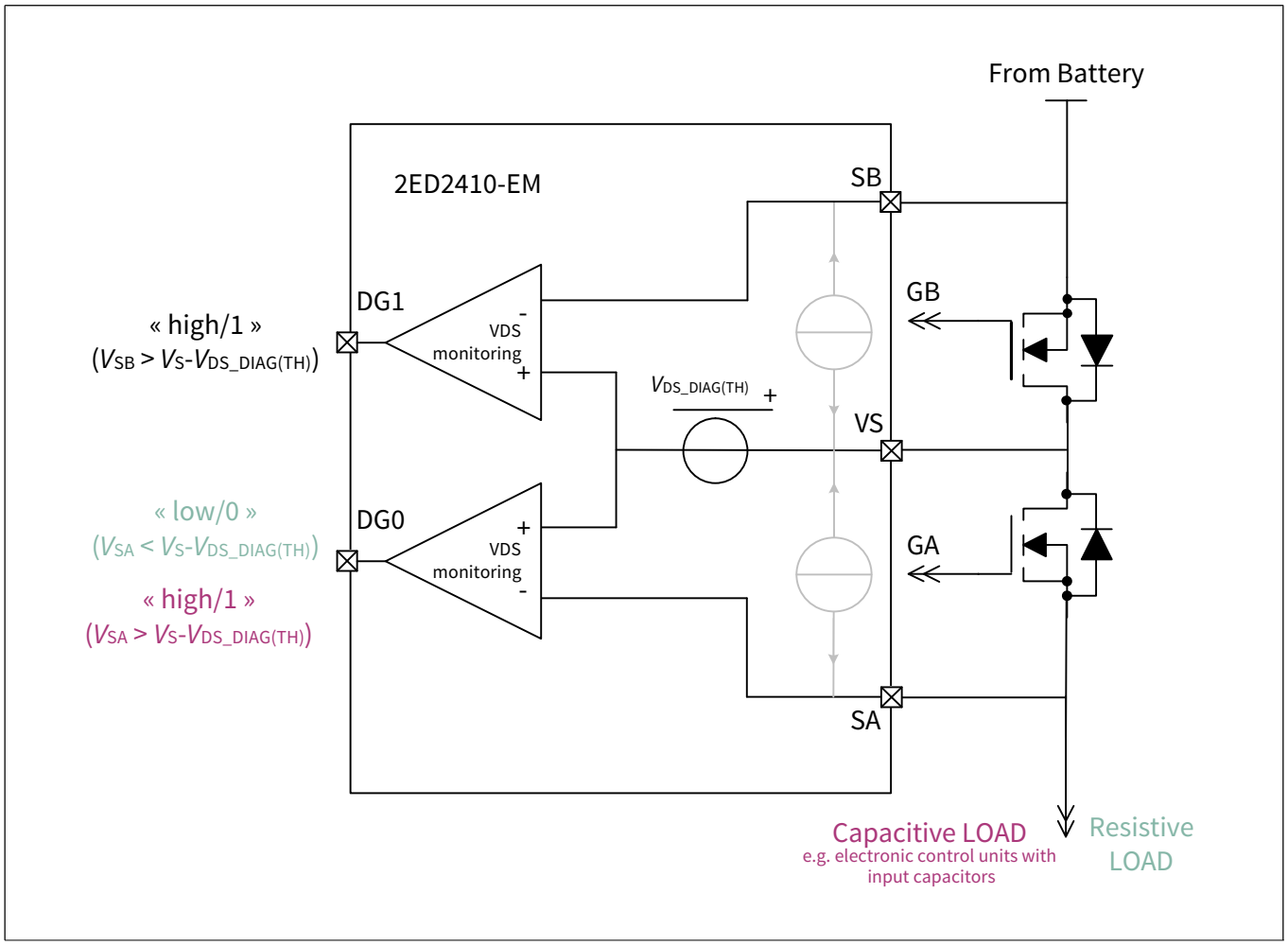


Figure 14 VDS monitoring diagram with example

VDS monitoring allows to detect various situations depending on the switch positions in the boardnet.

It depends on the application.

A non-exhaustive list of possible switch position in the boardnet and situation are described below:

Case 1: battery - resistive / inductive load configuration

The driver is used to drive the load.

DG1 = high show an open connector / or load is high impedance (HZ) > V_{BAT} / I_{SOURCE}.

DG1 = low shows that the load is still present. To avoid leakage Isource in IDLE mode, SLEEP mode can be used in car park mode.

Case 2: battery - Electronic Control Units (ECU)/capacitive load configuration

The driver is used to separate a power-net which is without power supply from the main power-net with power supply. DG1 = high shows that all ECUs input capacitors are charged and that there is no leakage.

DG1 = low shows that ECUs input capacitors are charging with I_{SOURCE} or that there is a leakage.

Case 3: battery - battery configuration

The driver is used to connect two power-nets where both power-nets have their power supply.

DG1 = high shows that $V_{BAT(A)} - V_{BAT(B)} < V_{DS\_DIAG(TH)}$.

DG1 = low shows that $V_{BAT(A)} - V_{BAT(B)} > V_{DS\_DIAG(TH)}$.

A very high current may flow when reconnecting and trigger SAFESTATE. Inductances between batteries must be carefully considered, including ground path.

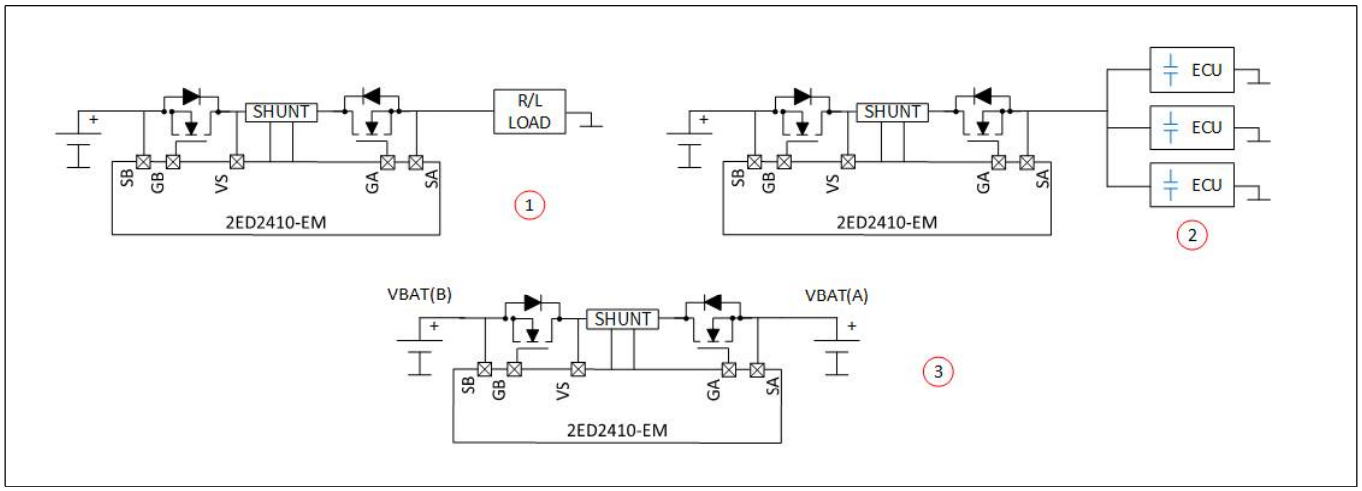


Figure 15 Cases 1, 2, 3

7.2 Current senses in ON and SAFESTATE modes

2ED2410-EM features two integrated current sense amplifiers (active in ON and SAFESTATE modes).

These **current sense amplifiers CSA1 and CSA2** are implemented with two identical differential amplifiers with a wide adjustable gain (*G*) (see PRQ-317).

The inputs are ISP1/2 and ISN1/2 pins and the outputs are CSO1/2 pin.

The current sensors must have a high-side position, or be positioned between the MOSFET drains in a back-to-back common drain configuration.

The current sense amplifier allows to monitor the currents flowing into the shunt (or MOSFET) in **both** directions, which is referred to as bidirectional current sensing.

The gain is set with external resistors $R_{ISP1/2} = R_{ISN1/2}$ on input (on sensor side) and $R_{CSO1/2}$ on output (on microcontroller/connector side). R_{ISP} and R_{ISN} can be different if a different gain is necessary depending of the current direction. On CSA1, this difference in gain will also impact the short-circuit protection which can be higher or lower depending on the gain magnitude.

Resistor values can be adjusted based on the customer's current sensor solution.

The output is an analog voltage signal, $V_{CSO1/2}$, which represents the current flowing in the current sensor. It can be directly read on pin CSO1/2 (Current Sense Output) by a microcontroller. $V_{CSO1/2}$ output voltage varies from 0 V to V_{EN}, in both directions, allowing better accuracy than current sensors using an offset as middle point for zero current.

The information of current direction is available only for **CSA1** and can be read in ON mode directly on pin DG1 (0 if current direction is from ISN1 to ISP1, 1 otherwise) by a microcontroller.

CSA1 features an integrated comparator for fast short-circuit protection. See Chapter 8.1.

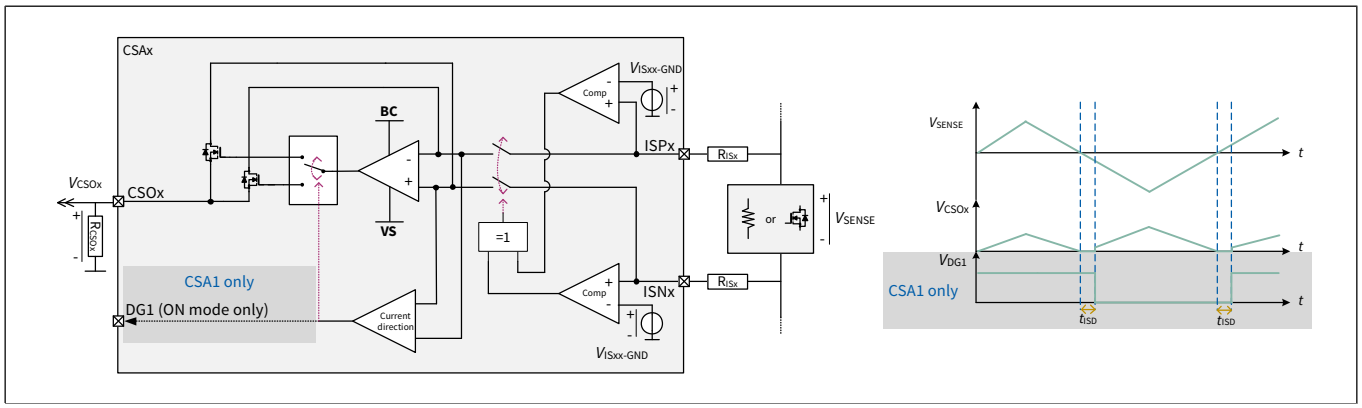


Figure 16 Current sense measurement principle and timing diagram [not to scale]

The amplifiers are supplied between BC and VS. If the V_{BC}-V_S voltage is below or above its functional range (see PRQ-339), the amplifiers input switches will open. As a result the current sense function is ensured and random reconnection can connect unwanted SAFESTATE.

The gain of the current sense amplifiers is configurable by three external resistors (R_{CSO}, 2 x R_{IS}).

The relationship between V_{SENSE} and V_{CSO} through the current sense amplifier is given by:

$$V_{CSO} = |V_{SENSE}| \times \frac{R_{CSO}}{R_{IS}} \quad (1)$$

Where the gain is set by:

$$G_{CSO} = \frac{R_{CSO}}{R_{IS}} \quad (2)$$

Special care has to be taken when setting the gain and the parameters G_{CSO} and R_{CSO} must be observed. Resistors are recommended with at least 1% precision and should be placed as close as possible to the 2ED2410-EM pins. See application note "Getting started with 2ED2410-EM" for a complete description on how to use the current sense amplifiers.

If not used, CSA1 or CSA2, or both, can be simply disconnected with the following configuration. One of the two input pins, either ISP or ISN needs to be connected close to GND (see PRQ-340).

This will reduce the driver self-consumption in ON and SAFESTATE modes.

Warning: short-circuit protection with internal comparator on CSA1 will also be disabled if CSA1 is disabled.

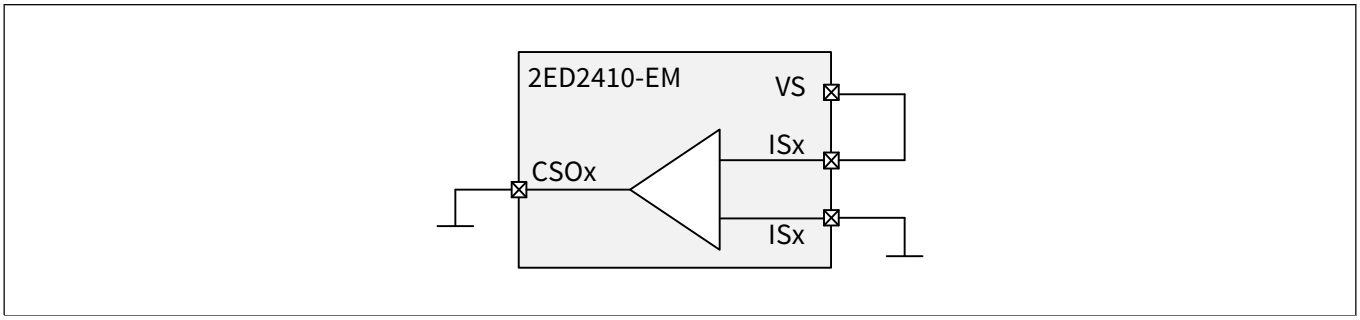


Figure 17 CSA1 & 2 disconnection configuration

7.3 Temperature measurement amplifier in ON and SAFESTATE modes

2ED2410-EM features an integrated temperature monitoring amplifier **TMPA** (active in ON and SAFESTATE modes).

This **temperature monitoring** function is implemented with a differential amplifier.

The input pin is TMP and the output pin is TMPO.

The temperature amplifier allows to monitor the heat flowing into the R_{NTC} by monitoring V_{TMPO} .

The gain is not directly adjustable and the ratio k_{TMP} is kept constant by the driver auto-adjusting the gain.

The ratio is kept with the R_{NTC} in input and R_{TMPO} in output. Resistor values can be adjusted based on customer's thermistor solution.

In the present document, the temperature sensor is referred to as "R_{NTC}" but other sensors, such as PTC or other thermistors can be implemented.

The output is an analog voltage signal: V_{TMPO} represents the temperature in the R_{NTC}. It can be directly read on pin TMPO (Temperature Output) by a microcontroller. R_{TMP} is not mandatory, but may be needed for linearisation of the output signal V_{TMPO}, depending on the thermistor solution choice.

Finally, TMPA can also be disabled if not used. TMP and TMPO pins can be left open.

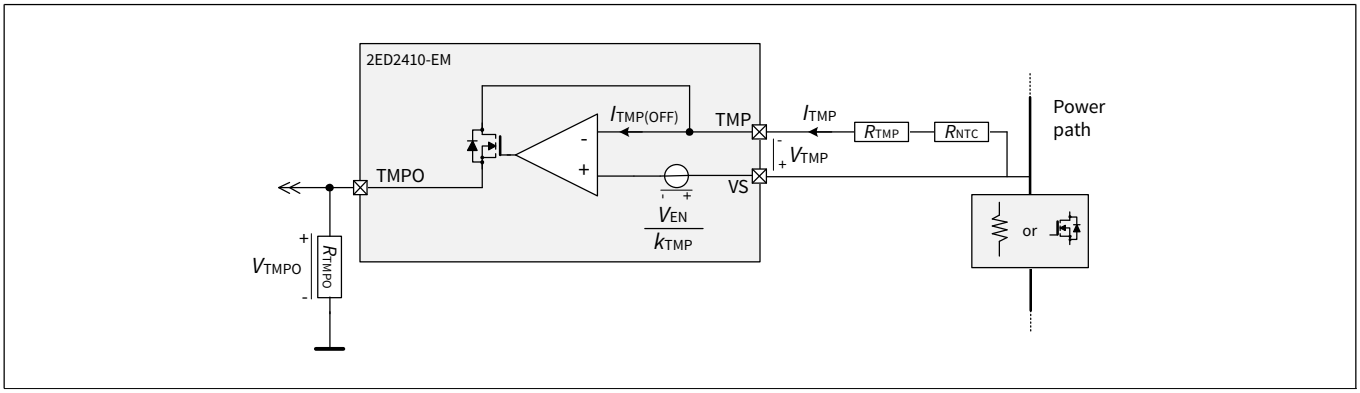


Figure 18 Temperature measurement diagram

The ratio k_{TMP} is defined as follows according to the Figure 18.

$$k_{TMP} = \frac{V_{EN}}{V_{TMP}} \tag{3}$$

8 Protections features in ON mode

8.1 Short-circuit protection

CSA1 has a fast comparator on its output CSO1, which allows 2ED2410-EM to enter SAFESTATE mode when V_{CSO1} reaches $V_{CSO(TH)} = k_{CSO} \times V_{EN}$.

This allows fast turn-off delay time in case of overcurrent/short-circuit when CSA1 is used. 2ED2410-EM is able to switch off the MOSFET without the microcontroller.

The turn-off delay time is $t_{DSCG(L)}$ and can be computed by the sum $t_{DSCCSO1(H)} + t_{DCSO1(H)INT(L)} + t_{DINT(L)G(L)}$. However, the maximum of $t_{DSCG(L)}$ is not the sum of the maximum of the other delays, because by construction, the silicon process and variation make such a case impossible. This is why only the maximum of $t_{DSCG(L)}$ (PRQ-330) should be considered when considering the worst case turn-off delay in case of short-circuit detection by CSA1 comparator.

See Chapter 5.1 for details on diagnostics in SAFESTATE mode.

Once in SAFESTATE mode, the driver needs to be reset.

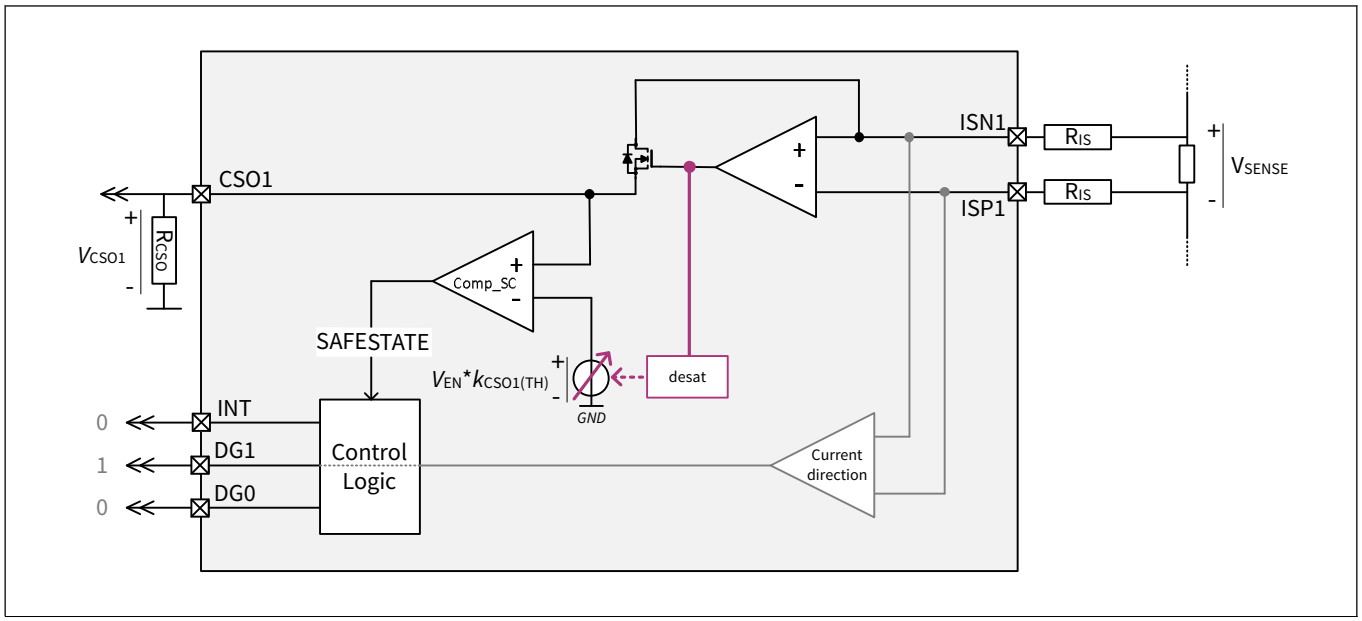


Figure 19 CSA1, internal comparator and diagnostics (one amplifier direction represented for simplicity)

The nominal voltage range for short-circuit protection is $V_{S(NOR)}$. As represented in the graph in Figure 20, in the $V_{S(SC)LOW}$ range (PRQ-40), 2ED2410-EM keeps operating if already in ON or IDLE mode. In the $V_{S(SC)LOW}$ range the short-circuit detection and shutdown are operational and 2ED2410-EM is protected but the $V_{CSO(TH)}$ parameter, hence the short-circuit detection depends on V_S and V_{EN}. A dedicated function named DESAT covers the protection threshold in the $V_{S(SC)LOW}$ range.

The variation of $V_{CSO(TH)}$ is shown in the following graphs.

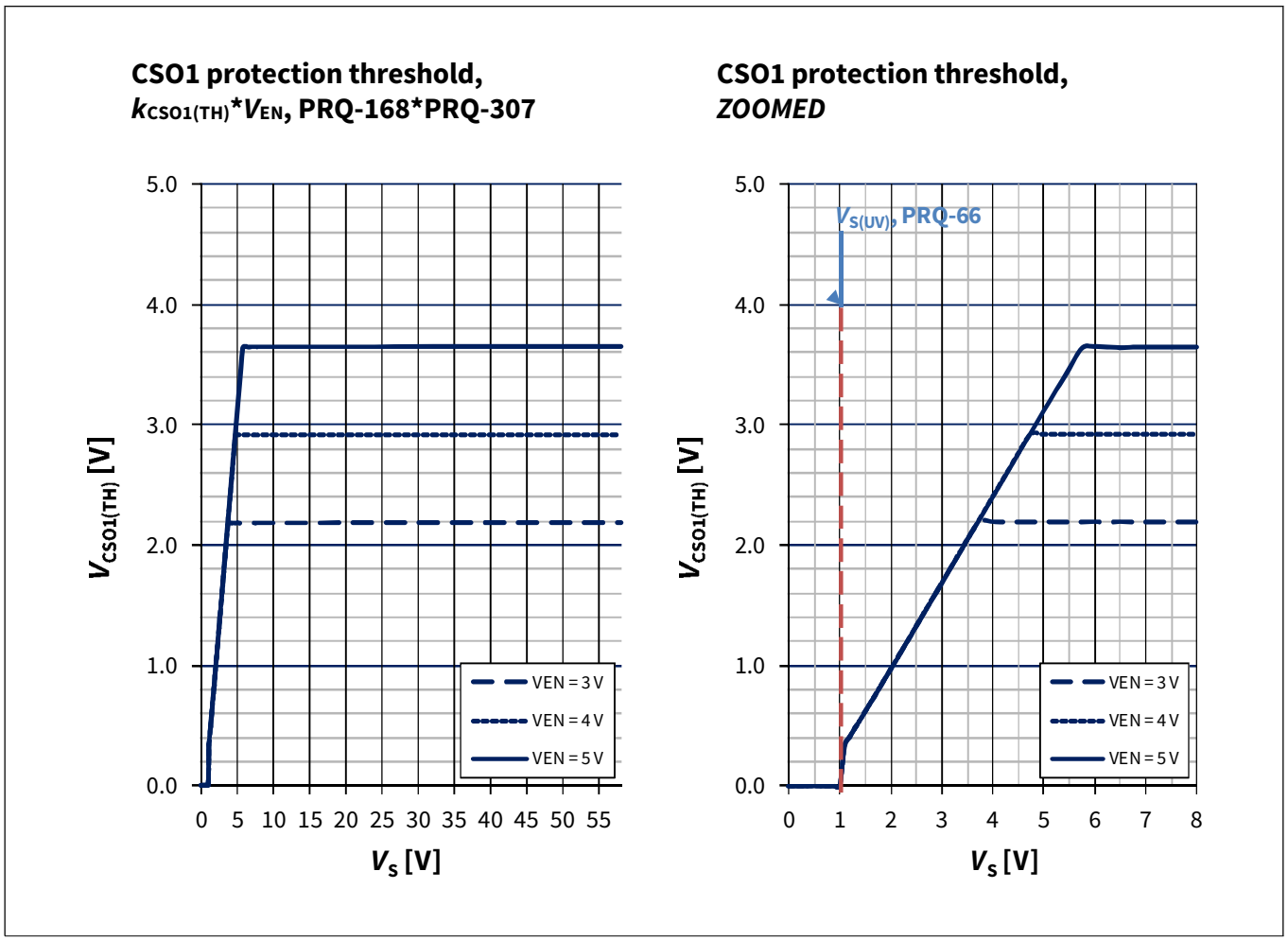


Figure 20 **Typical $V_{CSO1(TH)}$ versus V_S and V_{EN} (independent of T_J)**

8.2 Undervoltage protection on VS

VS pin has an integrated comparator comparing permanently V_S voltage to $V_{S(UV)}$ reference (PRQ-66), which allows 2ED2410-EM to enter SAFESTATE mode when V_S reaches down $V_{S(UV)}$ level.

The turn-off delay time is computed by the sum $t_{DUV(H)INT(L)} + t_{DINT(L)G(L)}$ (PRQ-320, PRQ-136).

This has two consequences:

- The driver is protected down to 0 V on battery, meaning that a very strong short-circuit that would actually bring the voltage on VS node to 0 V is covered and switch is protected.
- The driver could be sensitive to micro-cuts on the supply if the micro-interruptions are longer than $t_{DUV(H)INT(L)}$. To overcome this effect, a capacitor can be used next to VS pin (e.g. a few micro-farad). Additionally, if large micro-cuts are expected in the application, ENABLE pin can be connected to VS pin directly through a 100kΩ (or more) resistor. An additional Zener diode is necessary on the ENABLE pin to limit the voltage to the desired value, e.g. 3.3 V or 5 V. When the micro-interruption is over, the driver will automatically turn-on again as soon as $V_{EN(H)}$ (PRQ-74) threshold is reached again on the ENABLE pin.

See Chapter 5.1 for details on diagnostics in SAFESTATE mode.

Once in SAFESTATE mode, the driver needs to be reset.

The figure below shows the diagram, (1), the normal driver configuration, and (2), a possible adapted configuration with external circuitry for connection of the ENABLE pin to VS which will reset the driver automatically in case of a large micro-interruption.

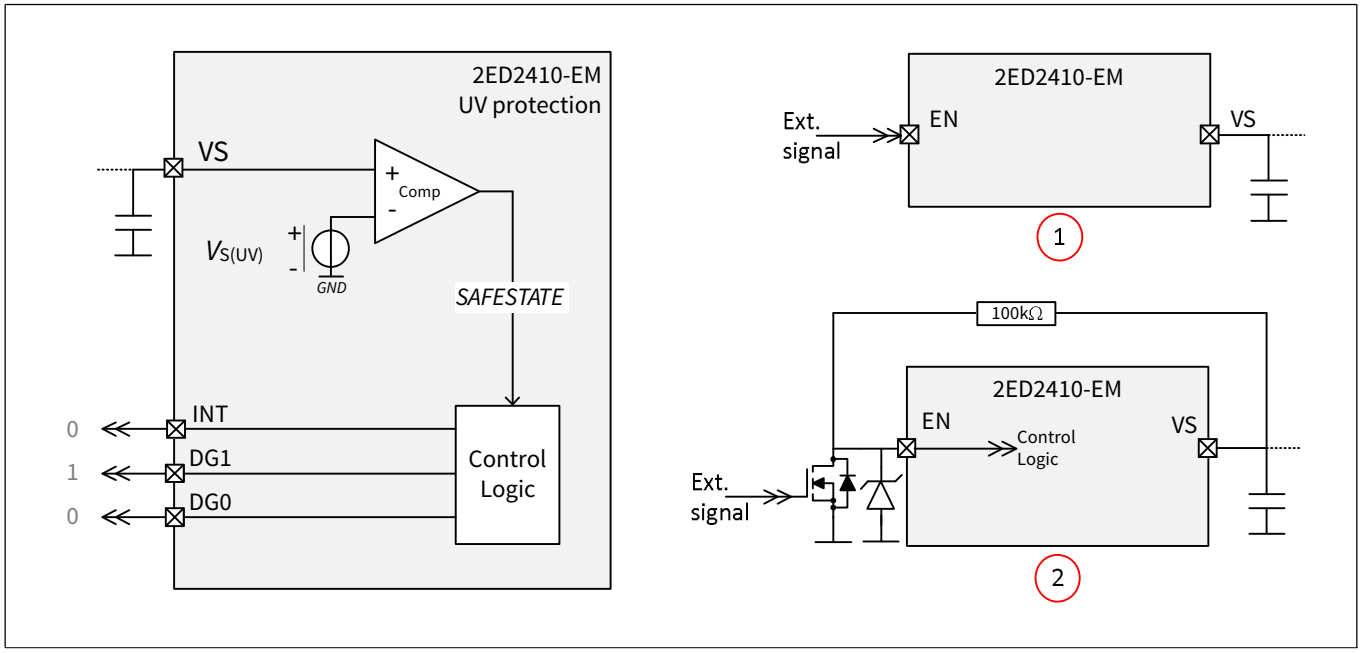


Figure 21 $V_{S(UV)}$ protection diagram and possible driver configuration

8.3 Custom protections with comparator

2ED2410-EM features a voltage comparator with inputs CPP and CPN.

This comparator can be used to trigger SAFESTATE mode based on any analog voltage, even a voltage external to 2ED2410-EM.

CPP is the positive input of the comparator and CPN is the negative input.

V_{CPREF} can be adjusted by microcontroller, or fixed by an on-board power supply chip, such as an Infineon SBC, or a simple voltage divider, within the limits $V_{CP(REF)}$ for stability.

Using this comparator allows 2ED2410-EM to enter SAFESTATE and turn-off MOSFET independently from the microcontroller. The comparator reacts with a delay time $t_{DCP(H)INT(L)}$. Consequently the turn-off delay time in case of shutdown by comparator CP can be computed by the sum $t_{DCP(H)INT(L)} + t_{DINT(L)G(L)}$.

When SAFESTATE mode is triggered, digital outputs {DG0;DG1} will feedback {1;1}. See Chapter 5.1. Once in SAFESTATE, driver needs to be reset.

Below are illustrated 4 possible use cases, and more are possible:

Case 1: overtemperature protection using TMPO output.

Case 2: I-t wire protection using RC. Both limits, short-reaction time and long-time direct current are adjustable dynamically (e.g. a microcontroller PWM output) with V_{EN} and V_{CPREF} respectively.

Case 3: protection using any external signal. The $V_{CP(REF)}$ can be dynamically adjusted by microcontroller. For example, for battery switch application, the current feedback from BMS can be used to trigger the SAFESTATE mode.

Case 4: undervoltage protection by monitoring VS with simple voltage divider.

Note: this custom protection is available together with the short-circuit comparator on CSA1 output.

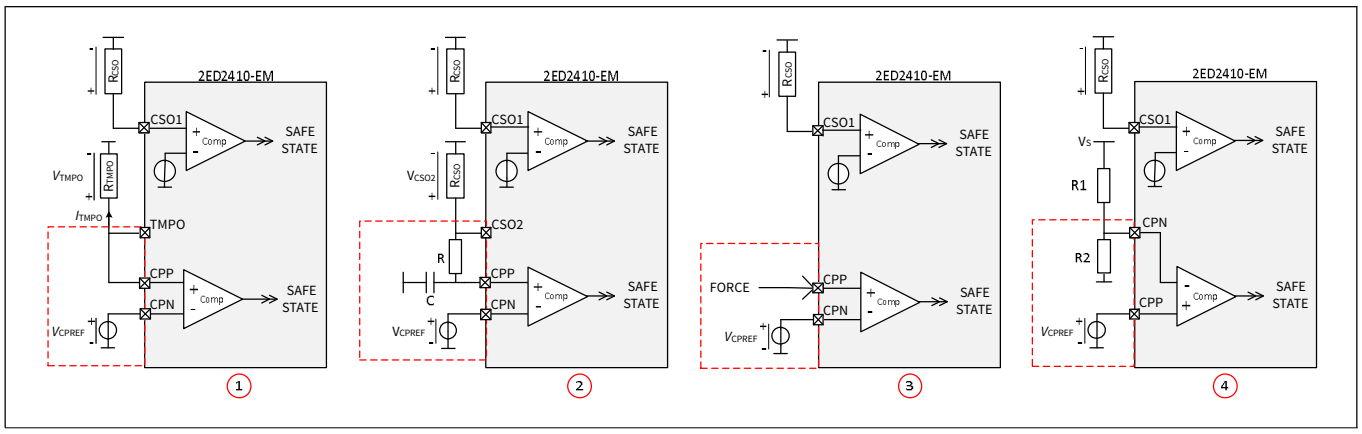


Figure 22 Comparator use cases examples

8.4 Gate undervoltage lock-out protection

The purpose of the gate undervoltage lock-out protection **UVLO** is to avoid to drive MOSFET in linear mode due to a leakage on boost converter output or MOSFET gates.

If V_{BC} - V_S < UVLO in ON mode, the driver enters SAFESTATE mode.

UVLO protection function is activated in ON mode, if at least V_{BC} - V_S has satisfied the condition V_{BC} - V_S > $V_{BC(TH)}$ at least once in ON mode.

If V_{BC} - V_S < UVLO in ON mode and $V_{BC(TH)}$ has not been reached once in ON mode, the device does not enter SAFESTATE mode because UVLO is not activated, but **gates do not turn on.**

As a result this situation can be detected by INT = 1 and DG0 displaying the maximum frequency of the boost converter, given the implemented boost converter external components. Once in SAFESTATE, driver needs to be reset.

8.5 Reset of SAFESTATE

2ED2410-EM has one way to actively reset the SAFESTATE: the voltage on EN pin needs to be pulled low for t_{RESET}.

Set V_{EN} < $V_{EN(L)}$ for t_{RESET}, see PRQ-75. See Figure 8 for timing diagram.

Once EN pin is pulled down, INT signal will go up one the driver reaches SLEEP state again.

SLEEP state can be verified by DG0 = DG1 = low.

2ED2410-EM can move back to IDLE mode by EN=high and INA=INB=low.

Note: If INA or INB remain "high" when EN is set "high", the driver will immediately enter ON mode if the condition V_{BC} - V_S ≥ $V_{BC(TH)}$ is satified.

9 Driver supply: boost converter

A **boost DC/DC converter structure** is the supply of 2ED2410-EM.

The diode and the activation switch K1 are implemented in the driver, but the capacitor C_{BC}, the resistor R_{RS} and the inductor L1 have to be added as external components.

The boost converter is active in IDLE mode, ON mode, SAFESTATE mode. It is off in SLEEP mode.

The boost converter starts when $V_S \geq V_{S(NOR)}$ and $V_{EN} \geq V_{EN(H)}$ (PRQ-74). Then, once $V_{BC} - V_S \geq V_{BC(TH)}$ (PRQ-139), the boost converter operates normally over the $V_{S(EXT)}$ range. If $V_{EN} \leq V_{EN(L)}$, the driver goes back to SLEEP mode from any of the other three operating modes and the boost converter is stopped.

The switch K1 activation time is reflected on pin DG0 in ON mode.

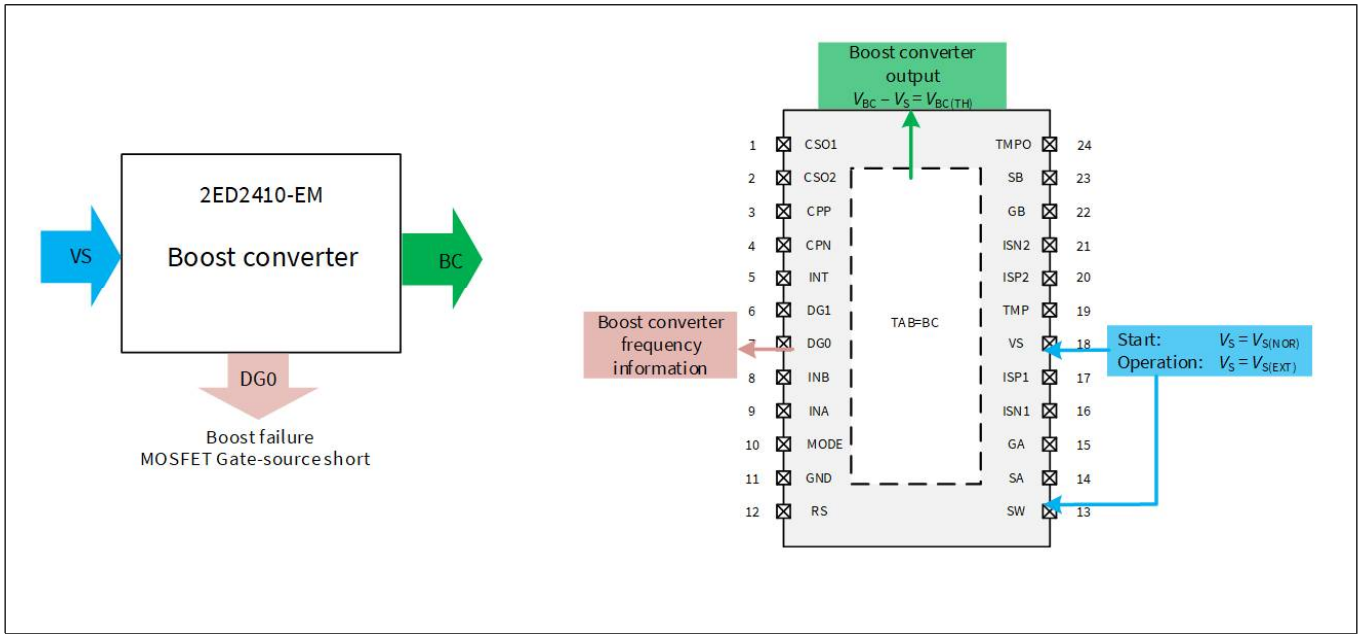


Figure 23 Principle of boost converter as driver supply

The topology of the 2ED2410-EM supply is a boost DC/DC converter working in current mode control.

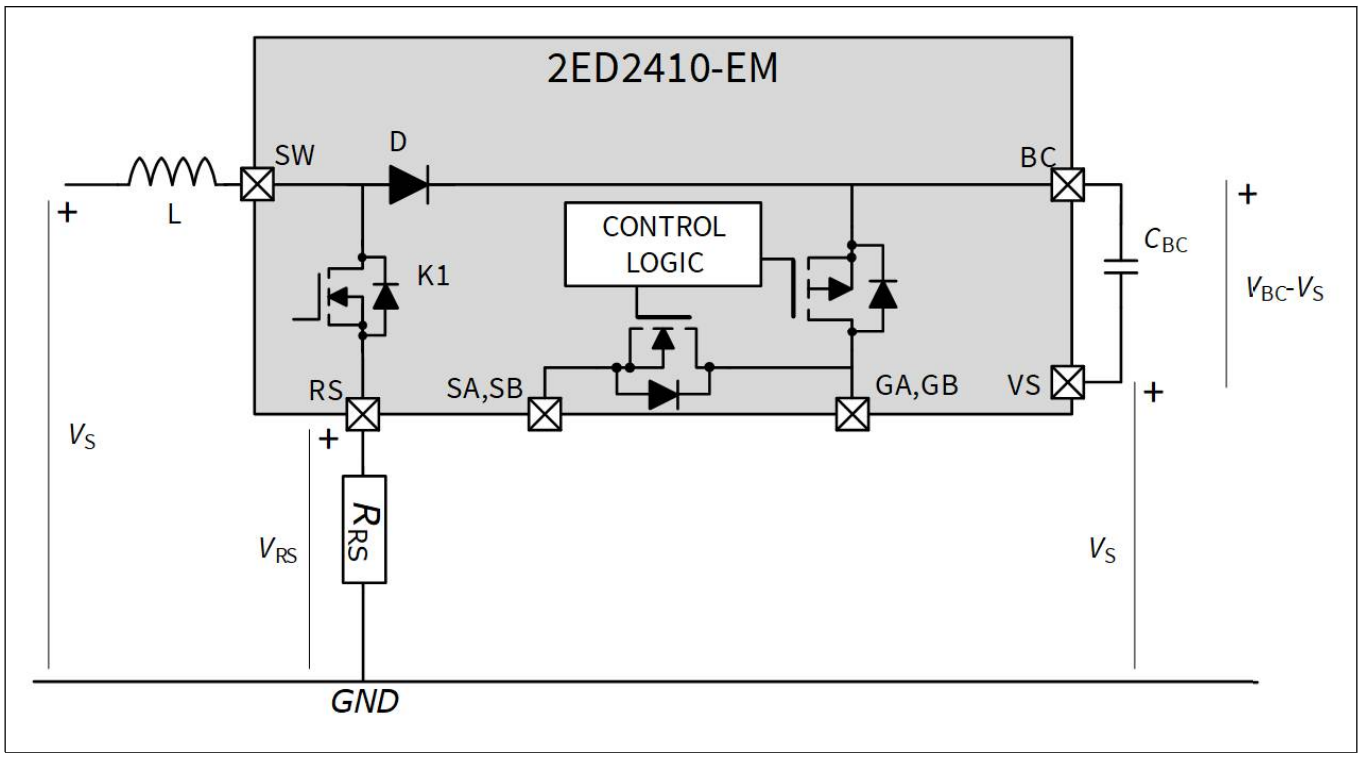


Figure 24 BC topology used as gate supply

Activation:
K1 is an integrated MOSFET, switched on when V_{BC} - V_S < $V_{BC(TH)}$ and V_{RS} < $V_{RS(TH)}$ (PRQ-147).
K1 is turned off when V_{RS} > $V_{RS(TH)}$ or V_{BC} - V_S > $V_{BC(TH)}$.
The inductor charges the C_{BC} capacitor through diode D.
D has a forward voltage drop of V_{FBC} (PRQ-148).

The K1 MOSFET cannot restart during $t_{BC(OFF)}$ (PRQ-152) after $V_{RS(TH)}$ has been reached. This limits the boost converter maximum frequency.

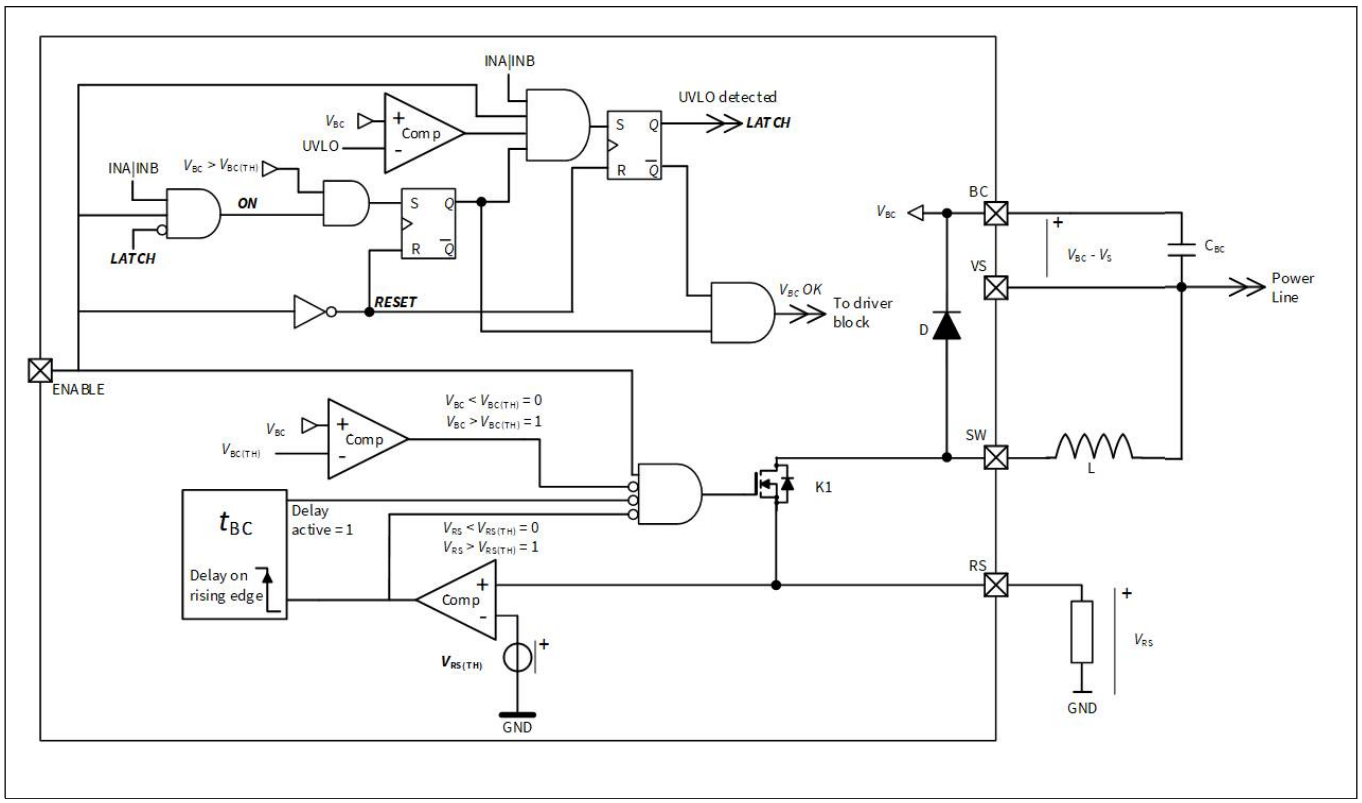


Figure 25 Boost converter control logic

The current in the inductor is limited by the $V_{RS(TH)}$ comparator which monitors the voltage across R_{RS}. Due to the delay in the loop, $t_{D(OFF)K1}$ (PRQ-155), the inductor current exceeds the threshold set by: $V_{RS(TH)}$.

The current waveform in the inductor is not linear, but exponential, because the sum of the resistance of K1, of the parasitic inductor of L1 (R_L), and R_{RS} are not negligible in the K1 short activation timeframe.

The calculations are described in the application note "Getting started with 2ED2410-EM".

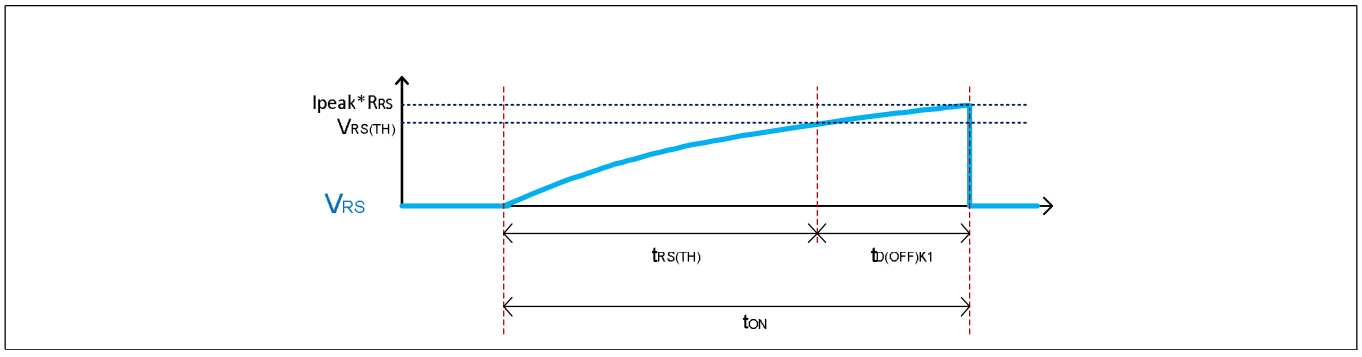


Figure 26 Current peak control

The peak current must not exceed the maximum rating of I_{SW} (PRQ-16).

10 MOSFET connections in application

The next figure shows a few typical connections in which the 2ED2410-EM driver can operate.

Amplifiers CSO1 and/or CSO2 can be disconnected to reduce 2ED2410-EM self-consumption. See Chapter 7.3.

Any custom protection signal can be connected to the additional comparator regardless of the power MOSFET structure used, see Chapter 8.3.

See application note "Getting started with 2ED2410-EM" on what to do with non-used pins.

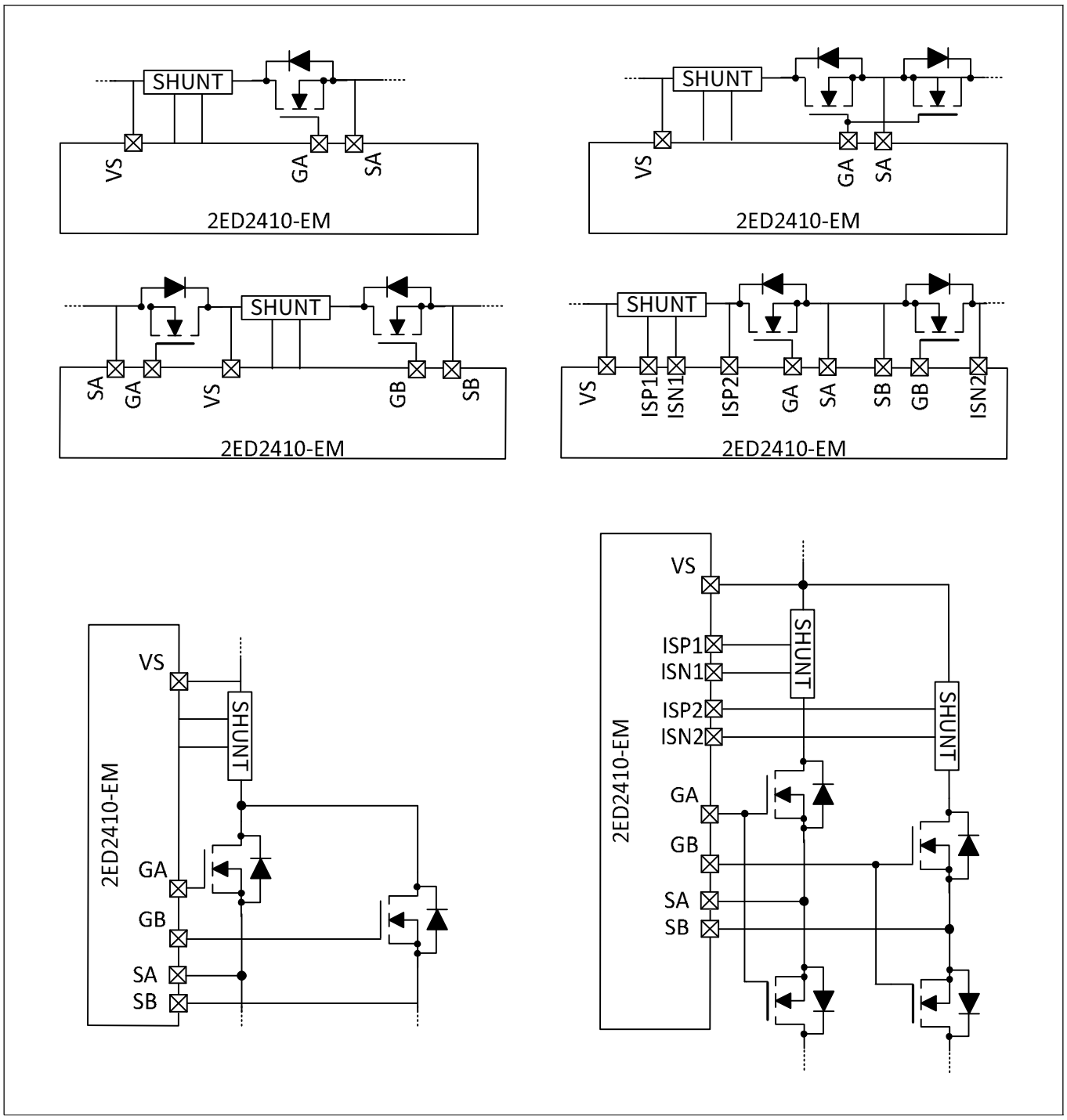


Figure 27 Typical MOSFET and shunt resistor connections

11 Characterization graphs

The graphs shown in this section are measured on typical parts, on a limited number of samples.

The goal is to show the variation of some parameters along the driver's operating voltage range and temperature, or a specific behaviour.

T_J = -40 to 150°C, V_S = 8 V to 36 V (unless otherwise specified), all voltages with respect to ground, typical values are given for V_S = 14 V or/and T_J = 25°C.

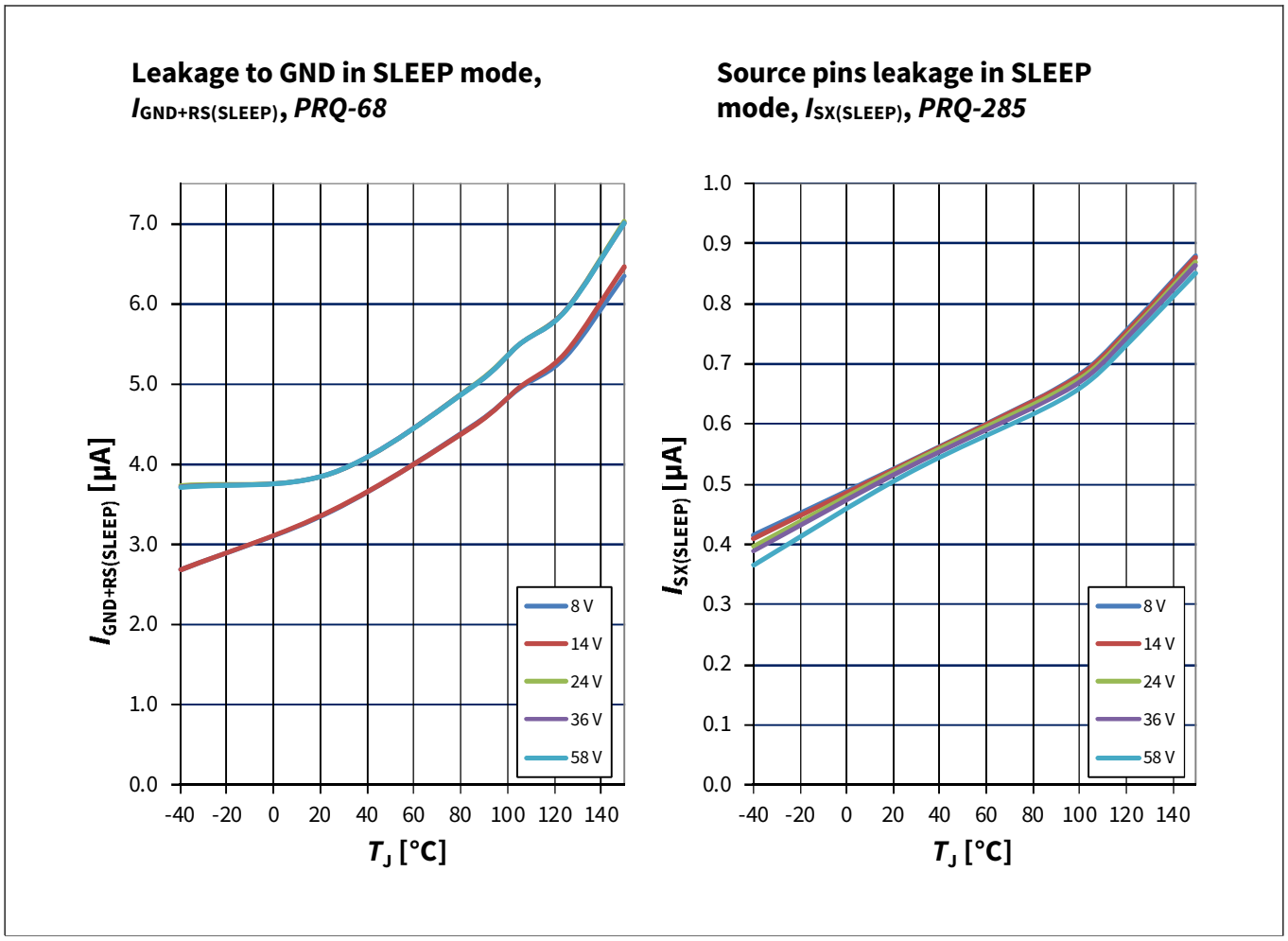
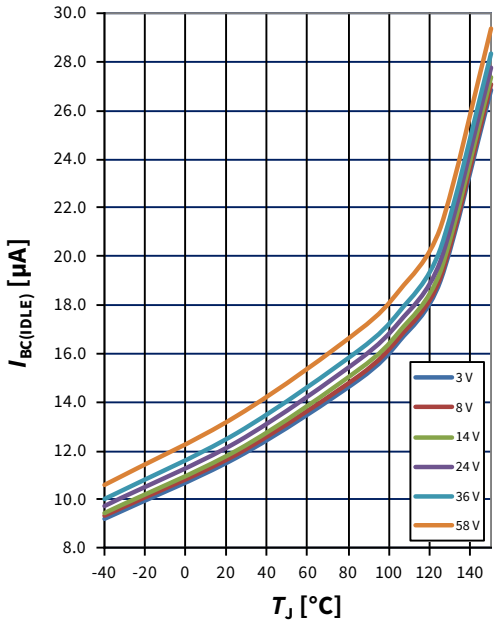
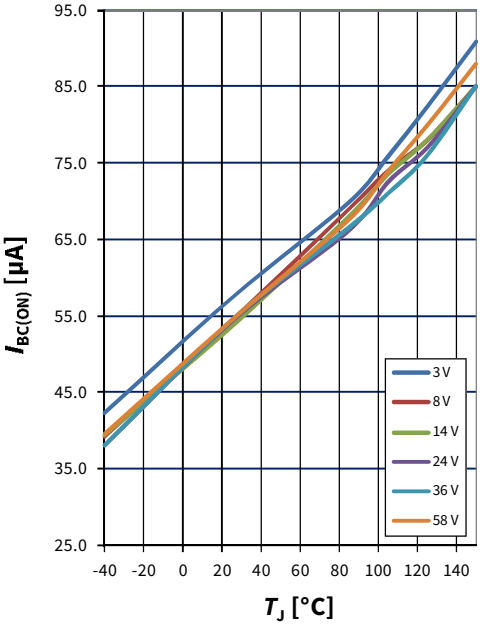


Figure 28 Driver leakage in SLEEP mode

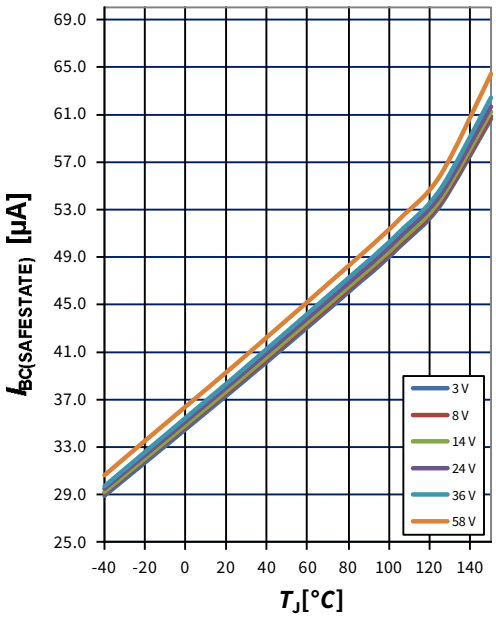
BC current in IDLE mode
$I_{BC(IDLE)}$, PRQ-144



BC current in ON mode
$I_{BC(ON)}$, PRQ-145



BC current in SAFESTATE mode
$I_{BC(SAFESTATE)}$, PRQ-146



BC current in ON mode, 1 CSA off
$I_{BC(ON)\_1CSA(OFF)}$, PRQ-302

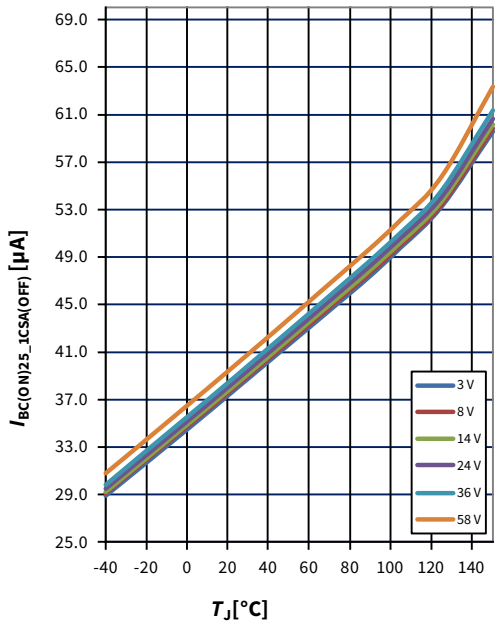
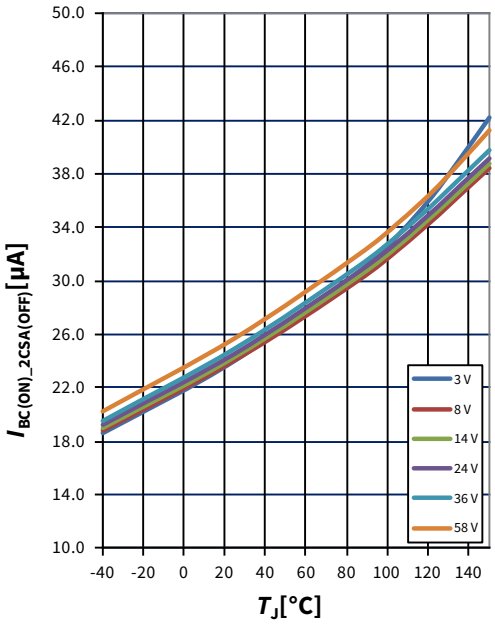
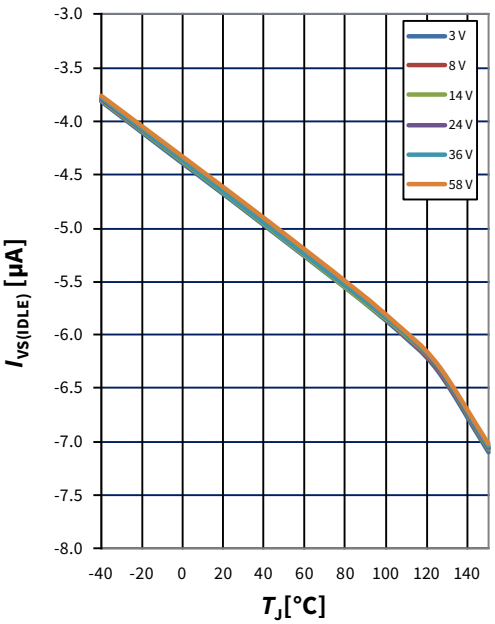


Figure 29 Current consumption

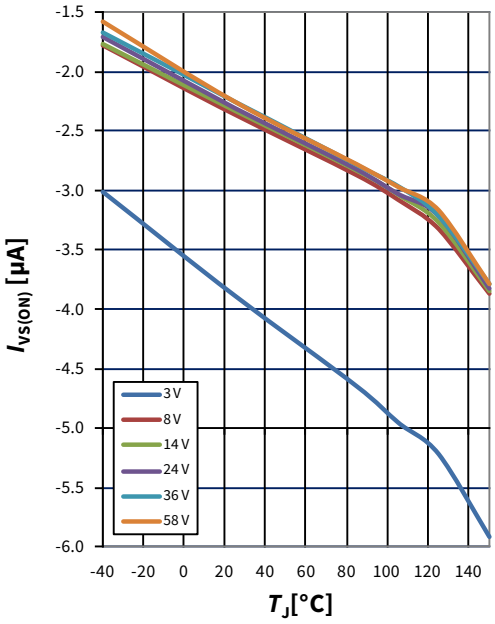
BC current in ON mode, 2 CSA off
$I_{BC(ON)\_2CSA(OFF)}$, PRQ-303



VS current in IDLE mode
$I_{VS(IDLE)}$, PRQ-69



VS current in ON mode
$I_{VS(ON)}$, PRQ-72



VS current in SAFESTATE mode
$I_{VS(SAFESTATE)}$, PRQ-146

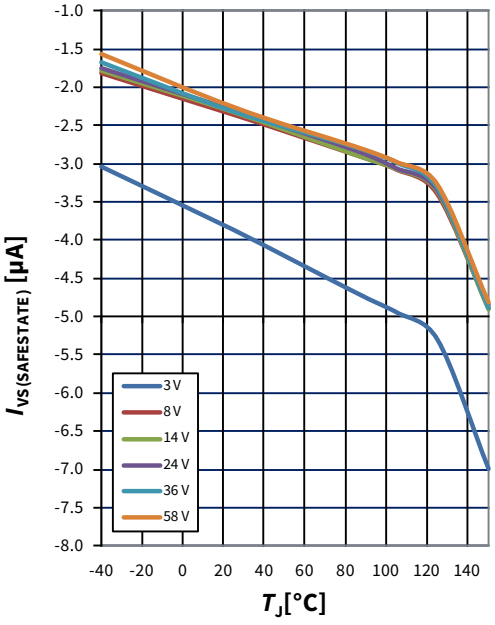
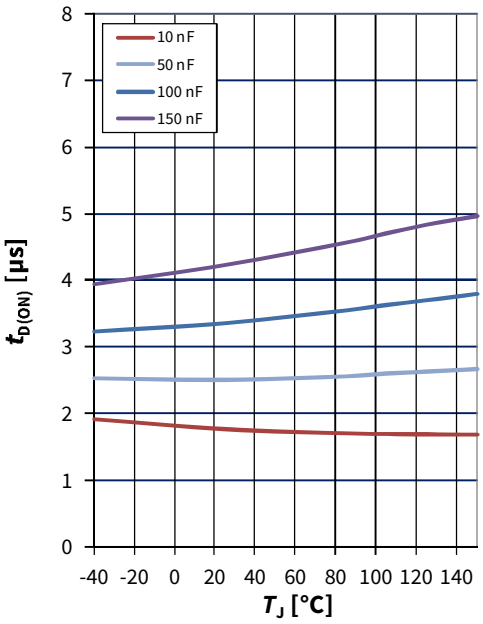
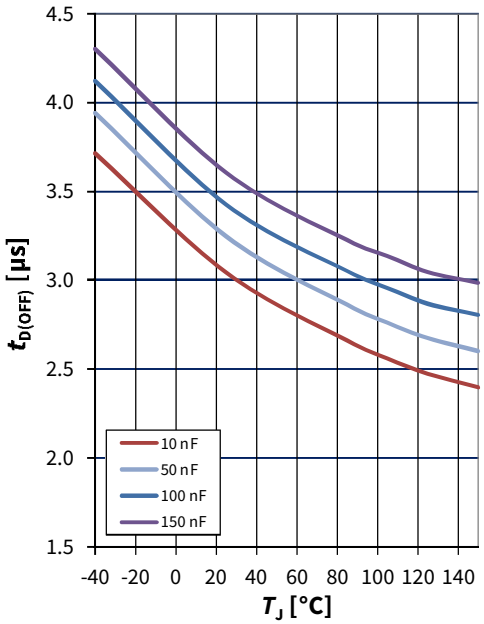


Figure 30 Current consumption continued

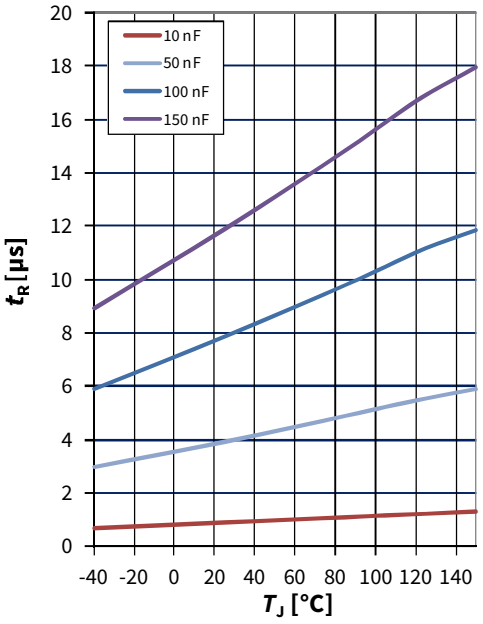
Gate turn-on delay variation with different C_{GS}, $t_{D(ON)}$, PRQ-50



Gate turn-off delay variation with different C_{GS}, $t_{D(OFF)}$, PRQ-53



Gate-source rise time (20% to 80%) with different C_{GS} , t_R, PRQ-51



Gate-source fall time (80% to 20%) with different C_{GS} , t_F, PRQ-54

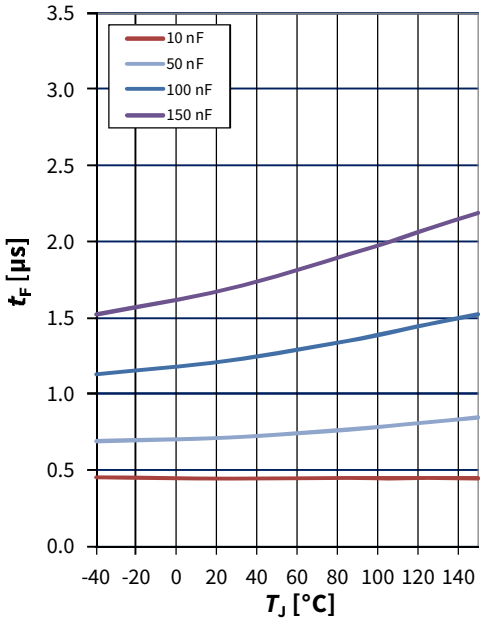


Figure 31 Switching timings (GA or GB)

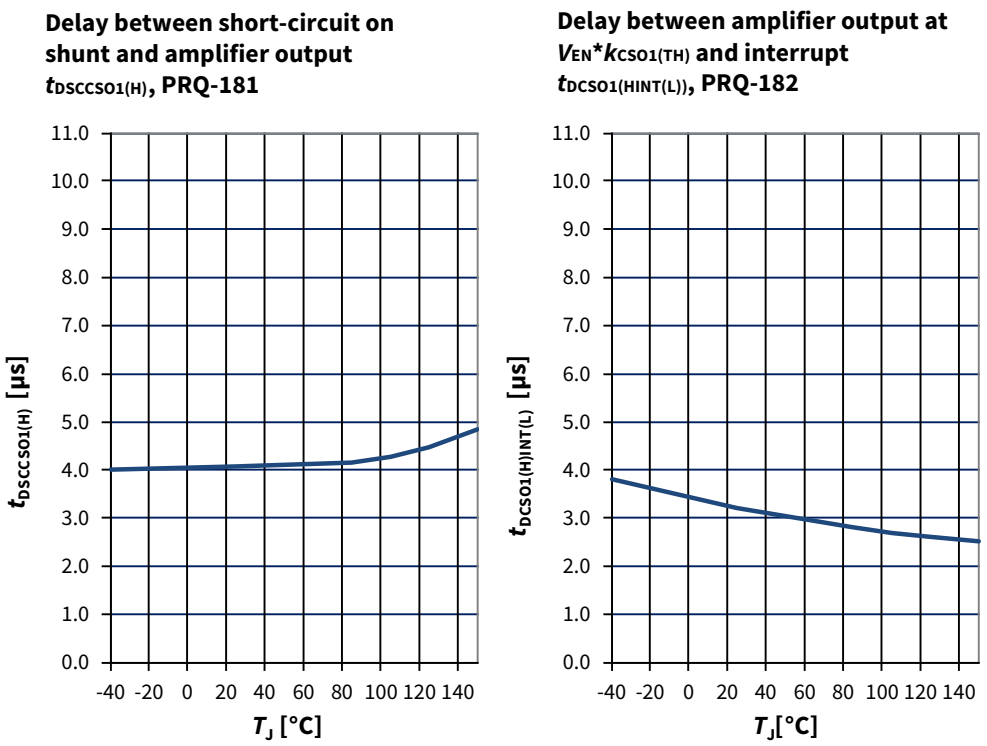
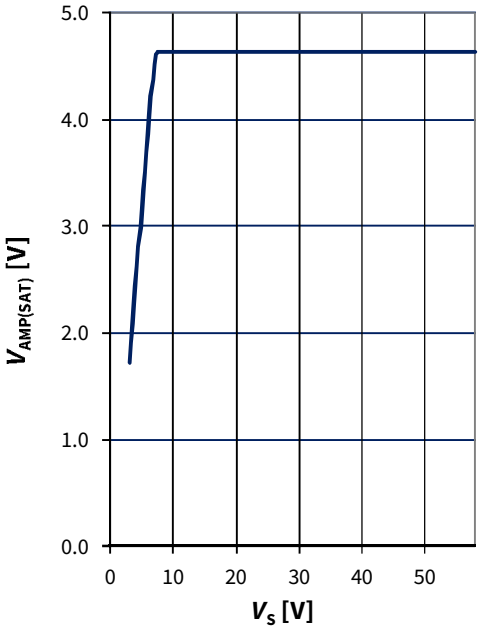
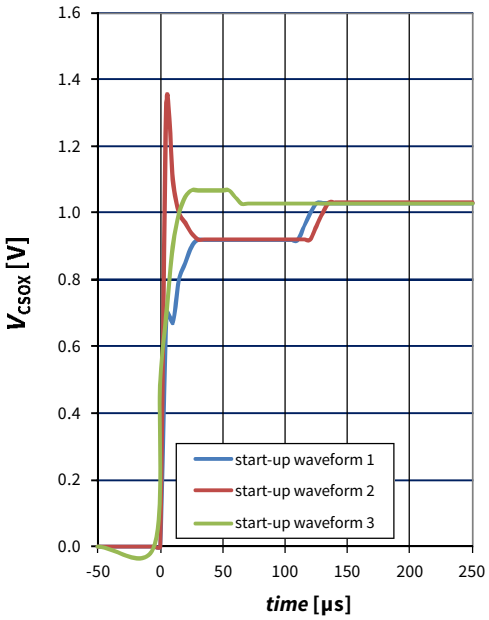


Figure 32 Short-circuit protection timings

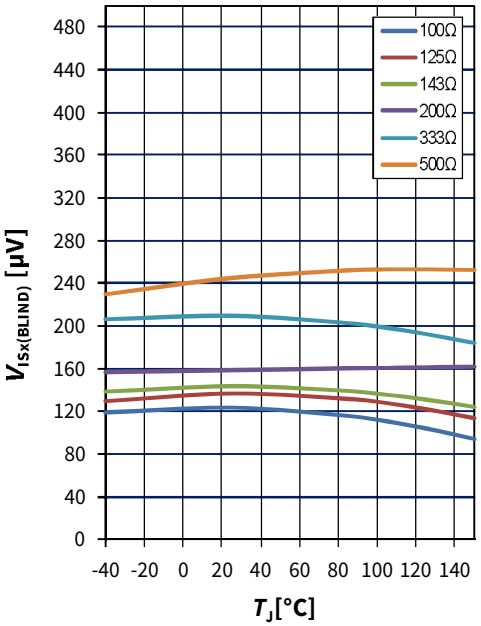
Amplifiers output saturation voltage, $V_{AMP(SAT)}$, PRQ-310



CSA start-up waveforms with $t_{CSA(ACC)}$, PRQ-310



CSA input blind range, $V_{ISx(BLIND)}$, PRQ-324



TMPA input offset, absolute value, $V_{TMP(OFFSET)}$, PRQ-186

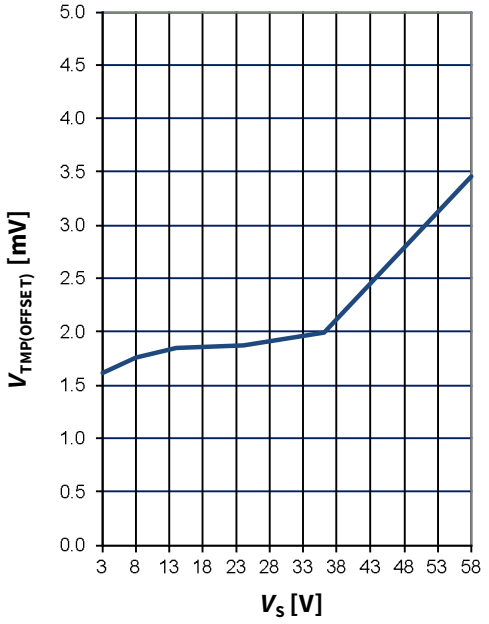


Figure 33 Amplifier characteristics

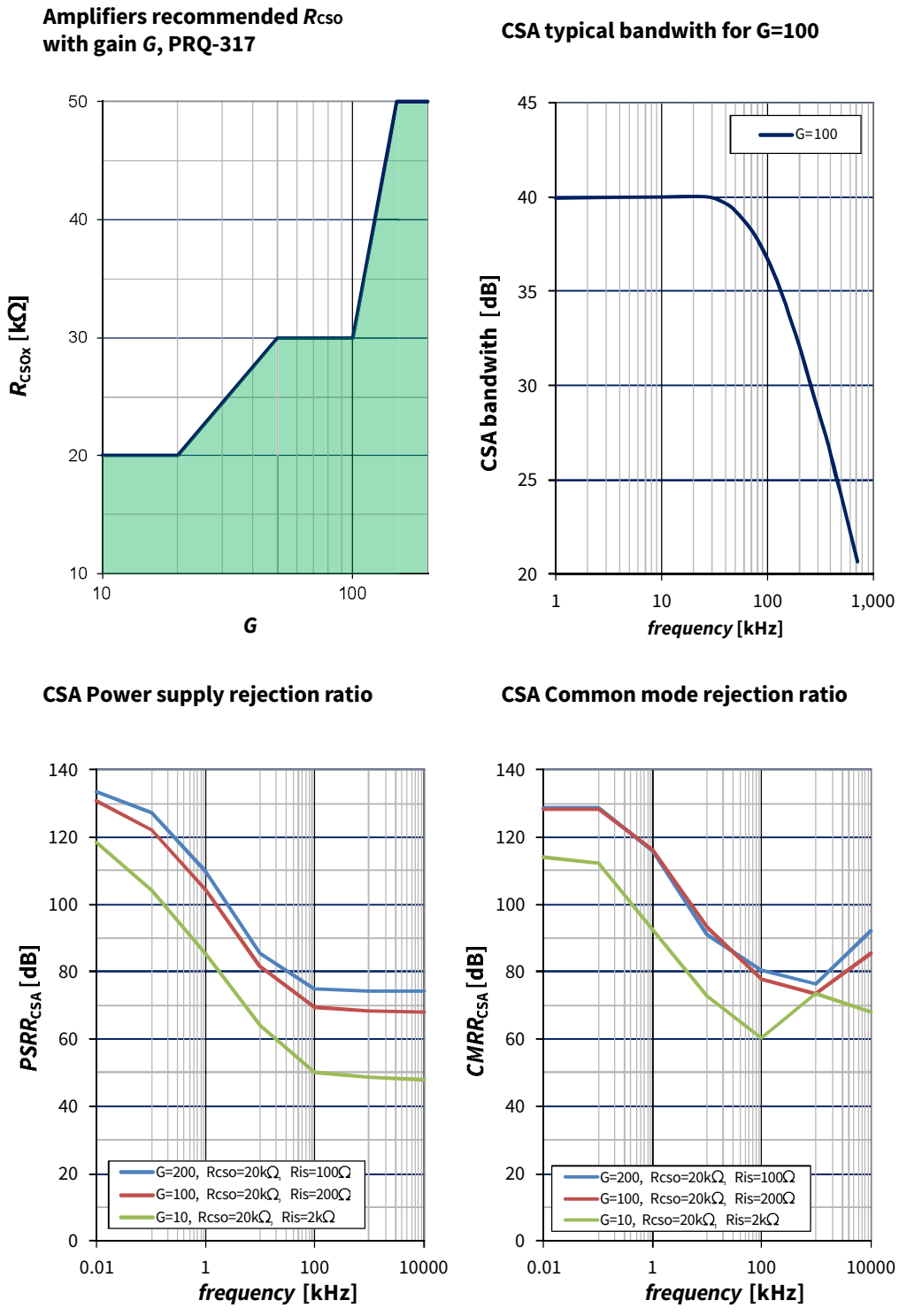
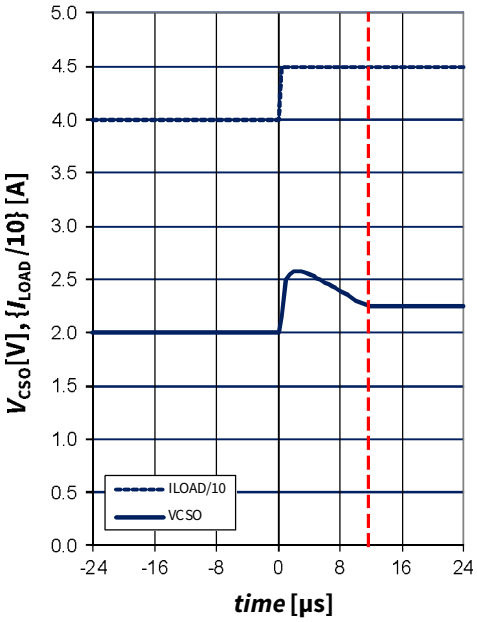
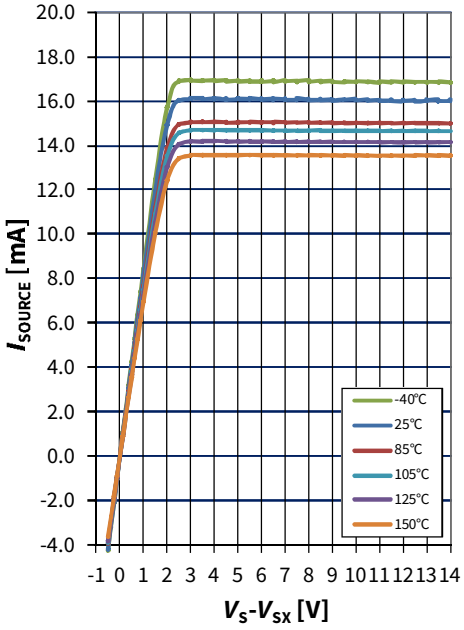


Figure 34 Amplifiers characteristics continued

Amplifiers settling time, di/dt = 7.5A/µs $t_{CSA(SET)}$, PRQ-328



Source current with V_S-V_{Sx} variation, I_{SOURCE}, PRQ-56



CP comparator reaction time, $t_{DCP(H)INT(L)}$, PRQ-184

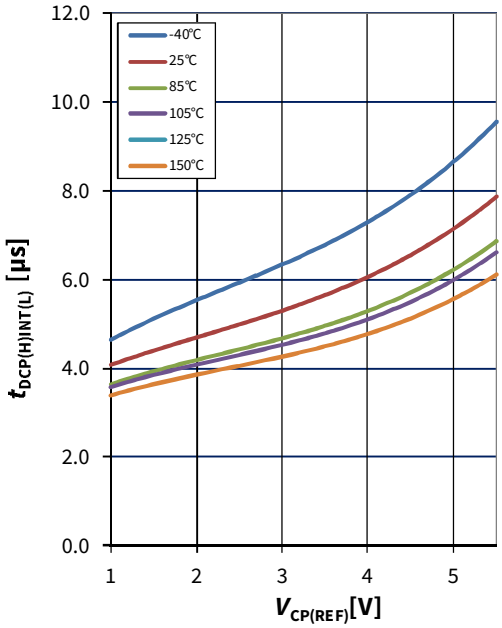


Figure 35 Miscellaneous characteristics

12 Package information

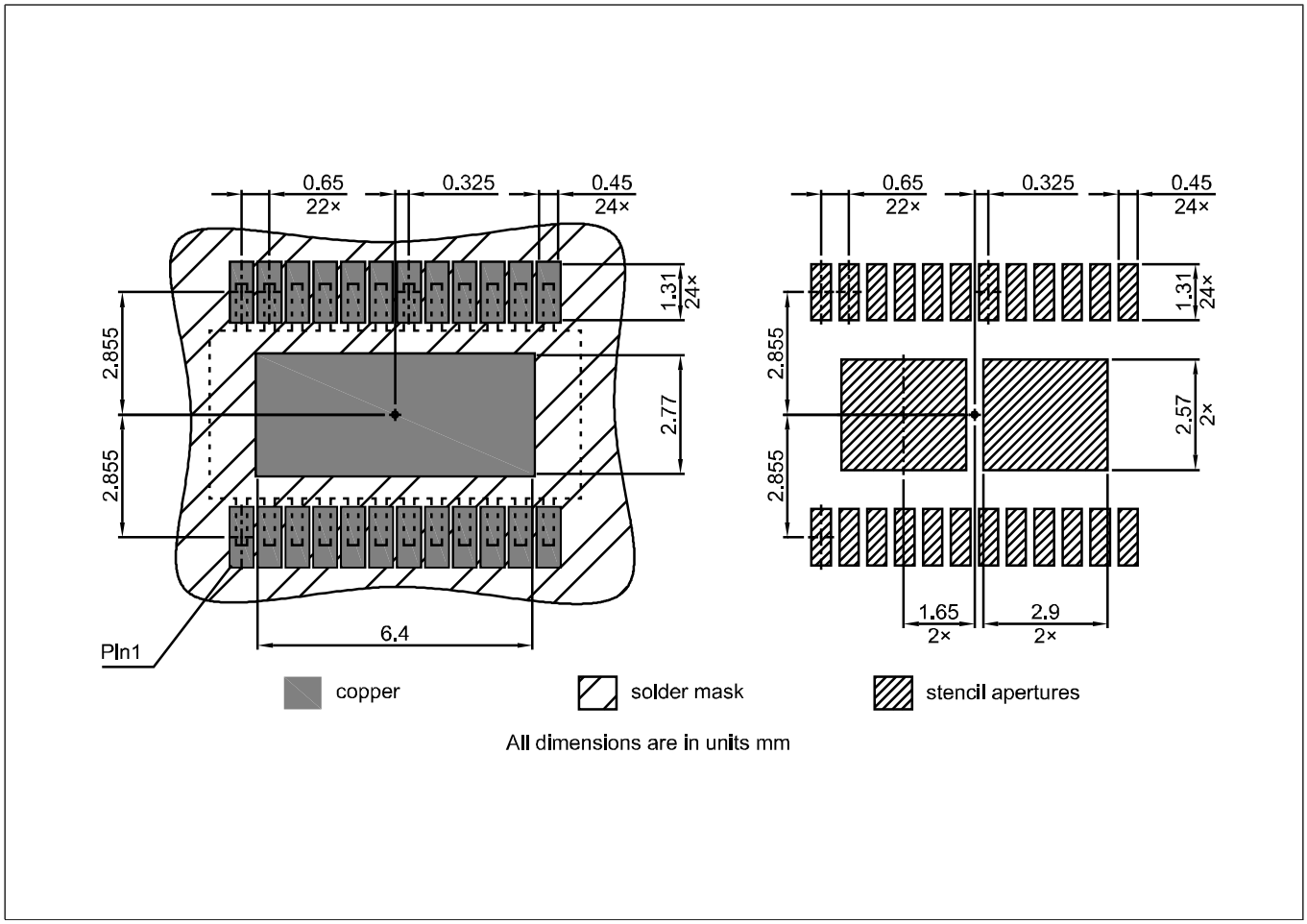


Figure 36 Footprint drawing

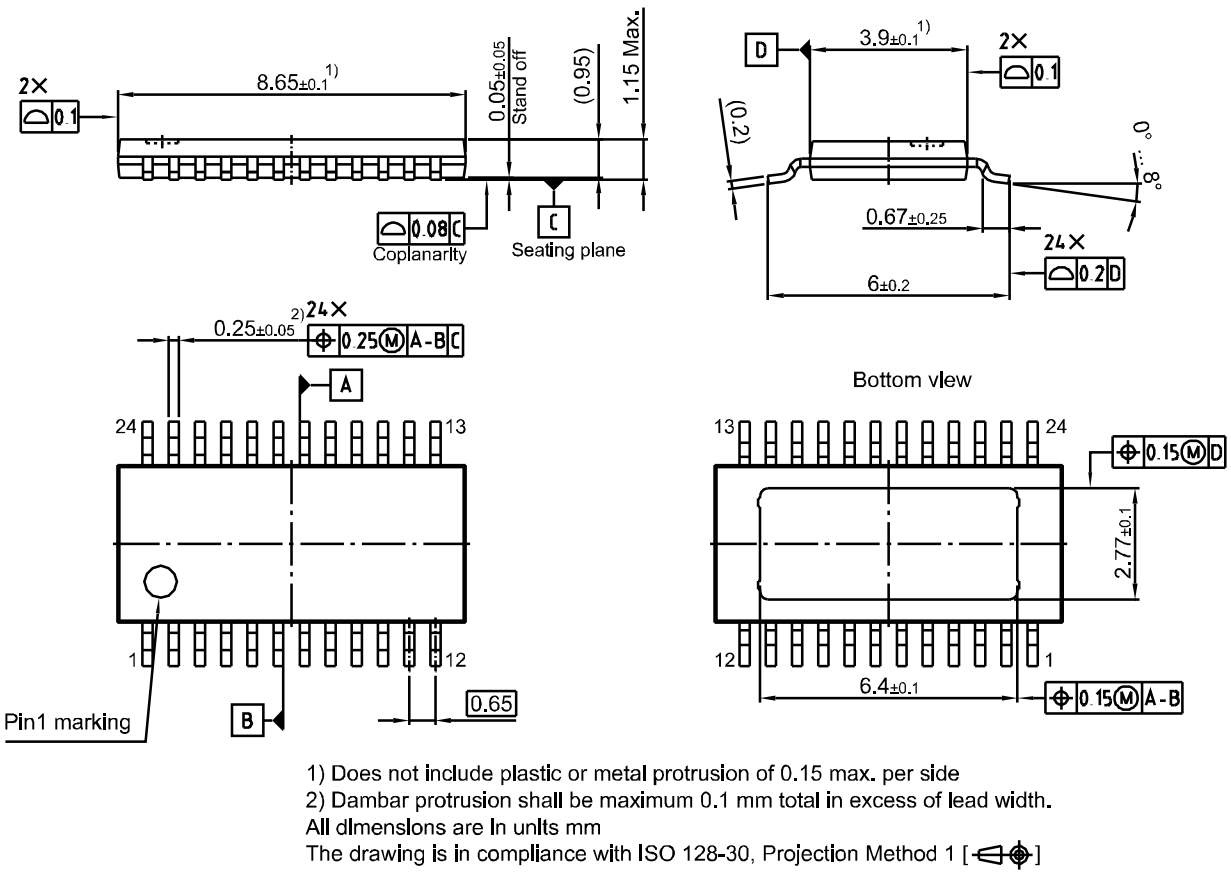


Figure 37 Package outline

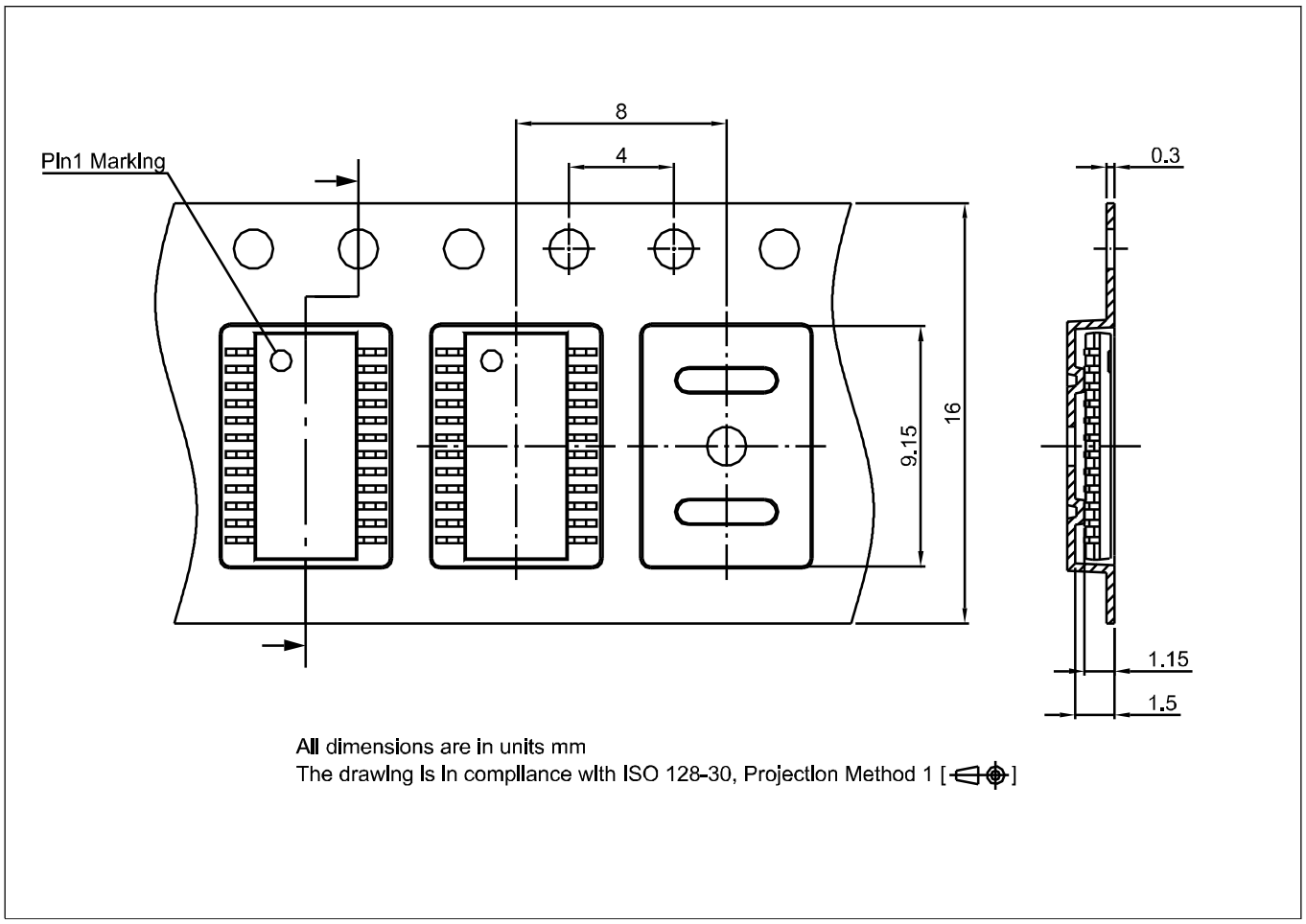


Figure 38 Tape & Reel

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Revision history

Document version	Date of release	Description of changes
Rev. 2.10	2023-01-26	• PRQ-341 added • PRQ-69 lower limit changed from -12µA to -15µA
Rev. 2.00	2022-07-11	• Device released • Footnote added in column “Note or condition“ of PRQ-157, PRQ-336, PRQ-337, PRQ-338 • Footnote added in column “Note or condition” of PRQ-154
Rev. 1.00	2022-05-23	• Datasheet creation during development phase

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PCN 2022-233-A

Functional Safety related PCN: Update of safety application note and data sheet affecting product 2ED2410-EM

Affected products sold to FUTURE ELECTRONICS INC. (4048203)

Sales name	SP number	OPN	Package	Customer part number
2ED2410-EM	SP005072940	2ED2410EMXUMA1	PG-TSDSO-24-5	