



## Product Change Notification / JAON-230QOC341

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### Date:

26-Jan-2023

### Product Category:

Memory

### PCN Type:

Manufacturing Change

### Notification Subject:

CCB 6126 Initial Notice: Qualification of United Microelectronics Corporation - Fab 8D (U08D) as new fabrication site for selected 24LC515, 24AA515, and 24FC515 device families available in 8L SOIJ (.208in) and 8L PDIP (.300in) packages.

### Affected CPNs:

[JAON-230QOC341\\_Affected\\_CPN\\_01262023.pdf](#)

[JAON-230QOC341\\_Affected\\_CPN\\_01262023.csv](#)

### Notification Text:

**PCN Status:**Initial Notification

**PCN Type:**Manufacturing Change

**Microchip Parts Affected:**Please open one of the files found in the Affected CPNs section.

Note: For your convenience Microchip includes identical files in two formats (.pdf and .xls)

**Description of Change:**Qualification of United Microelectronics Corporation - Fab 8D (U08D) as new fabrication site for selected 24LC515, 24AA515, and 24FC515 device families available in 8L SOIJ (.208in) and 8L PDIP (.300in) packages.

### Pre and Post Change Summary:

	Pre Change	Post Change
Fabrication Site	Die # 1: Microchip Technology Tempe – Fab 2 (TMGR)	United Microelectronics Corporation - Fab 8D (U08D)
	Die # 2: Microchip Technology Tempe – Fab 2 (TMGR) or Microchip Technology Gresham – Fab 4 (GRTM)	
Wafer Technology	Die # 1: 121k Technology	66.88k Technology
	Die # 2: 150k Technology	
Wafer Diameter	Die # 1: 8 inches	8 inches
	Die # 2: 8 inches	
Quality Certification	ISO-9001	ISO-9001
	IATF16949	IATF16949
	ISO-14001 CERTIFIED	ISO-14001 CERTIFIED

Note: This change is from dual die to single die solution while keeping the same Catalog Part Number (CPN).

**Impacts to Data Sheet:**None

**Change Impact**None

**Reason for Change:**To improve manufacturability by qualifying United Microelectronics Corporation - Fab 8D (U08D) as a new wafer fabrication site.

**Change Implementation Status:**In Progress

**Estimated Qualification Completion Date:**February 2023

Note: Please be advised the qualification completion times may be extended because of unforeseen business conditions however implementation will not occur until after qualification has completed and a final PCN has been issued. The final PCN will include the qualification report and estimated first ship date. Also note that after the estimated first ship date guided in the final PCN customers may receive pre and post change parts.

**Time Table Summary:**

	January 2023					February 2023			
Workweek	01	02	03	04	05	06	07	08	09
Initial PCN Issue Date				X					

Qual Report Availability								X	
Final PCN Issue Date								X	

**Method to Identify Change:**Traceability code

**Qualification Plan:**Please open the attachments included with this PCN labeled as PCN\_#\_Qual\_Plan.

**Revision History:**January 26, 2023: Issued initial notification.

The change described in this PCN does not alter Microchip's current regulatory compliance regarding the material content of the applicable products.

## Attachments:

[PCN\\_JAON-230QOC341\\_Qual Plan.pdf](#)

[PCN\\_JAON-230QOC341\\_Qual Report.pdf](#)

Please contact your local [Microchip sales office](#) with questions or concerns regarding this notification.

## Terms and Conditions:

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If you wish to change your PCN profile, including opt out, please go to the [PCN home page](#) select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.



**PCN #: JAON-23OQOC341**

**Date:  
January 24, 2023**

**Qualification of United Microelectronics Corporation - Fab 8D (U08D) as new fabrication site for selected 24LC515, 24AA515, and 24FC515 device families available in 8L SOIJ (.208in) and 8L PDIP (.300in) packages.**

**Purpose:** Qualification of United Microelectronics Corporation - Fab 8D (U08D) as new fabrication site for selected 24LC515, 24AA515, and 24FC515 device families available in 8L SOIJ (.208in) and 8L PDIP (.300in) packages.

**CCB No.:** 6126

ESD-CDM & Latchup Characterization for SOIJ package

Test	Sample Size	Reference Method
CDM	18	JEDEC JS-002
Latch Up @ 25°C	6	JESD78
Latch Up @ 125°C	6	JESD78

Affected Catalog Part Numbers (CPN)

24LC515-I/SM  
24AA515-I/SM  
24LC515-I/P  
24AA515-I/P  
24LC515T-I/SM  
24AA515T-I/SM  
24FC515-I/SM  
24FC515-I/P  
24FC515T-I/SM



**PCN #: JAON-230QOC341**

**Date:  
June 24, 2021**

**Qualification of United Microelectronics Corporation - Fab 8D (U08D) as new fabrication site for selected 24LC515, 24AA515, and 24FC515 device families available in 8L SOIJ (.208in) and 8L PDIP (.300in) packages.**

**Purpose:** Qualification of United Microelectronics Corporation - Fab 8D (U08D) as new fabrication site for selected 24LC515, 24AA515, and 24FC515 device families available in 8L SOIJ (.208in) and 8L PDIP (.300in) packages.

**CCB No.:** 6126

**Device Description:**

Device	AT24C512C, 24CS512, 24FC512, 24LC512, 24AA512
Product	512kBit I2C SEEPR0M Memory

**Qualification Material:**

Test Lot	Lot 1	Lot 2	Lot 3	Lot 4
CPN	24CS512	24CS512	24CS512	24CS512
WAFER FAB	UMC - 8D	UMC - 8D	UMC - 8D	UMC - 8D
ASSEMBLY LOT	MTAI204401928	MTAI210902449	MTAI211103063	MTAI211103064
PACKAGE	8L SOIC	8L SOIC	8L SOIC	8L SOIC
ASSEMBLY SITE	MTAI	MTAI	MTAI	MTAI
FINAL TEST	MTAI	MTAI	MTAI	MTAI
QUAL TESTS –SJ	END, ESD/LU	END/DLT, END/DR	END/DLT, END/DR	END/DLT, END/DR
ASSEMBLY LOT	Note 1	MMT-210900044	MMT-211300072	MMT-211300073
PACKAGE	Note 1	8L PDIP	8L PDIP	8L PDIP
ASSEMBLY SITE	Note 1	MMT	MMT	MMT
FINAL TEST	Note 1	MMT	MMT	MMT
QUAL TESTS – MTHAI	Note 1	ELFR / DLT	ELFR / DLT	ELFR / DLT

Note 1: Lot 1 used for ESD/LU testing only, as only 3 lots are required for ELFR/DLT per QCI-39000.





**Qualification Data:****Endurance / Dynamic Life Test (Stress conducted at MCHP San Jose)**

Stress Method	MIL-STD 883 Method 1033		
Stress Condition	$T_a = 85^{\circ}\text{C} / V_{cc} = 5\text{V} / 100,000 \text{ cycles (Write } 0\text{x}00\text{h)}$		
Min Sample Size	77 pieces/lot		
Test Temperatures	25C, -40C, 85C, 125C		
Lot #; Fail / Pass	Lot 2; 0 Fails / 92	Lot 3; 0 Fails / 92	Lot 4; 0 Fails / 92
Stress Method	MIL-STD 883 Method 1005		
Stress Condition	$T_a = 150^{\circ}\text{C} / V_{CC} = 5.5\text{V} / 408 \text{ hours}$		
Min Sample Size	77 pieces/lot		
Test Temperatures	25C, -40C, 85C, 125C		
Readpoint 1	408 hours		
Lot #; Fail / Pass	Lot 2; 0 Fails / 92	Lot 3; 0 Fails / 92	Lot 4; 0 Fails / 92
Readpoint 2	+600 hours (1008 Total)		
Lot # Fail / Pass	Lot 2; 0 Fails / 92	Lot 3; 0 Fails / 92	Lot 4; 0 Fails / 92

**Endurance / Data Retention (Stress conducted at MCHP San Jose)**

Stress Method	MIL-STD 883 Method 1033		
Stress Condition	$T_a = 85^{\circ}\text{C} / V_{cc} = 5\text{V} / 100,000 \text{ cycles (Write } 0\text{x}00\text{h)}$		
Min Sample Size	231 pieces/lot		
Test Temperatures	25C, -40C, 85C, 125C		
Lot #; Fail / Pass	Lot 2; 0 Fails / 246	Lot 3; 0 Fails / 246	Lot 4; 0 Fails / 246
Stress Method	JESD22A-103		
Stress Condition	$T_a = 175^{\circ}\text{C} 504 \text{ hours}$		
Min Sample Size	231 pieces/lot		
Test Temperatures	25C, -40C, 85C, 125C		
Readpoint 1	504 hours		
Lot #; Fail / Pass	Lot 2; 0 Fails / 246	Lot 3; 0 Fails / 246	Lot 4; 0 Fails / 246

Endurance Testing (Stress conducted at MCHP San Jose)

Test Method	MIL-STD 883 Method 1033
Test Condition	Ta = +25°C / VCC= 5V / 1,000,000 cycles Write 0x00h
Min Sample Size	Not Required
Readpoint 1 – 9	Every 100,000 Cycles
Lot #; Fail / Pass, Test Criteria	Lot 2; 0 / 92, QC Test +25C
Readpoint 10	1,000,000 Cycles
Lot #; Fail / Pass, Test Criteria	Lot 2; 0 / 92, QC Test +25C, -40C, +85C, +125C 0 / 10. Margin Test at +25C

Early Life Reliability (ELFR) + Dynamic Life Test (Stress conducted at MTAI)

Stress Method	MIL-STD 883 Method 1005		
Stress Condition	Ta = 150°C / VCC= 5.5V / 408 hours		
Min Sample Size	ELFR 800 Pieces/Lot, 0 Fails		
Readpoint 1 Test Temperatures	24 hours 25C, -40C, 85C, 125C		
Lot# Fail / Pass	Lot 2; 0 / 815	Lot 3; 0 Fails / 815	Lot 4; 0 Fails / 814
Min Sample Size	DLT 600 Pieces/Lot, 0 Fails		
Readpoint 2 Test Temperatures	+312 hours (408 Total) 25C, -40C, 85C, 125C		
Lot# Fail / Pass	Lot 2; 0 / 615	Lot 3; 0 Fails / 615	Lot 4; 0 Fails / 615

Note: Lot 4 sample excludes one device failed for handling induced damage not related to product stress.

ESD & Latchup Characterization (Stress conducted at MCHP San Jose)

Test	Sample Size	Reference Method	Result
ESD – HBM	12	JEDEC JS-001-2017	Pass ±5000 V
CDM	18	JEDEC JS-002	Pass ±1500 V
Latch Up @ 25°C	6	JESD78	200mA Pass
Latch Up @ 125°C	6	JESD78	200mA Pass