Product Change Notification / SYST-18DEPU987

Date:

23-Jan-2023

Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ERRATA - PIC18(L)F27/47/57K42 Family Silicon Errata and Data Sheet Clarification

Affected CPNs:

SYST-18DEPU987_Affected_CPN_01232023.pdf
SYST-18DEPU987_Affected_CPN_01232023.csv

Notification Text:

SYST-18DEPU987

Microchip has released a new Errata for the PIC18(L)F27/47/57K42 Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at PIC18(L)F27/47/57K42 Family Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change:
Updated Module 1.3 Minimum VDD Specification for silicon revision A3.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 23 Jan 2023

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

PIC18(L)F27/47/57K42 Family Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

Terms and Conditions:

If you wish to receive Microchip PCNs via email please register for our PCN email service at our PCN home page select register then fill in the required fields. You will find instructions about registering for Microchips PCN email service in the PCN FAQ section.

If you wish to change your PCN profile, including opt out, please go to the PCN home page select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.

PIC18(L)F27/47/57K42

PIC18(L)F27/47/57K42 Family Silicon Errata and Data Sheet Clarification

The PIC18(L)F27/47/57K42 family devices that you have received conform functionally to the current Device Data Sheet (DS40001919**F**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18(L)F27/47/57K42 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A3**).

Data Sheet clarifications and corrections start on page 9, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, contact your local Microchip sales office for assistance.

The DEVREV/REVID values for the various PIC18(L)F27/47/57K42 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID<13:0>(1), (2)	Revision ID for Silicon Revision	
		A1	A3
PIC18F27K42	6C40h	A001	A003
PIC18F47K42	6BE0h	A001	A003
PIC18F57K42	6B80h	A001	A003
PIC18LF27K42	6D80h	A001	A003
PIC18LF47K42	6D20h	A001	A003
PIC18LF57K42	6CC0h	A001	A003

Note 1: The Revision ID is located in addresses 3FFFFCh-3FFFFDh and Device ID is located in addresses 3FFFFEh-3FFFFFh.

2: Refer to the *"PIC18(L)F27/47/57K42 Memory Programming Specification"* (DS40001886) for detailed information on Device and Revision IDs for your specific device.

© 2019-23 Microchip Technology Inc. and its subsidiaries

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item No.	Issue Summary	Affected Revisions(1)	
				A1	A3
Electrical Specifications	SMBus 3.0	1.1	SMBus 3.0 logic levels.	X	X
	Minimum VDD specification (rev A1)	1.2	Device may not work properly at certain voltage levels and temperatures in this silicon revision.	X	
	Minimum VDD specification (rev A3)	1.3	Device may not work properly at certain voltage levels and temperatures in this silicon revision.		X
	Fixed Voltage Reference (FVR) accuracy	1.4	FVR output tolerance may be higher than specified at temperatures below -20°C.	X	X
Direct Memory Access (DMA)	DMA reads from data EEPROM	2.1	DMA reads from data EEPROM does not operate.	X	
	DMA in Doze mode	2.2	DMA transfers may not work when CPU is in Doze mode.	X	
Analog-to-Digital Converter with Computation (ADC2)	ADC Conversion in FOSC mode	3.1	ADC does not complete conversion successfully in FOSC mode.	X	
	Burst Average mode Double Sampling	3.2	The ADC^2 does not trigger the second conversion when operated in non-continuous double-sampling Burst Average mode.	X	
	Double Sample Conversions	3.3	An unexpected acquisition time is added between the first and second conversions.	X	X
Universal Asynchronous Receiver Transmitter (UART)	BRGS Select	4.1	BRGS Select feature not functional in DALI mode.		X
	Stop bit interrupt flag	4.2	Stop bit interrupt flag functionality not available.	X	
	Auto-baud	4.3	The first character after auto-baud may be corrupted.	X	X
I2C	I^{2}C Receive Buffer	5.1	Received data is transferred into the I2CxRXB buffer on an incorrect clock edge.	X	X
	I^{2}C Start/Stop Flags	5.2	I^{2}C Start and/or Stop flags maybe set when I^{2}C is enabled.	X	X
Nonvolatile Memory (NVM) Control	WRERR bit functionality	6.1	The WRERR bit cannot be cleared in hardware after being set once.	X	
Windowed Watchdog Timer (WWDT)	WWDT operation in Doze mode	7.1	Window violation occurs when WWDT operated in Doze mode.	X	
Power-Saving Operation Modes	Low-Power Sleep mode	8.1	Low-power Sleep mode does not operate at 3.1V < VDD < 3.3V.	X	
Program Flash Memory (PFM)	Endurance of PFM	9.1	Endurance of PFM is lower than specified.	X	X
Instruction Set	MOVFF/MOVSF instruction	10.1	MOVFF/MOVSF may corrupt destination.	X	X
In-Circuit Debugging (ICD)	Software breakpoints	11.1	Software breakpoints are not available.	X	X
Central Processing Unit (CPU)	FSR Shadow Registers	12.1	FSR Shadow Registers are not writable.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

© 2019-23 Microchip Technology Inc. and its subsidiaries

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A3**).

1. Module: Electrical Specifications

1.1 SMBus 3.0

The SMBus 3.0 V_{IL} specification (Parameter D305) is temperature and V_{DD} dependent. Refer to the table below.

Temperature	V_{DD}	D305 SMBus 3.0 V_{IL} Specification
-40°C	1.8V	0.6V
-40°C	5.5V	0.8V
25°C	1.8V	0.6V
25°C	5.5V	0.8V
85°C	1.8V	0.6V
85°C	5.5V	0.7V
125°C	1.8V	0.5V
125°C	5.5V	0.7V

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

1.2 Minimum V_{DD} Specification (Silicon Revision A1)

V_{DDMIN} for silicon revision A1 has changed for temperatures below +25°C, as shown in the excerpt of Table 44-1 below (in **bold**).

Work around

None.

Affected Silicon Revisions

A1	A3						
X							

TABLE 44-1: SUPPLY VOLTAGE (EXCERPT)

PIC18LF27/47/57K42			Standard Operating Conditions (unless otherwise stated)				
PIC18F27/47/57K42							
Param. No.	Sym.	Characteristic	Min.	Typ.†	Max.	Units	Conditions
Supply Voltage							
D002	V_{DD}		**2.5** 1.8 2.5 2.7	— — — —	3.6 3.6 3.6 3.6	V V V V	$F_{OSC} \leq$ 16 MHz **(-40°C to <+25°C)** $F_{OSC} \leq$ 16 MHz **(≥+25°C to +125°C)** $F_{OSC} >$ 16 MHz and $F_{OSC} \leq$ 32 MHz $F_{OSC} >$ 32 MHz
D002	V_{DD}		**2.5** 2.3 2.5 2.7	— — — —	5.5 5.5 5.5 5.5	V V V V	$F_{OSC} \leq$ 16 MHz **(-40°C to <+25°C)** $F_{OSC} \leq$ 16 MHz **(≥+25°C to +125°C)** $F_{OSC} >$ 16 MHz and $F_{OSC} \leq$ 32 MHz $F_{OSC} >$ 32 MHz

1.3 Minimum VDD Specification (Silicon Revision A3)

VDDMIN for silicon revision A3 devices has changed for the temperature ranges between -40°C to +25°C and +25°C to +125°C, as shown in the excerpt of Table 44-1 below (in **bold**).

Work around

None.

Affected Silicon Revisions

A1	A3						
	X						

.

TABLE 44-1: SUPPLY VOLTAGE (EXCERPT)

PIC18LF27/47/57K42			Standard Operating Conditions (unless otherwise stated)				
PIC18F27/47/57K42							
Param. No.	Sym.	Characteristic	Min.	Typ.†	Max.	Units	Conditions
Supply Voltage							
D002	VDD		**2.7** **2.5** 2.7	**—** **—** —	**3.6** **3.6** 3.6	**V** **V** V	**Fosc ≤ 32 MHz (-40°C to <+25°C)** **Fosc ≤ 32 MHz (≥+25°C to +125°C)** FOSC > 32 MHz
D002	VDD		**2.7** **2.5** 2.7	**—** **—** —	**5.5** **5.5** 5.5	**V** **V** V	**Fosc ≤ 32 MHz (-40°C to <+25°C)** **Fosc ≤ 32 MHz (≥+25°C to +125°C)** FOSC > 32 MHz

1.4 Fixed Voltage Reference (FVR) Accuracy

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This will apply to all three gain amplifier settings (1X, 2X, 4X). The affected parameter numbers found in the data sheet are: FVR01 (1X gain setting), FVR02 (2X gain setting), and FVR03 (4X gain setting).

Work around

At temperatures above -20°C, the stated tolerances in the data sheet remain in effect. Operate the FVR only at temperatures above -20°C.

Affected Silicon Revisions

A1	A3						
X	X						

© 2019-23 Microchip Technology Inc. and its subsidiaries

2. Module: Direct Memory Access (DMA)

2.1 DMA Reads from Data EEPROM

The DMA modules do not operate when configured to access the data EEPROM (i.e., SMR[1:0] = 1x). The destination gets written to 0x00.

Work around

None. NVMCON reads work as described.

Affected Silicon Revisions

A1	A3						
X							

2.2 DMA in Doze Mode

When the CPU is operated in Doze mode, DMA transfers may not work as expected.

Work around

None.

Affected Silicon Revisions

A1	A3						
X							

3. Module: Analog-to-Digital Converter with Computation (ADC^2)

3.1 ADC Conversion in Fosc Mode

The ADCON0.GO bit remains set and the conversion does not complete successfully when configured to operate in FOSC mode (ADCON0.CS = 0) with FOSC > 40 MHz.

Work around

Use ADCRC as the ADC clock source (ADCON0.CS = 1).

Affected Silicon Revisions

A1	A3						
X							

3.2 Burst Average Mode Double Sampling

When the ADC^2 is operated in Burst Average mode (MD = 0b011 in the ADCON2 register) while enabling non-continuous operation and double-sampling (CONT = 0 in the ADCON0 register and DSEN = 1 in the ADCON1 register), the value in the ADCNT register does not increment beyond 0b1 toward the value in the ADRPT register.

Work around

When operating the ADC^2 in Burst Average mode with double-sampling, enable continuous operation of the module (CONT = 1 in the ADCON0 register) and set the Stop-On-Interrupt bit (SOI in the ADCON3 register). After the interrupt occurs, perform appropriate threshold calculations in the software and retrigger ADC^2 as necessary.

If the CPU is in Low-Power Sleep mode, alternatively the ADC^2 in non-continuous Burst Average mode can be operated with single ADC conversion (DSEN = 0 in the ADCON1 register) compromising noise immunity for lower power consumption by preventing the device from waking up to perform threshold calculations in the software.

Affected Silicon Revisions

A1	A3						
X							

3.3 Double Sample Conversions

When enabling a Double Sample Conversion (DSEN = 1), with no Precharge time (ADPRE = 0) and no Acquisition time (ADACQ = 0), the maximum number of cycles of acquisition time is inserted prior to the second conversion.

The first conversion will be performed as expected with no Precharge time and no Acquisition time. It is only between the first and second conversions where a maximum number of cycles of Acquisition time is performed unexpectedly.

Work around

Method 1: Disable double conversion (DSEN = 0) and perform two single conversions back to back.

Method 2: If adding acquisition time is acceptable, then select no Precharge time, along with the desired Acquisition time.

Affected Silicon Revisions

A1	A3						
X	X						

4. Module: Universal Asynchronous Receiver Transmitter (UART)

4.1 Baud Rate Generator Speed Select

The Baud Rate Generator Speed Select feature (the BRGS bit in the UxCON0 register) in DALI mode is not functional. The Baud Rate Generator always operates at normal speed with 16 baud clocks per bit in DALI mode.

Work around

None.

Affected Silicon Revisions

A1	A3						
	X						

4.2 Stop Bit Interrupt Flag

Stop bit interrupt flag functionality is not available in the CERIF bit in revision A1.

Work around

Use Timer2 with HLT and connect the UART RX port to the timer Reset trigger. Set the time-out period to the desired Stop bit time (for DALI mode, this is equivalent to two Stop bits at 1200 baud = 1.66 ms). When the Stop bit is received, the timer times out notifying end of data.

Affected Silicon Revisions

A1	A3						
X							

4.3 Auto-Baud

When the UART is configured as follows, then the first character received after auto-baud may be corrupted:

- The UBRG registers are cleared.
- The BRGS bit is set (Fast Baud Rate mode).
- The Stop bits are configured for two Stop bits (STP = 0b1x).

Work around

a) In asynchronous modes other than LIN: The transmitter may delay the first character by at least one character period after sending auto-baud.

b) In all asynchronous modes including LIN: Clear the BRGS bit to select the normal baud rate mode.

Affected Silicon Revisions

A1	A3						
X	X						

5. Module: I²C

5.1 I²C Receive Buffer

When receiving data into the receive buffer I2CxRXB, the byte is transferred into the buffer on the 9th rising clock edge rather than the expected 8th falling edge. This causes both the Receive Buffer Full (RXBF) status bit and the Receive Buffer Interrupt Flag (I2CxRXIF) to also be set on the 9th rising clock edge. The Data Write Interrupt (WRIF) and Address Interrupt Flag (ADRIF) will still be set on the 8th falling clock edge. If user software is configured to interrupt (or poll) when either the WRIF bit or the ADRIF bit is set, hardware will read an empty receive buffer, set the Receive Read Error (RXRE) status flag, and a NACK will be issued.

Work around

Do not use WRIF or ADRIF to determine when the receive buffer has received data. Instead, interrupt/poll using the I2CxRXIF interrupt bit or poll the RXBF bit. These bits are correctly set once the address/data byte has been transferred into I2CxRXB.

Affected Silicon Revisions

A1	A3						
X	X						

5.2 I²C Start and/or Stop Flags May be Set When I²C is Enabled

When I²C is enabled, erroneous Start and/or Stop conditions may be detected. This can generate erroneous I²C interrupts if enabled.

Work around

Use the following procedure to correctly detect the Start and Stop conditions:

1. Disable Start and Stop conditions interrupt functions.
2. Enable I²C module.
3. Wait 250 ns + 6 instruction cycles (Fosc/4).
4. Clear the Start and Stop conditions interrupt flags.
5. Enable Start and Stop conditions interrupt functions if used.

```
I2CxPIEbits.SCIE = 0;
I2CxPIEbits.PCIE = 0;
I2CxCON0bits.EN = 1;
Delay();
I2CxPIRbits.SCIF = 0;
I2CxPIRbits.PCIF = 0;
I2CxPIEbits.SCIE = 1;
I2CxPIEbits.PCIE = 1;
```

Affected Silicon Revisions

A1	A3						
X	X						

6. Module: Nonvolatile Memory (NVM) Control

6.1 WRERR Bit Functionality

When a Reset is issued while an NVM high-voltage operation is in progress, the WRERR bit in the NVMCON1 register is set as expected. After clearing the WRERR bit, if a Reset reoccurs, the WRERR bit is set again regardless of whether an NVM operation is in progress or not.

Work around

None.

Affected Silicon Revisions

A1	A3						
X							

7. Module: Windowed Watchdog Timer (WWDT)

7.1 WWDT Operation in Doze Mode

When the CLRWDT instruction is issued in Doze mode, a window violation error occurs in WWDT even though the window is open and armed.

Work around

Do not operate the WWDT in Doze mode.

Affected Silicon Revisions

A1	A3						
X							

8. Module: Power-Saving Operation Modes

8.1 Low-Power Sleep Mode in F Devices

The F device resets when waking up from Sleep while in Low-Power mode (VREGPM = 1 in the VREGCON register) at 3.1V < VDD < 3.3V.

Work around

a) If wake-up from Sleep is needed at 3.1V < VDD < 3.3V, operate the F device in Normal Power mode (VREGPM = 0).

b) If wake-up from Sleep is needed at 3.1V < VDD < 3.3V, enable the Fixed Voltage Reference (EN = 1 in the FVRCON register). This increases the current in Sleep mode by typically 7 µA.

Affected Silicon Revisions

A1	A3						
X							

9. Module: Program Flash Memory (PFM)

9.1 Endurance of PFM

The Flash memory cell endurance specification (Parameter MEM30) is 1K cycles.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

10. Module: Instruction Set

10.1 MOVFF/MOVSF Instruction

When the BSR points to the last bank of the SFR region (BSR = 0x3F) and the low byte of the source or destination address of a MOVFF/MOVSF instruction equals the low byte of an indirect addressing operation register address (INDFx, POSTINCx, POSTDECx, PREINCx, PLUSWx), the operation will not be completed as expected. Either, one or more of the destination, FSR value, or location pointed to by the FSR will be corrupted, or the move will simply not occur.

Work around

Ensure that the BSR does not point to the last bank of the SFR region (BSR = 0x3F) when the MOVFF/MOVSF instruction is being executed.

Affected Silicon Revisions

A1	A3						
X	X						

11. Module: In-Circuit Debugging (ICD)

11.1 Software Breakpoints

When debugging code, software breakpoints will not be available.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

12. Module: Central Processing Unit (CPU)

12.1 FSR Shadow Registers

Writing to the FSR Shadow Registers does not result in accurate values being stored in the registers. Consequently, reading the FSR Shadow Registers after they have been written will return inaccurate data.

Work around

Writes to the FSR shadow registers can be performed safely using the following steps:

1. Save regular FSR2 value into RAM
2. Write the regular FSR2 with the targeted value minus the computed offset (IR[6:0] + 1, see below)
3. Write the shadow FSRxL (data doesn't matter), this will clock the shadow FSR with the FSR computed offset value.
4. Decrement FSR2 value by 1 since FSRxH increments the address by 1 (IR[6:0])
5. Write FSRxH
6. Restore the regular FSR2 from the stored RAM value.

The FSR shadow should have the value desired and the regular FSR should have the original value.

Affected Silicon Revisions

A1	A3						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001919**F**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev G Document (01/2023)

Updated Module 1.3 Minimum VDD Specification for silicon revision A3.

Rev F Document (04/2022)

Added Module 3.3 Double Sample Conversions, 12 Central Processing Unit (CPU), and 12.1 FSR Shadow Registers.

Rev E Document (09/2021)

Added Module 5.2 I^2C Start/Stop Flags.

Rev D Document (02/2021)

Added Module 11.1 Software Breakpoints. Minor corrections.

Rev C Document (06/2019)

Added Modules 1.4 Fixed Voltage Reference (FVR) Accuracy and 5.1 I^2C Receive Buffer.

Rev B Document (03/2019)

Added silicon rev A3. Added Modules 1.3: Min V_{DD} Specification for LF Devices for A3 Rev, 2.2: DMA in Doze mode, 4: UART, 5: NVM Control, 6: WWDT, 7: Power-Saving Operation Modes, 8: PFM, and 9: Instruction Set.

Updated Module 1.2: Min VDD Specification for A1 Rev. Updated Table 2.

Data Sheet Clarifications: Removed Module 1.

Rev A Document (01/2018)

Initial release of this document.

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable" Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at https://www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, CryptoMemory, CryptoRF, dsPIC, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Kleer, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AgileSwitch, APT, ClockWorks, The Embedded Control Solutions Company, EtherSynch, Flashtec, Hyper Speed Control, HyperLight Load, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet-Wire, SmartFusion, SyncWorld, Temux, TimeCesium, TimeHub, TimePictra, TimeProvider, TrueTime, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, Augmented Switching, BlueSky, BodyCom, Clockstudio, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, Espresso T1S, EtherGREEN, GridTime, IdealBridge, In-Circuit Serial Programming, ICSP, INICnet, Intelligent Paralleling, IntelliMOS, Inter-Chip Connectivity, JitterBlocker, Knob-on-Display, KoD, maxCrypto, maxView, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, RTAX, RTG4, SAM-ICE, Serial Quad I/O, simpleMAP, SimpliPHY, SmartBuffer, SmartHLS, SMART-I.S., storClad, SQI, SuperSwitcher, SuperSwitcher II, Switchtec, SynchroPHY, Total Endurance, Trusted Time, TSHARC, USBCheck, VariSense, VectorBlox, VeriPHY, ViewSpan, WiperLock, XpressConnect, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, and Symmcom are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2019-23, Microchip Technology Incorporated and its subsidiaries.

All Rights Reserved.

ISBN: 978-1-6683-1840-9

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880- 3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4485-5910
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-72400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820

© 2019-23 Microchip Technology Inc. and its subsidiaries

SYST-18DEPU987 - ERRATA - PIC18(L)F27/47/57K42 Family Silicon Errata and Data Sheet Clarification

Affected Catalog Part Numbers(CPN)

PIC18F27K42-E/SP
PIC18F27K42-E/ML
PIC18F27K42-E/MLVAO
PIC18F27K42-E/MX
PIC18F27K42-E/SS
PIC18F27K42-E/SO
PIC18F27K42-I/SP
PIC18F27K42-I/ML
PIC18F27K42-I/MX
PIC18F27K42-I/SS
PIC18F27K42-I/SO
PIC18F27K42T-I/ML
PIC18F27K42T-I/MX
PIC18F27K42T-I/SS
PIC18F27K42T-I/SO
PIC18F27K42T-E/ML
PIC18F27K42T-E/MLV01
PIC18F27K42T-E/MLVAO
PIC18F47K42-E/P
PIC18F47K42-E/MV
PIC18F47K42-E/ML
PIC18F47K42-E/PT
PIC18F47K42-I/P
PIC18F47K42-I/MV
PIC18F47K42-I/ML
PIC18F47K42-I/PT
PIC18F47K42T-I/MV
PIC18F47K42T-I/ML
PIC18F47K42T-I/PT
PIC18F57K42-E/MV
PIC18F57K42-E/PT
PIC18F57K42-I/MV
PIC18F57K42-I/PT
PIC18F57K42T-I/MV
PIC18F57K42T-I/PT
PIC18LF27K42-E/SP
PIC18LF27K42-E/ML
PIC18LF27K42-E/MX
PIC18LF27K42-E/SS
PIC18LF27K42-E/SO
PIC18LF27K42-I/SP
PIC18LF27K42-I/ML

PIC18LF27K42-I/MX
PIC18LF27K42-I/SS
PIC18LF27K42-I/SO
PIC18LF27K42T-I/ML
PIC18LF27K42T-I/MX
PIC18LF27K42T-I/SS
PIC18LF27K42T-I/SO
PIC18LF27K42T-E/ML
PIC18LF47K42-E/P
PIC18LF47K42-E/MV
PIC18LF47K42-E/ML
PIC18LF47K42-E/PT
PIC18LF47K42-I/P
PIC18LF47K42-I/MV
PIC18LF47K42-I/ML
PIC18LF47K42-I/PT
PIC18LF47K42T-I/MV
PIC18LF47K42T-I/ML
PIC18LF47K42T-I/PT
PIC18LF57K42-E/MV
PIC18LF57K42-E/PT
PIC18LF57K42-I/MV
PIC18LF57K42-I/PT
PIC18LF57K42T-I/MV
PIC18LF57K42T-I/PT