ERRATA

N° 10391AERRA

Dear customer,

With this Infineon Technologies AG errata note we would like to inform you about the following

Erratum of Product Marking in Datasheet for BSC094N06LS5

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ERRATA

N° 10391AERRA

▶ Products affected

Please refer to attached affected product list
“ERR_10391AERRA_[customer-no].pdf”

▶ Detailed change information

Subject

Erratum of Product Marking in Datasheet for BSC094N06LS5

Reason

Product marking in datasheet shows nonconformance compared to the physical product marking on the device

Description

	Old	New
Marking Text	■ 094N06L	■ 094N06LS

▶ Impact of change

NO change of existing datasheet parameters

NO change in quality and reliability

NO change in package outline dimensions

▶ Attachments

ERR_10391AERRA_[customer-no].pdf	affected product list
DS_BSC094N06LS5_2_2.pdf	Product datasheet

▶ Implementation date

Immediate

If you have any questions, please do not hesitate to contact your local sales office.

ERR 10391AERRA

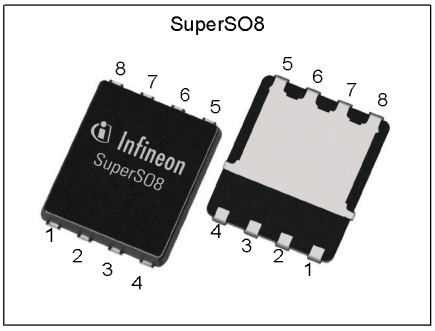
Erratum of Product Marking in Datasheet for BSC094N06LS5

Affected products sold to FUTURE ELECTRONICS INC. (4048203)

Sales name	SP number	OPN	Package	Customer part number
BSC094N06LS5	SP001458086	BSC094N06LS5ATMA1	PG-TDSON-8	BSC094N06LS5ATMA1

MOSFET

OptiMOS™ Power-Transistor, 60 V

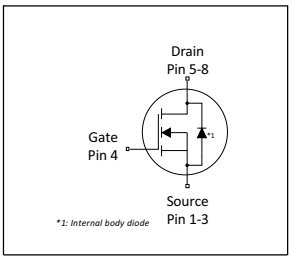


Features

- Optimized for high performance SMPS, e.g. sync. rec.
- 100% avalanche tested
- Superior thermal resistance
- N-channel, logic level
- Qualified according to JEDEC[1)] for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	60	V
$R_{DS(on),max}$	9.4	mΩ
I_D	47	A
Q_{OSS}	13	nC
Q_G(0V..4.5V)	7	nC



Type / Ordering Code	Package	Marking	Related Links
BSC094N06LS5	PG-TDSON-8	094N06LS	-

[1)] J-STD20 and JESD22

Table of Contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	- - -	- - -	47 30 11	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=10 V, T_A=25 °C, R_{thJA} =50K/W[1)]
Pulsed drain current[2)]	$I_{D,pulse}$	-	-	188	A	T_C=25 °C
Avalanche energy, single pulse[3)]	E_{AS}	-	-	13	mJ	I_D=30 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	36 2.1	W	T_C=25 °C T_A=25 °C, R_{thJA}=50 K/W[1)]
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	2.1	3.5	K/W	-
Device on PCB, 6 cm² cooling area[1)]	R_{thJA}	-	-	50	K/W	-

[1)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[2)] See Diagram 3 for more detailed information
[3)] See Diagram 13 for more detailed information

3 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	1.1	1.7	2.3	V	V_{DS}=V_{GS}, I_D=14 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1 100	µA	V_{DS}=60 V, V_{GS}=0 V, T_j=25 °C V_{DS}=60 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	7.7 11	9.4 13.4	mΩ	V_{GS}=10 V, I_D=24 A V_{GS}=4.5 V, I_D=12 A
Gate resistance[1)]	R_G	-	1.1	1.65	Ω	-
Transconductance	g_{fs}	22	45	-	S	|V_{DS}|>2|I_D|$R_{DS(on)max}$, I_D=24 A

Table 5 Dynamic characteristics[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	970	1300	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Output capacitance	C_{oss}	-	210	280	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	12	21	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	4	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=24 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	3	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=24 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	14	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=24 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	3	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=24 A, $R_{G,ext}$=1.6 Ω

Table 6 Gate charge characteristics[2)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	3	-	nC	V_{DD}=30 V, I_D=24 A, V_{GS}=0 to 4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	2	-	nC	V_{DD}=30 V, I_D=24 A, V_{GS}=0 to 4.5 V
Gate to drain charge[1)]	Q_{gd}	-	2	3.5	nC	V_{DD}=30 V, I_D=24 A, V_{GS}=0 to 4.5 V
Switching charge	Q_{sw}	-	4	-	nC	V_{DD}=30 V, I_D=24 A, V_{GS}=0 to 4.5 V
Gate charge total[1)]	Q_g	-	7	9.4	nC	V_{DD}=30 V, I_D=24 A, V_{GS}=0 to 4.5 V
Gate plateau voltage	$V_{plateau}$	-	3.1	-	V	V_{DD}=30 V, I_D=24 A, V_{GS}=0 to 4.5 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	12	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge[1)]	Q_{oss}	-	13	18	nC	V_{DD}=30 V, V_{GS}=0 V

[1)] Defined by design. Not subject to production test.
[2)] See "Gate charge waveforms" for parameter definition

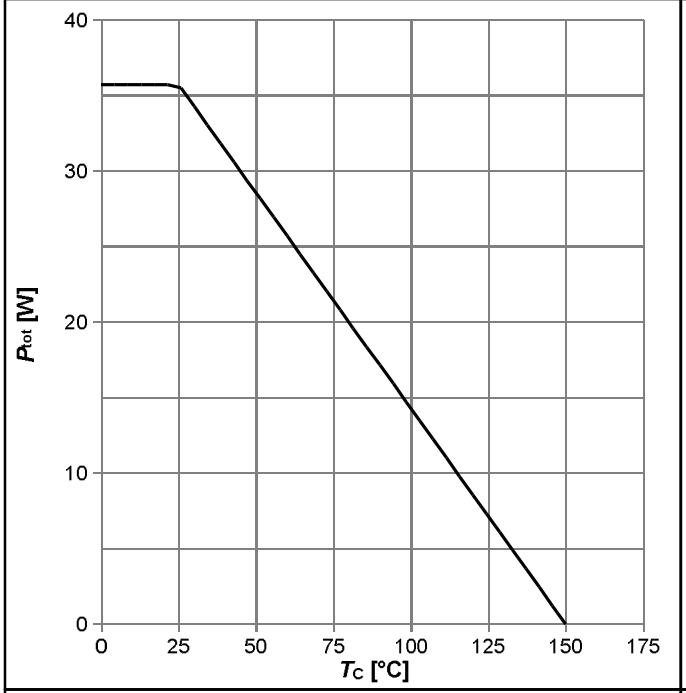
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	30	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	188	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.9	1.2	V	V_{GS}=0 V, I_F=24 A, T_j=25 °C
Reverse recovery time[1)]	t_{rr}	-	18	36	ns	V_R=30 V, I_F=24 A, di_F/dt=100 A/µs
Reverse recovery charge[1)]	Q_{rr}	-	6	12	nC	V_R=30 V, I_F=24 A, di_F/dt=100 A/µs

[1)] Defined by design. Not subject to production test.

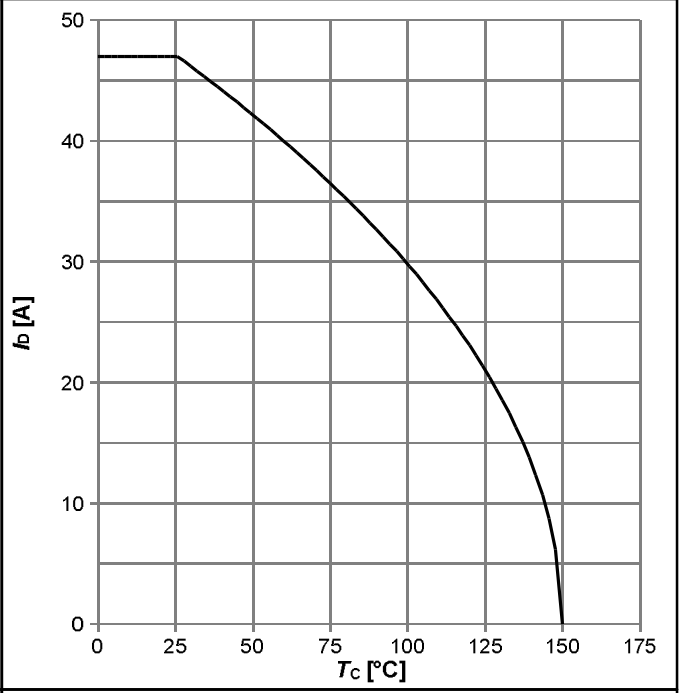
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



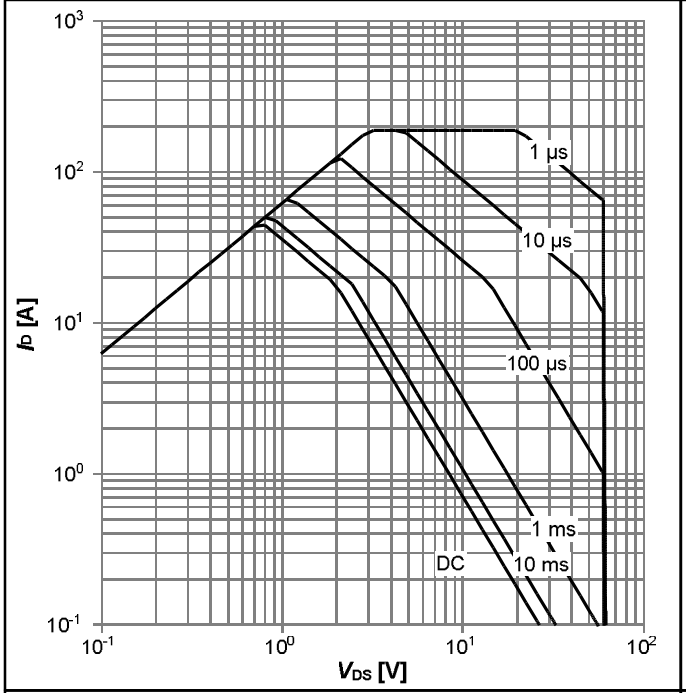
$P_{tot}=f(T_C)$

Diagram 2: Drain current



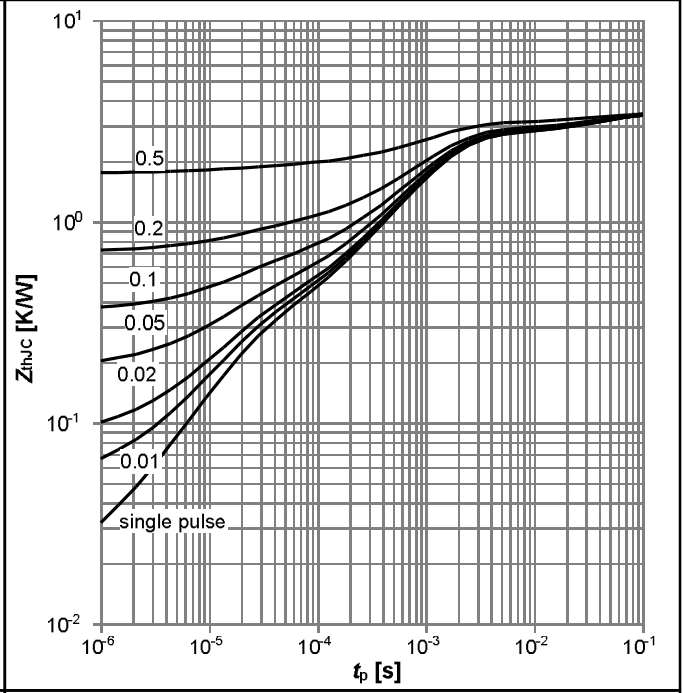
$I_D=f(T_C)$; $V_{GS}\geq 10$ V

Diagram 3: Safe operating area



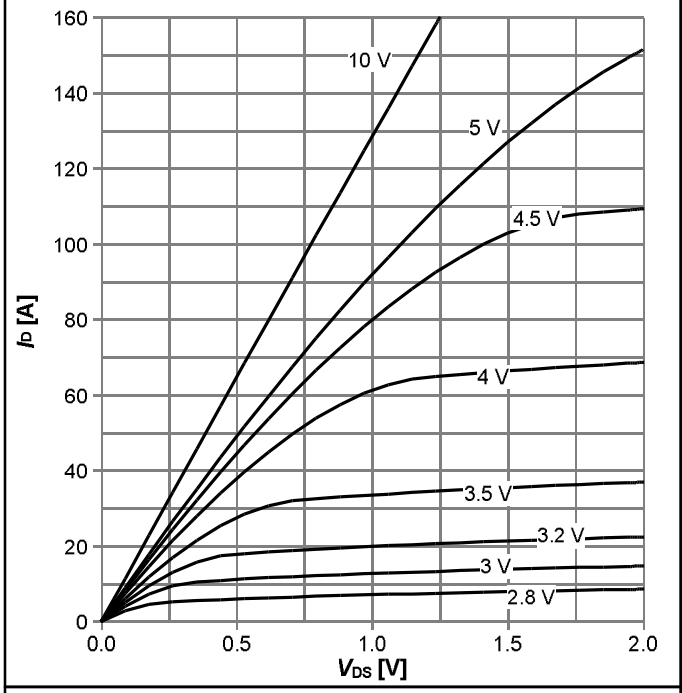
$I_D=f(V_{DS})$; T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



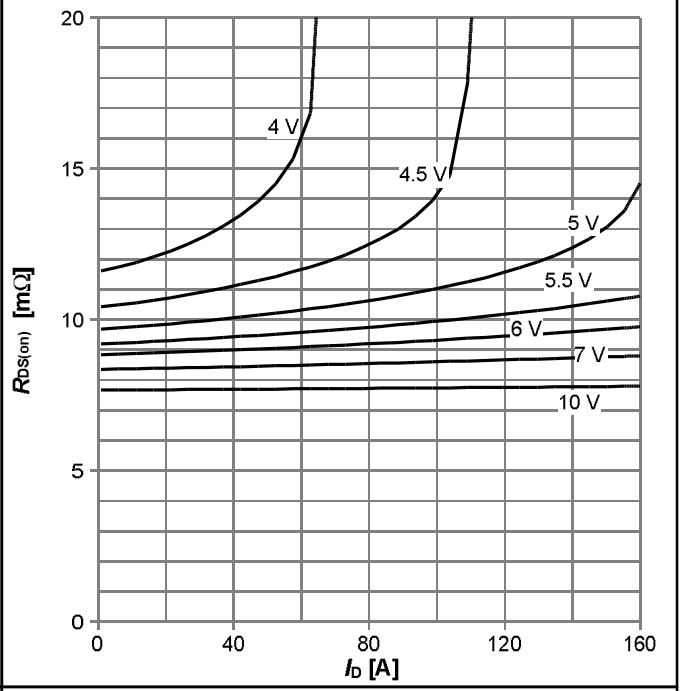
$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



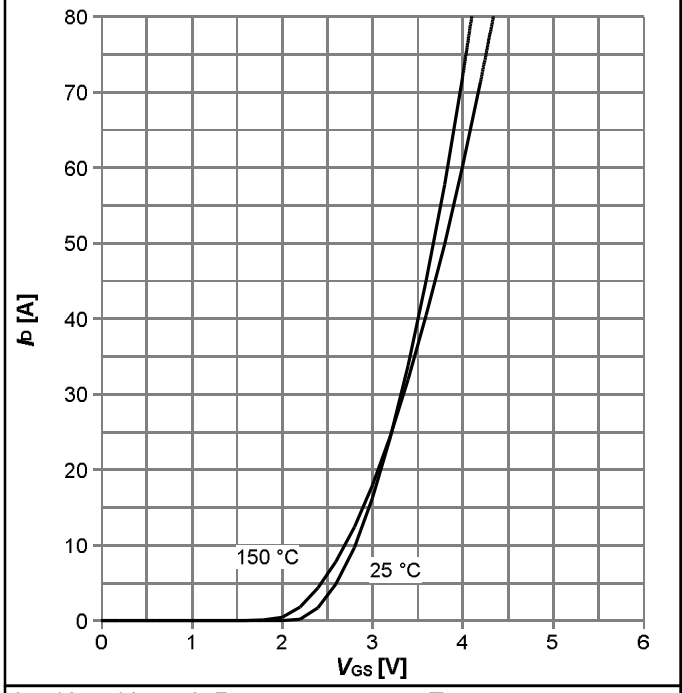
$I_D=f(V_{DS})$; $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



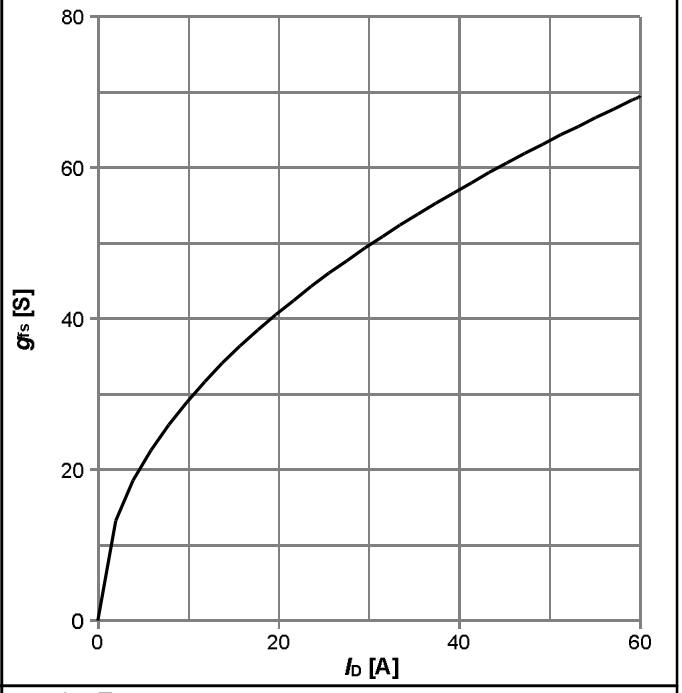
$R_{DS(on)}=f(I_D)$; $T_j=25$ °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



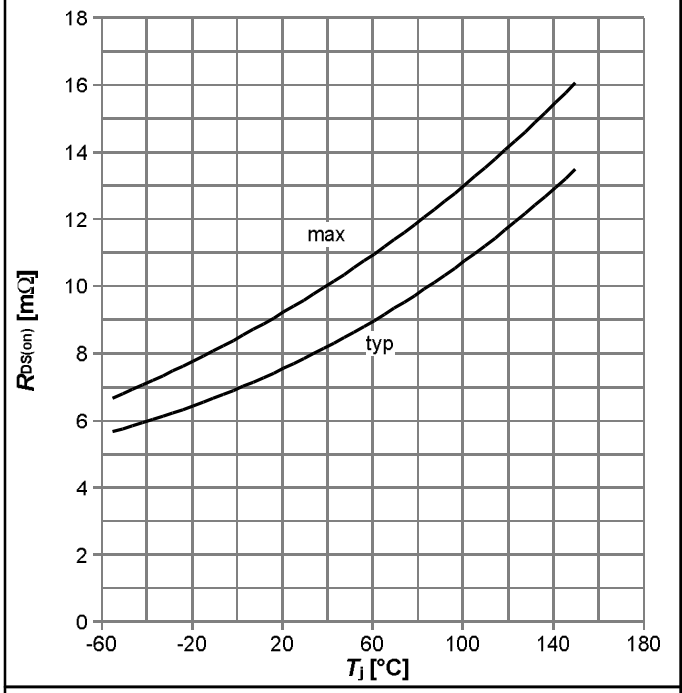
$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance



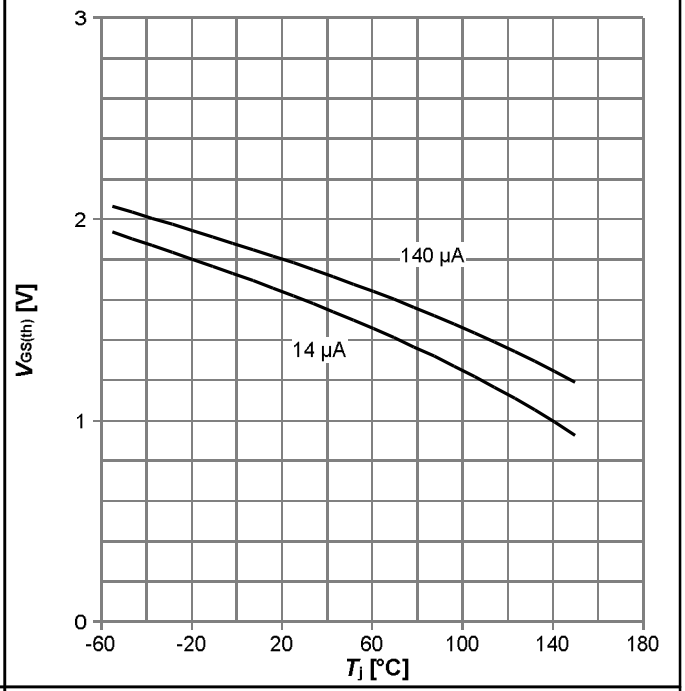
$g_{fs}=f(I_D)$; $T_j=25$ °C

Diagram 9: Drain-source on-state resistance



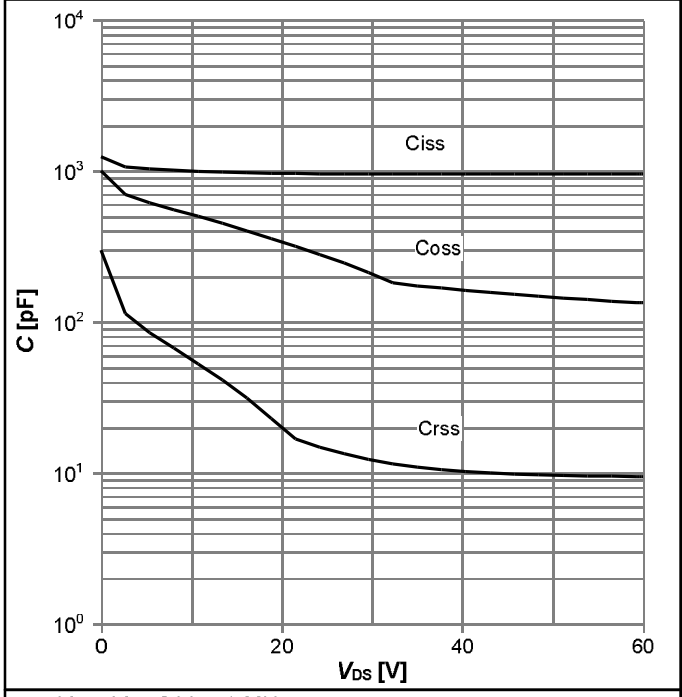
$R_{DS(on)}=f(T_j)$; I_D=24 A; V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



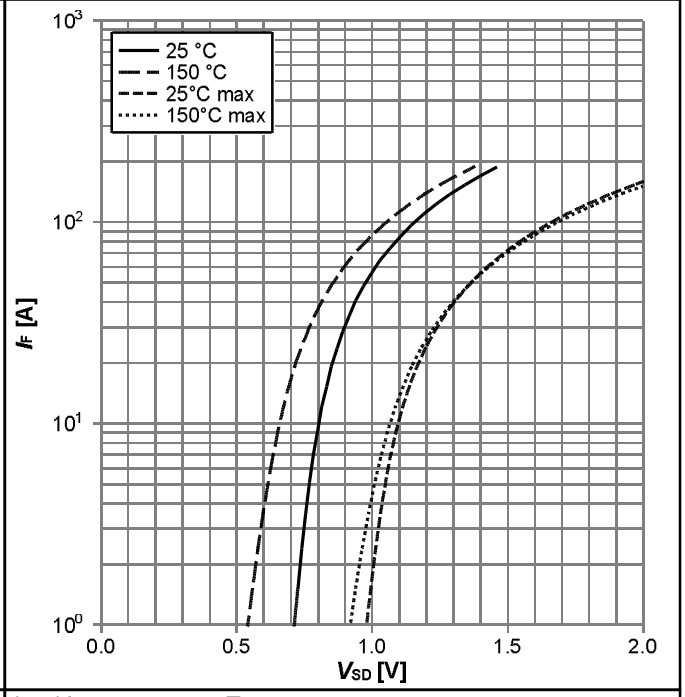
$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$

Diagram 11: Typ. capacitances



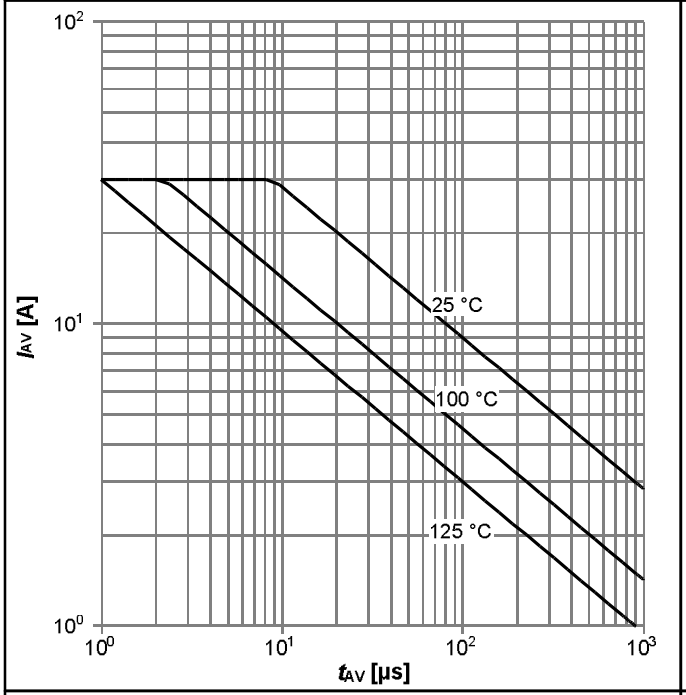
$C=f(V_{DS})$; V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



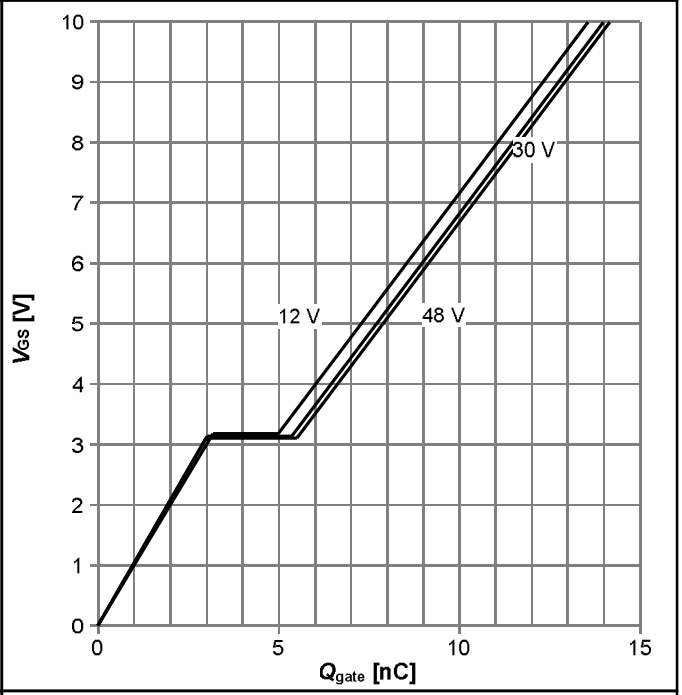
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



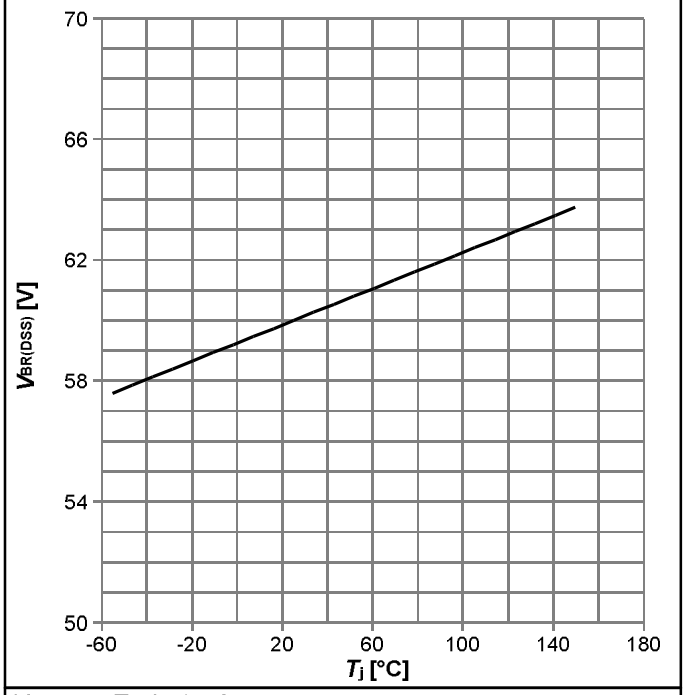
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



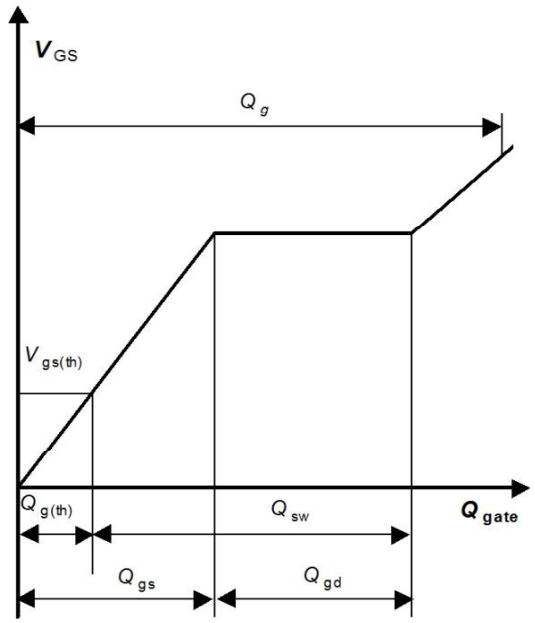
$V_{GS}=f(Q_{gate})$; $I_D=24$ A pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

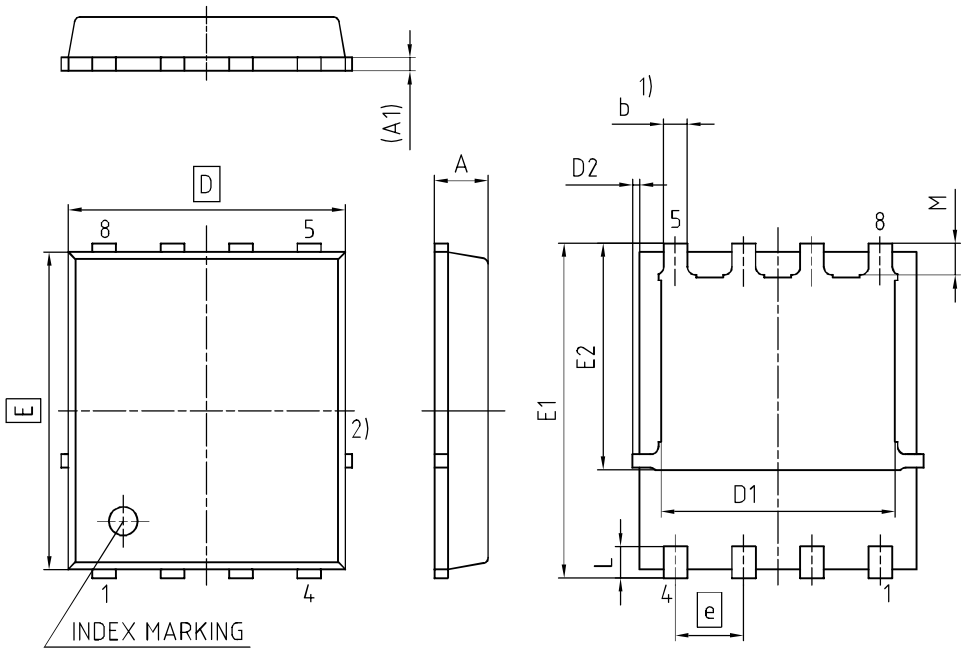


$V_{BR(DSS)}=f(T_j)$; $I_D=1$ mA

Diagram Gate charge waveforms



5 Package Outlines



1) EXCLUDING MOLD FLASH
2) REMOVAL ON MOLD GATE
INTRUSION 0.1 MM
PROTRUSION 0.1 MM
LEAD LENGTH UP TO ANTI FLASH LINE
ALL METAL SURFACES ARE PLATED, EXCEPT AREA OF CUT

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
A1	0.15	0.35
b	0.34	0.54
D	4.80	5.35
D1	3.90	4.40
D2	0.03	0.23
E	5.70	6.10
E1	5.90	6.42
E2	3.88	4.31
e	1.27	
L	0.45	0.71
M	0.45	0.69

DOCUMENT NO.	Z8B00003332
REVISION	07
SCALE	10:1
	0 1 2 3mm
EUROPEAN PROJECTION	
ISSUE DATE	06.06.2019

Figure 1 Outline PG-TDSON-8, dimensions in mm

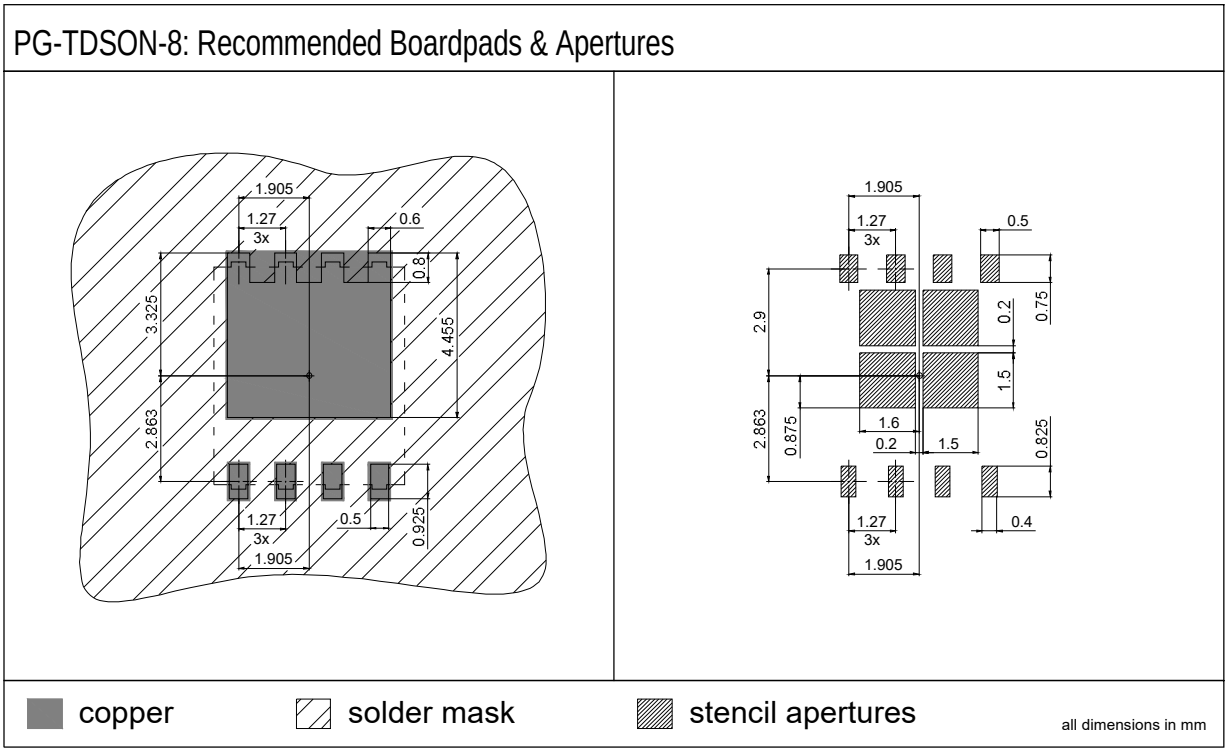
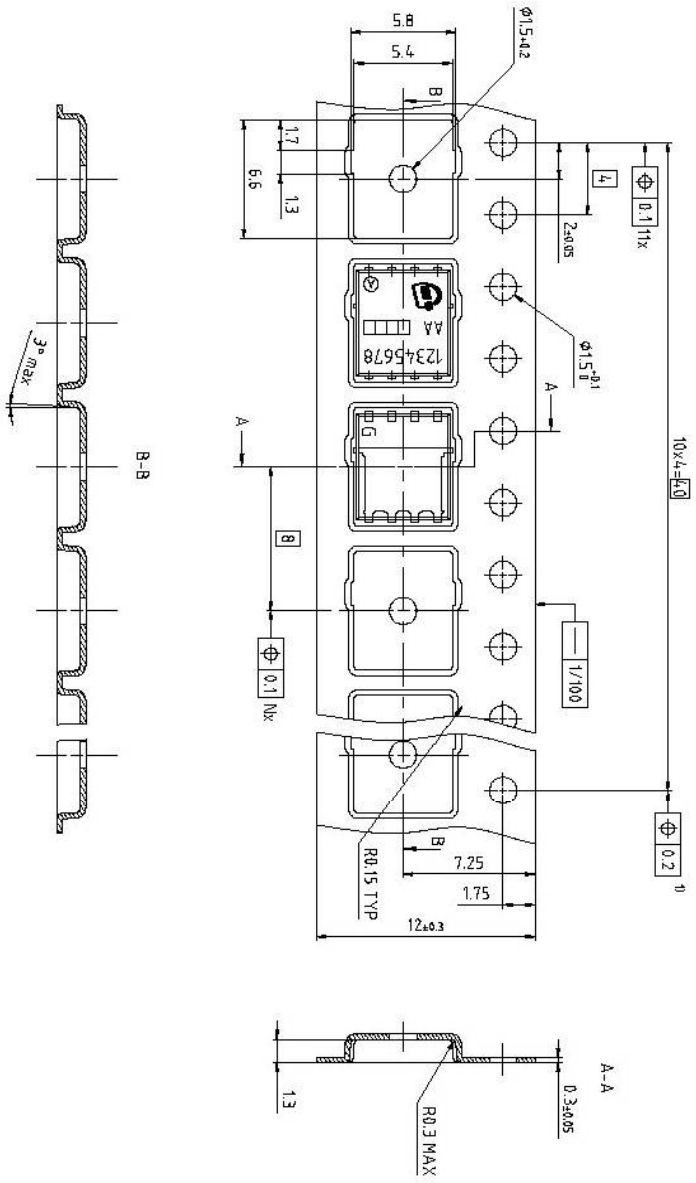


Figure 2 Outline Boardpads (TDSON-8), dimensions in mm



Dimension in mm

Figure 3 Outline Tape (TDSON-8)

Revision History

BSC094N06LS5

Revision: 2023-01-13, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-09-23	Release of final version
2.1	2020-05-15	Update package drawings
2.2	2023-01-13	Update Marking

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