Product Change Notification / SYST-23EPUW891

SYST-23EPUW891

Microchip has released a new Errata for the PIC18F27/47Q10 Silicon Errata and Data Sheet Clarifications of devices. If you are using one of these devices please read the document located at **PIC18F27/47Q10 Silicon Errata and Data Sheet Clarifications**.

Notification Status: Final

Description of Change: Added silicon erratum item 1.9.1

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 24 Nov 2022

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Date
24-Nov-2022

PCN Type
Document Change

PCN
SYST-23EPUW891

Title
ERRATA - PIC18F27/47Q10 Silicon Errata and Data Sheet Clarifications

Product Category
8-bit Microcontrollers

Affected CPNs
SYST-23EPUW891_Affected_CPN_11242022.pdf
SYST-23EPUW891_Affected_CPN_11242022.csv

Attachments
PIC18F27/47Q10 Silicon Errata and Data Sheet Clarifications

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Affected Catalog Part Numbers (CPN)

PIC18F27Q10-E/ML
PIC18F27Q10-E/SO
PIC18F27Q10-E/SP
PIC18F27Q10-E/SS
PIC18F27Q10-E/STX
PIC18F27Q10-I/ML
PIC18F27Q10-I/SO
PIC18F27Q10-I/SP
PIC18F27Q10-I/SS
PIC18F27Q10-I/STX
PIC18F27Q10T-I/ML
PIC18F27Q10T-I/SO
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PIC18F27Q10T-I/STX
PIC18F47Q10-E/MP
PIC18F47Q10-E/P
PIC18F47Q10-E/PT
PIC18F47Q10-I/MP
PIC18F47Q10-I/P
PIC18F47Q10-I/PT
PIC18F47Q10T-I/MP
PIC18F47Q10T-I/PT

PIC18F27/47Q10

PIC18F27/47Q10 Silicon Errata and Data Sheet Clarifications

The PIC18F27/47Q10 devices you have received conform functionally to the current device data sheet (DS40002043E), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC18F27/47Q10 silicon.

Note: This document summarizes all silicon errata issues from all silicon revisions, previous and current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID	
		A4	B2
PIC18F27Q10	0x7100	0xA004	0xA042
PIC18F47Q10	0x70E0	0xA004	0xA042

Important: Refer to the **Device/Revision ID** section in the current **"PIC18F2X/4XQ10 Memory Programming Specification"** (DS40001874) for more detailed information on Device Identification and Revision IDs for your specific device.

Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions	
				A4	B2
Electrical Specifications	Temperature range	1.1.1	Industrial temperature range only	X	
Electrical Specifications	Sleep current	1.1.2	Higher current after DFM write operation	X	
Resets	$\overline{\text{RMCLR}}$ flag	1.2.1	POR may clear the $\overline{\text{RMCLR}}$ bit by mistake	X	X
Resets	LPBOR	1.2.2	Trip point rises with temperature	X	
CWG	Auto-shutdown sources	1.3.1	CLC2 and CLC6 not available	X	
ADCC	FVR reference	1.4.1	Missing codes when using FVR as reference	X	X
ADCC	Burst average	1.4.2	ADCNT may not increment	X	
ADCC	ADCRC (FRC) oscillator	1.4.3	Oscillator continues to run in Sleep mode after conversion	X	
ADCC	Input slew rate	1.4.4	Unreliable conversion results with fast falling slew rate	X	X
WWDT	Window operation	1.5.1	The window feature of WWDT does not operate correctly in Doze mode	X	
NVM	NVMERR	1.6.1	The NVMERR bit is set by device Reset after being cleared by the software	X	
NVM	Self-writes	1.6.2	Do not write above 85°C		X
Oscillator	HFINTOSC	1.7.1	5% variation over temperature range	X	
Oscillator	XT mode	1.7.2	Maximum clock frequency limited to 2 MHz for XT mode	X	
In-Circuit Debug	Software breakpoints	1.8.1	Software breakpoints are not available	X	X
PFM-Program Flash Memory	Self-Write	1.9.1	The First Instruction Following a Self-write Instruction may not Execute.	X	X

Note: Only issues indicated in the last column apply to the current silicon revision.

1. Silicon Errata Issues

CAUTION **Notice:** This document summarizes all silicon errata issues from all revisions of silicon, previous and current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1 Module: Electrical Specifications

1.1.1 Industrial Temperature Range Only

Extended temperature range devices are not released.

Work around
Operate at or below 85°C.

Affected Silicon Revisions

A4	B2
X	

1.1.2 Sleep Current - Higher Sleep Current After DFM Write Operation

The system clock will stay Active when performing a DFM write operation during Sleep mode once completing the write operation, meaning a higher Sleep current will be experienced when the device remains in this state.

Work around
Once completing the DFM write operation, wake the device up from Sleep mode and re-execute a new Sleep command.

Affected Silicon Revisions

A4	B2
X	

1.2 Module: Resets

1.2.1 The $\overline{\text{RMCLR}}$ Flag in the PCON0 Register Cleared by Mistake

On an initial power-up of the device or when executing a software Reset, the $\overline{\text{RMCLR}}$ flag in the PCON0 register may be improperly cleared by a Power-on Reset (POR) or software Reset ($\overline{\text{RI}}$), thereby indicating a false $\overline{\text{MCLR}}$ event.

Work around
None.

Affected Silicon Revisions

A4	B2
X	X

1.2.2 Low-Power Brown-out Reset (LPBOR) Mode

The Brown-out Reset trip level increases proportionally with temperature to a level where BOR is never released. LPBOR cannot be used reliably because the trip level relative to temperature is indeterminate.

Work around
Use the Normal-Power BOR mode.

Affected Silicon Revisions

A4	B2
X	

1.3 Module: Complementary Waveform Generator (CWG)

1.3.1 CWG Auto-Shutdown Sources

Shutdown sources AS6E (CLC2_out) and AS7E (CLC6_out) are unavailable.

Work around
Route the CLC output through PPS to an output pin, and use the AS0E source selection (the pin selected by CWGxPPS) and PPS controls to select the same pin as the shutdown source.

Affected Silicon Revisions

A4	B2
X	

1.4 Module: Analog-to-Digital Converter with Computation (ADCC)

1.4.1 Missing Codes with FVR Reference

Using the FVR as the positive voltage reference for the ADC can cause an increase in missing codes.

Work around
Method 1:

Increase the bit conversion time, known as T_{AD}, to 8 µs or higher.

Method 2:

Use V_{DD} as the positive voltage reference to the ADC.

Affected Silicon Revisions

A4	B2
X	X

1.4.2 ADCC Burst Average Mode

When the ADCC is operated in Burst Average mode (ADMD = `0b011` in the ADCON2 register) while enabling noncontinuous operation and double-sampling (ADCONT = `0` in the ADCON0 register and ADDSEN = `1` in the ADCON1 register), the value in the ADCNT register does not increment beyond '`0b1`' toward the value in the ADRPT register.

Work around
When operating the ADCC in Burst Average mode with double-sampling, enable continuous module operation (ADCONT = 1 in the ADCON0 register) and set the Stop-on-Interrupt bit (the ADSOI bit in the ADCON3 register). After the interrupt occurs, perform appropriate threshold calculations in the software and retrigger ADCC as necessary.

Alternatively, if the CPU is in Low-Power Sleep mode, the ADCC in noncontinuous Burst Average mode can be operated with a single ADC conversion (ADDSEN = 0 in the ADCON1 register). Doing so compromises noise immunity for lower power consumption by preventing the device from waking up to perform threshold calculations in the software.

Affected Silicon Revisions

A4	B2
X	

1.4.3 ADCRC (FRC) Oscillator Operation in Sleep Mode

If the part is in Sleep mode and the ADCRC (FRC) oscillator is used as clock source to the ADC, the oscillator continues to run after the conversion is complete, increasing the current consumption in Sleep mode. The oscillator will stop after the device exits Sleep mode and resumes normal code execution.

Work around
None.

Affected Silicon Revisions

A4	B2
X	

1.4.4 Unreliable Conversion Results with Fast Falling Slew Rate

When the ADC input falls by greater than 3.2V, with a slew rate faster than -11 V/µs, the following ADC conversion will have the Most Significant bit (MSb) improperly set. This is likely to happen when the ADC input channel is switched from one with a high input level to another with a low input level.

Work around
When switching between input channels, discard the first conversion result after the switch. Subsequent conversions will not be affected.

Affected Silicon Revisions

A4	B2
X	X

1.5 Module: Windowed Watchdog Timer (WWDT)

1.5.1 Window Operation in Doze Mode

When enabling the Windowed operation mode in Doze mode, a window violation error is issued even though the window is open and armed. This condition occurs only when the window size is set to a value other than 100% open.

Work around
Method 1:

Use the Windowed operation mode in any mode other than Doze. If disabling the Doze mode is not an option, use the WWDT module without enabling the window.

Method 2:

If the device is in Doze mode, perform the arming process for the window in Normal mode and return to the Doze mode.

Method 3:

If there is an Interrupt Service Routine (ISR) in the application code, the arming within the window can be done inside the ISR with the ROI bit of the CPUDOZE register being set.

Affected Silicon Revisions

A4	B2
X	

1.6 Module: Nonvolatile Memory (NVM)

1.6.1 NVMERR

When a Reset is issued while an NVM high-voltage operation is in progress, the NVMERR bit in the NVMCON0 register is set as expected. After clearing the NVMERR bit, if a Reset reoccurs, the NVMERR bit is set again regardless of whether an NVM operation is in progress or not. A successful write operation will clear the NVMERR condition.

Work around
None.

Affected Silicon Revisions

A4	B2
X	

1.6.2 PFM Writes Above 85° Celsius

Do not perform write operations on the Program Flash Memory (PFM) when the temperature exceeds 85°C.

Work around
Perform PFM writes below 85°C.

Affected Silicon Revisions

A4	B2
	X

1.7 Module: Oscillator

1.7.1 Internal HFINTOSC Oscillator Varies up to 5%

The internal HFINTOSC oscillator frequency varies up to 5% over the voltage and temperature range.

Work around
For systems requiring more precision, use an external crystal or ceramic resonator in one of the external oscillator modes.

Affected Silicon Revisions

A4	B2
X	

1.7.2 Maximum Clock Frequency Limited to 2 MHz for XT Mode

The maximum clock frequency for the intermediate gain setting that supports quartz crystal and ceramic resonator operation (XT mode) is being reduced from 4 MHz to 2 MHz.

Work around

For crystal or resonator frequencies above 2 MHz, use HS mode.

Affected Silicon Revisions

A4	B2
X	

1.8 Module: In-Circuit Debug

1.8.1 Software Breakpoints Are Not Available

When debugging code, software breakpoints will not be available.

Work around

None.

Affected Silicon Revisions

A4	B2
X	X

1.9 Module: Program Flash Memory (PFM)

1.9.1 The First Instruction Following a Self-Write Instruction May Not Execute

When performing a self-write operation to Program Flash Memory, the first instruction following a self-write instruction may not execute.

Work around

Add two all-zero `NOP()` macros immediately after the self-write instruction. The all-zero `NOP()` macros are included automatically when the `#include <xc.h>` directive is used in user software.

Affected Silicon Revisions

A4	B2
X	X

2. Data Sheet Clarifications

Note the following typographic corrections and clarifications for the latest version of the device data sheet (DS40002043E):

Note:

Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1 Table 1 - 28-pin Allocation Table

The output pin allocations for SDO2 and SCK2 are omitted from the table. The correct table is shown below:

I/O(2)	28-Pin SPDIP, SOIC, SSOP	28-Pin (V)QFN	A/D	Reference	Comparator	Timers	CCP	CWG	ZCD	Interrupt	EUSART	DSM	MSSP	Pull-up	Basic
RA0	2	27	ANA0	—	C1IN0- C2IN0-	—	—	—	—	IOCA0	—	—	—	Y	—
RA1	3	28	ANA1	—	C1IN1- C2IN1-	—	—	—	—	IOCA1	—	—	—	Y	—
RA2	4	1	ANA2	DAC1OUT1 V_{REF-} (DAC) V_{REF-} (ADC)	C1IN0+ C2IN0+	—	—	—	—	IOCA2	—	—	—	Y	—
RA3	5	2	ANA3	V_{REF+} (DAC) V_{REF+} (ADC)	C1IN1+	—	—	—	—	IOCA3	—	MDCARL(1)	—	Y	—
RA4	6	3	ANA4	—	—	T0CKI(1)	—	—	—	IOCA4	—	MDCARH(1)	—	Y	—
RA5	7	4	ANA5	—	—	—	—	—	—	IOCA5	—	MDSRC(1)	$\overline{SS1}$(1)	Y	—
RA6	10	7	ANA6	—	—	—	—	—	—	IOCA6	—	—	—	Y	CLKOUT OSC2
RA7	9	6	ANA7	—	—	—	—	—	—	IOCA7	—	—	—	Y	OSC1 CLKIN
RB0	21	18	ANB0	—	C2IN1+	—	—	CWG1(1)	ZCDIN	IOCB0 INT0(1)	—	—	$\overline{SS2}$(1)	Y	—
RB1	22	19	ANB1	—	C1IN3- C2IN3-	—	—	—	—	IOCB1 INT1(1)	—	—	SCK2(1) SCL2(3,4)	Y	—
RB2	23	20	ANB2	—	—	—	—	—	—	IOCB2 INT2(1)	—	—	SDI2(1) SDA2(3,4)	Y	—
RB3	24	21	ANB3	—	C1IN2- C2IN2-	—	—	—	—	IOCB3	—	—	—	Y	—
RB4	25	22	ANB4	—	—	T5G(1)	—	—	—	IOCB4	—	—	—	Y	—
RB5	26	23	ANB5	—	—	T1G(1)	—	—	—	IOCB5	—	—	—	Y	—
RB6	27	24	ANB6	—	—	—	—	—	—	IOCB6	—	—	—	Y	ICSPCLK
RB7	28	25	ANB7	DAC1OUT2	—	T6IN(1)	—	—	—	IOCB7	—	—	—	Y	ICSPDAT
RC0	11	8	ANC0	—	—	T1CKI(1) T3CKI(1) T3G(1)	—	—	—	IOCC0	—	—	—	Y	SOSCO
RC1	12	9	ANC1	—	—	—	CCP2(1)	—	—	IOCC1	—	—	—	Y	SOSCIN SOSCI
RC2	13	10	ANC2	—	—	T5CKI(1)	CCP1(1)	—	—	IOCC2	—	—	—	Y	—
RC3	14	11	ANC3	—	—	T2IN(1)	—	—	—	IOCC3	—	—	SCK1(1) SCL1(3,4)	Y	—

.....continued															
I/O(2)	28-Pin SPDIP, SOIC, SSOP	28-Pin (V)QFN	A/D	Reference	Comparator	Timers	CCP	CWG	ZCD	Interrupt	EUSART	DSM	MSSP	Pull-up	Basic
RC4	15	12	ANC4	—	—	—	—	—	—	IOCC4	—	—	SDI1(1) SDA1(3,4)	Y	—
RC5	16	13	ANC5	—	—	T4IN(1)	—	—	—	IOCC5	—	—	—	Y	—
RC6	17	14	ANC6	—	—	—	—	—	—	IOCC6	CK1(1,3)	—	—	Y	—
RC7	18	15	ANC7	—	—	—	—	—	—	IOCC7	RX1/DT1(1,3)	—	—	Y	—
RE3	1	26	—	—	—	—	—	—	—	IOCE3	—	—	—	Y	Vpp/MCLR
VSS	19	16	—	—	—	—	—	—	—	—	—	—	—	—	VSS
VDD(5)	20	17	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	8	5	—	—	—	—	—	—	—	—	—	—	—	—	VSS
OUT(2)	—	—	ADGRDA ADGRDB	—	C1OUT C2OUT	TMR0	CCP1 CCP2 PWM3 PWM4	CWG1A CWG1B CWG1C CWG1D	—	—	TX1/CK1(3) DT1(3)	DSM	SDO1 SCK1 **SDO2** **SCK2**	—	—

Notes:

1. This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to the peripheral input selection table for details on which port pins to use for this signal.
2. All output signals shown in this row are PPS remappable. As described in the peripheral output selection table, these signals may be mapped to output onto one of several PORTx pin options.
3. This is a bidirectional signal. The firmware may map this signal to the same pin in the PPS input and output registers for ordinary module operation.
4. These pins are configured for I^2C logic levels; the SCLx/SDAx signals may be assigned to any of these pins. PPS assignments to the other pins (e.g., RB1) will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register instead of the I^2C specific or SMBus input buffer thresholds.
5. A 0.1 µF bypass capacitor to V_{SS} is required on the V_{DD} pin.

3. Appendix A: Revision History

Doc Rev.	Date	Comments
F	11/2022	Added silicon erratum item 1.9.1.
E	07/2021	Removed silicon erratum item 1.4.4. Minor editorial corrections.
D	01/2021	Added silicon erratum item 1.8.1. Minor editorial corrections.
C	09/2020	Added new silicon Rev B2 and silicon erratum item 1.6.2
B	08/2020	Updated Table 1, Data Sheet Clarification section. Added silicon erratum items 1.2.2 and 1.7.2. Minor editorial corrections.
A	04/2019	Initial document release

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