



MACRONIX INTERNATIONAL CO., LTD.

Product/Process Change Notice

PCN # P-2209-0007

Date: 2022/11/25

Dear Customer:

Please be informed that Macronix is going to add 2nd source assembly subcontractor to backup customer original approved assembly subcontractors for 56TSOP package products. The 2nd source assembly subcontractor is ChipMOS.

The detailed information about this change is described in the following pages. This process change has passed Macronix' qualification based on JEDEC standard, and the qualification report is attached below.

If you have any questions, concerns, or requests about this change, please contact your local Macronix Sales Representatives within 30 days, otherwise Macronix will assume customer received the PCN with no comments and the change is acceptable to the customer. Macronix follows JEDEC J-STD-046, which stipulates: ".....Lack of acknowledgement of the PCN within 30 days constitutes acceptance of the change".

Thank you.

Macronix International Co., Ltd.

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PCN No.: P-2209-0007**Issue Date :** 2022/11/25**Subject:** Adding a new assembly vendor—ChipMOS for 56TSOP package products.**Affected Macronix Part No.:**

MX68GL1G0FHT2I-11G
 MX68GL1G0FLT2I-11G
 MX29GL512FHT2I-11G
 MX29GL512FLT2I-11G
 MX29GL512FDT2I-11G
 MX29GL512FUT2I-11G

Package type: 56TSOP package products**Change Category :** New assembly vendor**Reason of Change:**

To increase 56TSOP package assembly capacity and flexibility..

Before Change :

Assembly vendors:

1. SPIL
2. LINGSEN(For MX29GL512F*T2I-11G only)

After Change :

Assembly vendors:

1. SPIL
2. LINGSEN(For MX29GL512F*T2I-11G only)
3. ChipMOS

Product identification:

SPIL assembled IC the marking has vendor code: S

LINGSEN assembled IC the marking has vendor code: L

ChipMOS assembled IC the marking has vendor code: a

Assessment of Change:

1. No impact to Form, Fit, Function, Quality & Reliability.
2. ChipMOS assembled 56TSOP package has passed Macronix' qualification based on JEDEC MSL level 3 standards, and it is also Halogen-Free, and meets the RoHS standards.
 * Attached is ChipMOS assembled 48TSOP package qualification report.
3. ChipMOS has been one of Macronix' qualified assembly vendors with good quality for a long time.

Schedule:

Sample available date: 2022/12/1

1st shipping date: 2023/3/1 (Or follow PCN agreement with the customer)



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ChipMOS 56TSOP Package Qualification Report

1. PURPOSE:

To qualify the new assembly subcontractor “ChipMOS” for 56TSOP package.

2. PACKAGE PROFILE:

ASSEMBLY HOUSE	ChipMOS
PACKAGE	56TSOP (14X20 mm)
DIE SIZE	6709 7016 x 8386 μm^2
DIE ATTACH	Nitto EM-760
LEAD FRAME	Copper, Double Ring Silver
WIRE BOND MATERIAL	Au
MOLD COMPOUND	Showa Denko CEL-9740HF
LEAD FINISH	Matte Sn

3. QUALIFICATION ITEMS, TEST CONDITION AND FLOW:

3-1. QUALIFICATION ITEMS:

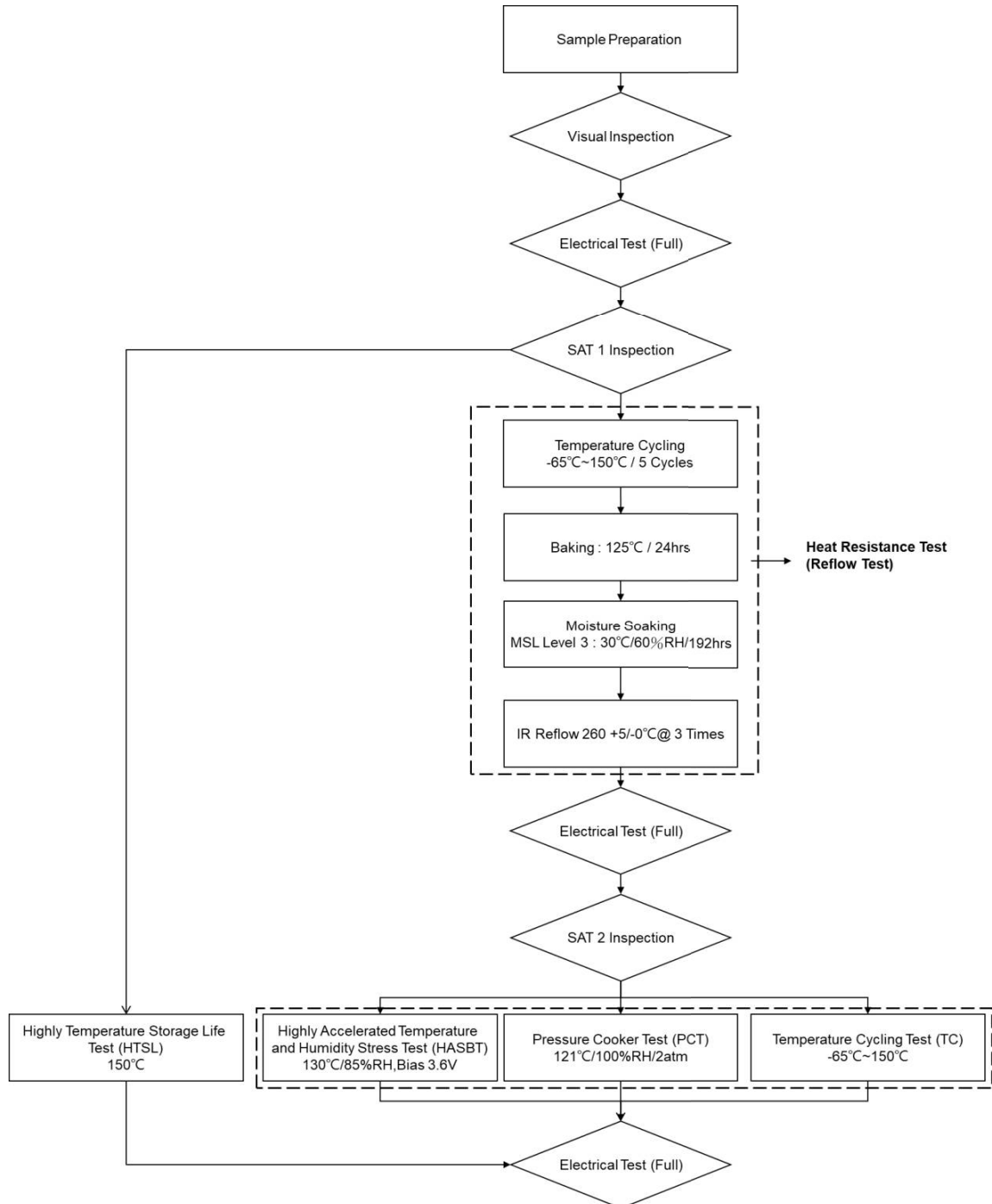
Test Item	Reference	Test Condition
1. Heat Resistance Test: Reflow Test	JEDEC J-STD-020	MSL: Follow JEDEC MSL Level 3 (30°C/ 60%RH, 192hrs)
2. Pressure Cooker Test	JESD22-A102	121°C/ 100%RH/ 2atm
3. Temperature Cycling Test	JESD22-A104	-65°C ~150°C
4. Highly Accelerated Temperature and Humidity Stress Test	JESD22-A110	130°C/ 85% RH, Bias: 3.6V
5. High Temperature Storage Life Test	JESD22-A103	150°C
6. Solderability Test	JESD22-B102	■ Steam aging 8hrs & Dipping Time $\leq$ 5sec ■ Sn-Ag-Cu solder paste: 245°C ■ Sn-Pb solder paste: 235°C

*Perform SAT examination before and after Preconditioning per JESD22-A112.



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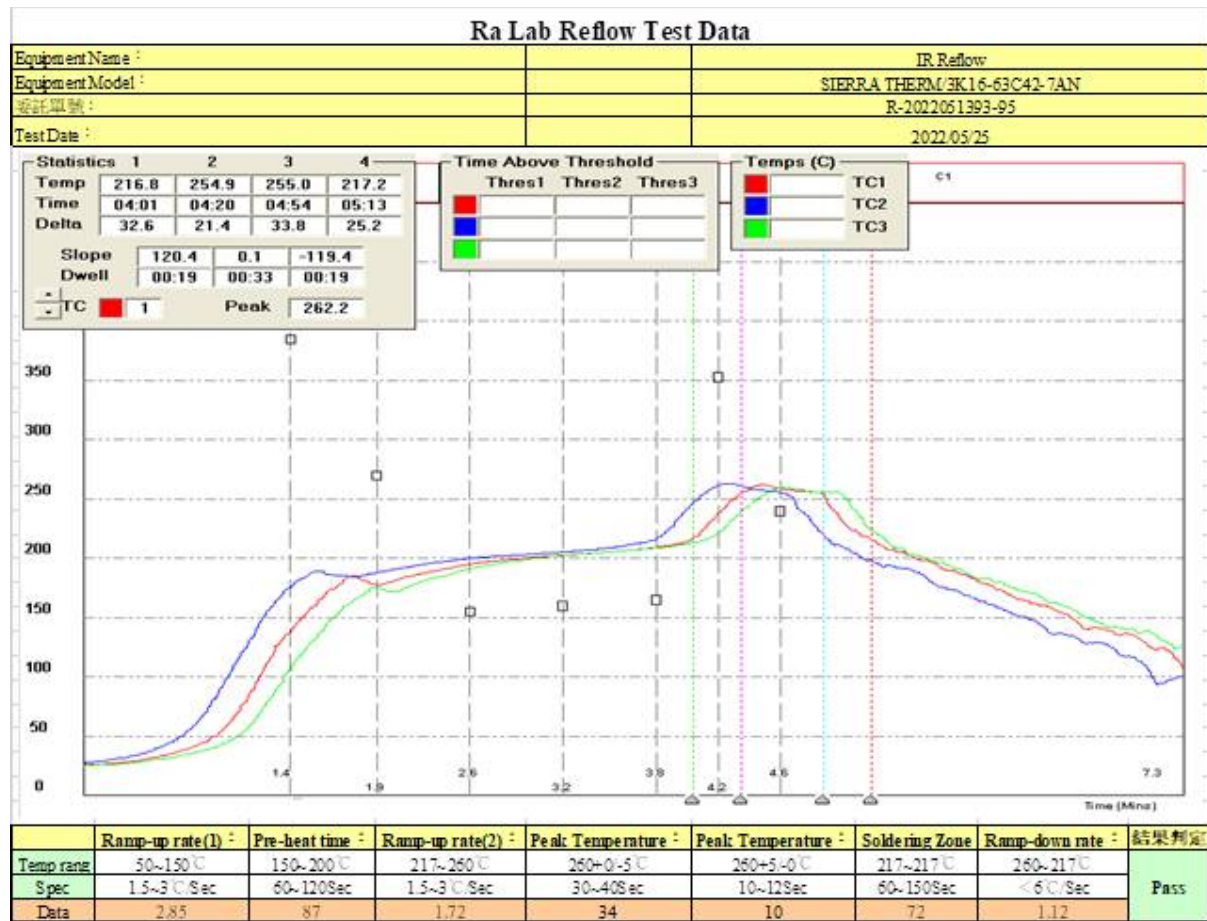
3-2. PRECONDITIONING AND RELIABILITY TEST FLOW:





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3-2-1. REFLOW PROFILE:



Note 1: Subject the samples to 3 cycles of the above defined reflow conditions

Note 2: Time 25°C to peak temperature: 8 minutes max.

Note 3: The time between reflows shall be 5 minutes minimum and 40 minutes maximum.

3-2-2. CRITERIA:

LTPD= 3%, PCT 96 hours and TC 500 cycles and HAST 96 hours

LTPD= 3%, HTSL 1000 hours.

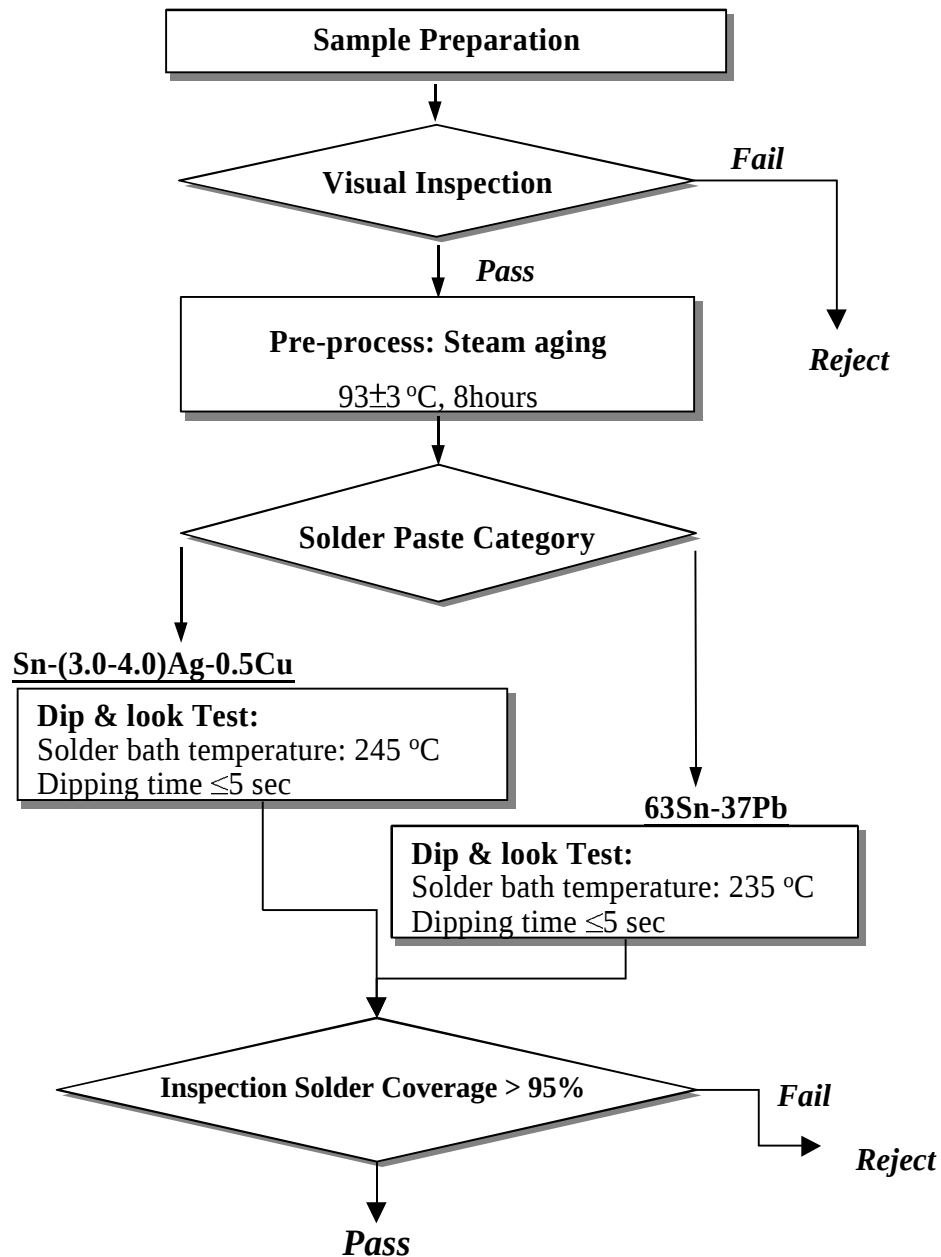
3-2-3. REFERENCE SPECIFICATION:

5650-0901: ASSEMBLY RELIABILITY QUALIFICATION SPEC.



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3-3. SOLDERABILITY TEST FLOW





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4. RESULTS:

4-1. HEAT RESISTANCE TEST AND RELIABILITY TEST RESULTS:

PRODUCT	6709		
LOT#	8J371903BL	8J371903BS	8J371903BT
DATE CODE	a2216	a2216	a2217
SAT 1	0/22	0/22	0/22
PRECON	0/231	0/231	0/231
SAT 2	0/22	0/22	0/22
PCT 96 HRS	0/77	0/77	0/77
TC 500 CYC	0/77	0/77	0/77
HAST 96 HRS	0/77	0/77	0/77
HTSL 1000 HRS	0/77	0/77	0/77

FAIL / SAMPLE SIZE

4-2. SOLDERABILITY TEST RESULTS:

Matte Sn Plating

Plating Material	Matte Sn		
Solder Paste Material	Sn-(3.0-4.0)Ag-0.5Cu		
INSPECTION	0/5	0/5	0/5

FAIL / SAMPLE SIZE

Plating Material	Matte Sn		
Solder Paste Material	63Sn-37Pb		
INSPECTION	0/5	0/5	0/5

FAIL / SAMPLE SIZE

5. CONCLUSION: PASS

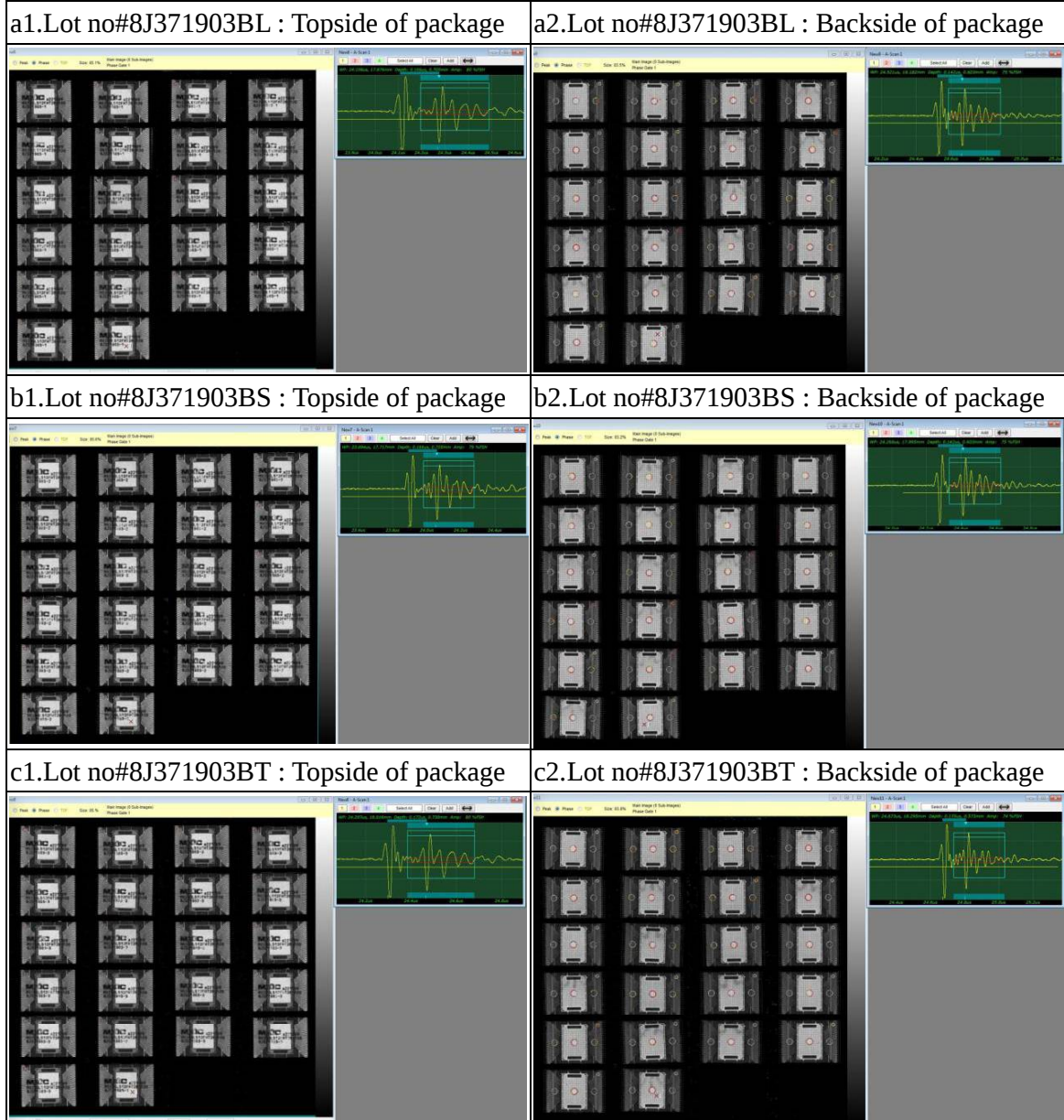


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6. ATTACHED FILE:

6-1. SAT photo

6-1-1. Before pre-condition

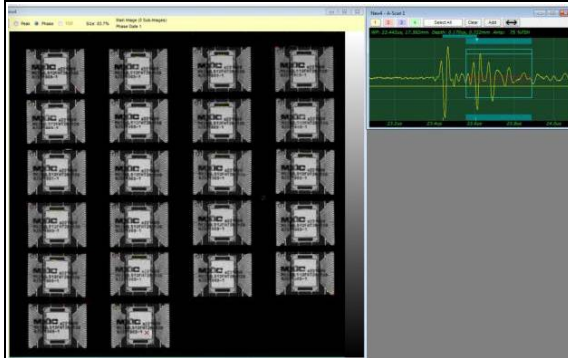




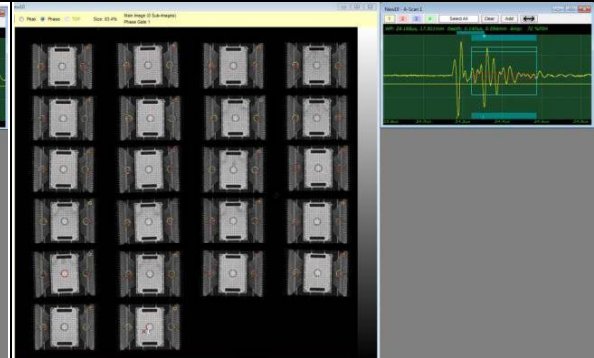
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6-1-2. After pre-condition

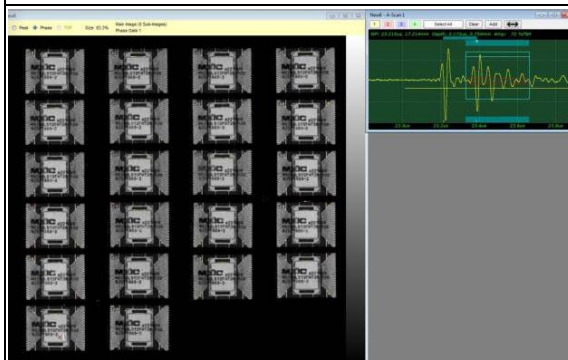
a1.Lot no#8J371903BL : Topside of package



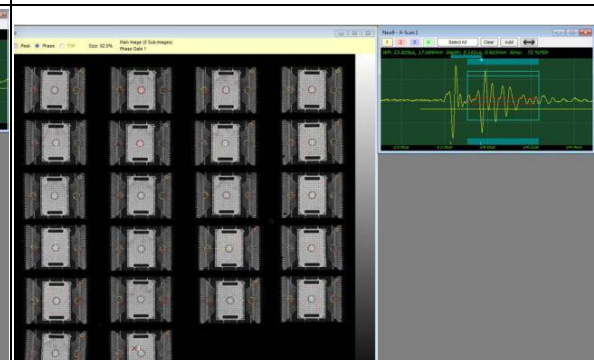
a2.Lot no#8J371903BL : Backside of package



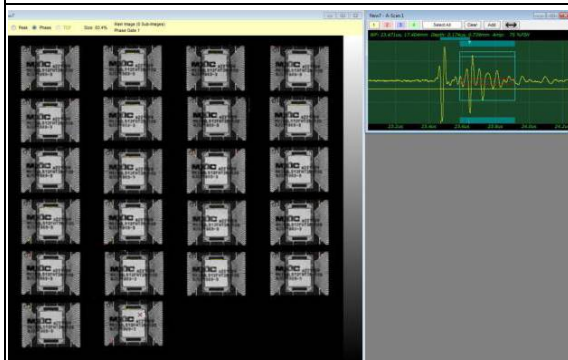
b1.Lot no#8J371903BS : Topside of package



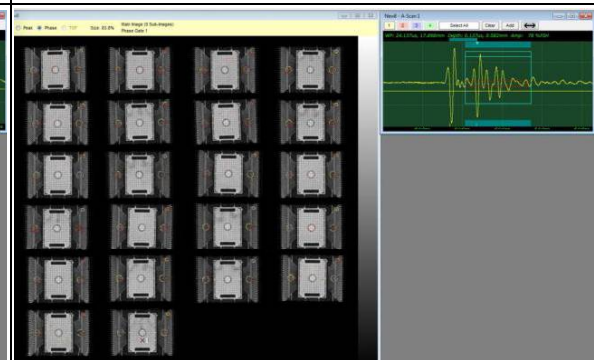
b2.Lot no#8J371903BS : Backside of package



c1.Lot no#8J371903BT : Topside of package



c2.Lot no#8J371903BT : Backside of package





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ChipMOS 56TSOP(STACK DIE) Package Qualification Report

1. PURPOSE:

To qualify the new assembly subcontractor “ChipMOS” for 56TSOP(STACK DIE) package.

2. PACKAGE PROFILE:

ASSEMBLY HOUSE	ChipMOS
PACKAGE	56TSOP (14X20 mm) (STACK DIE)
DIE SIZE	6709L : 7016 x 8386 μm^2 (Top Die) 6709X : 7016 x 8386 μm^2 (Btm Die)
DIE ATTACH	Nitto EM-310 (Top Die) Nitto EM-760 (Btm Die)
LEAD FRAME	Copper, Double Ring Silver
WIRE BOND MATERIAL	Au
MOLD COMPOUND	Showa Denko CEL-9740HF
LEAD FINISH	Matte Sn
STRUCTURE	

3. QUALIFICATION ITEMS, TEST CONDITION AND FLOW:

3-1. QUALIFICATION ITEMS:

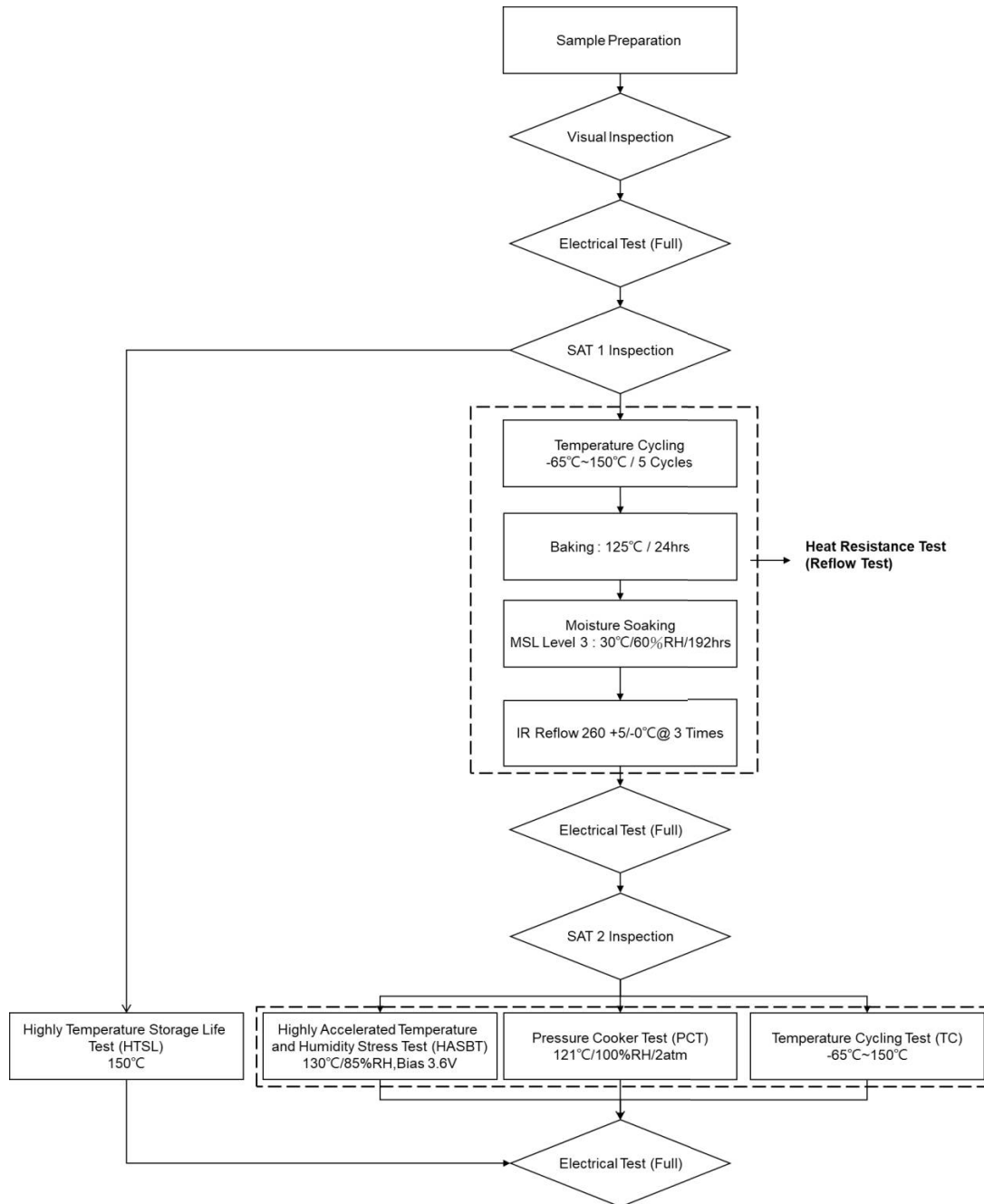
Test Item	Reference	Test Condition
1. Heat Resistance Test: Reflow Test	JEDEC J-STD-020	MSL: Follow JEDEC MSL Level 3 (30°C/ 60%RH, 192hrs)
2. Pressure Cooker Test	JESD22-A102	121°C/ 100%RH/ 2atm
3. Temperature Cycling Test	JESD22-A104	-65°C ~150°C
4. Highly Accelerated Temperature and Humidity Stress Test	JESD22-A110	130°C/ 85% RH, Bias: 3.6V
5. High Temperature Storage Life Test	JESD22-A103	150°C
6. Solderability Test	JESD22-B102	■ Steam aging 8hrs & Dipping Time $\leq$ 5sec ■ Sn-Ag-Cu solder paste: 245°C ■ Sn-Pb solder paste: 235°C

*Perform SAT examination before and after Preconditioning per JESD22-A112.



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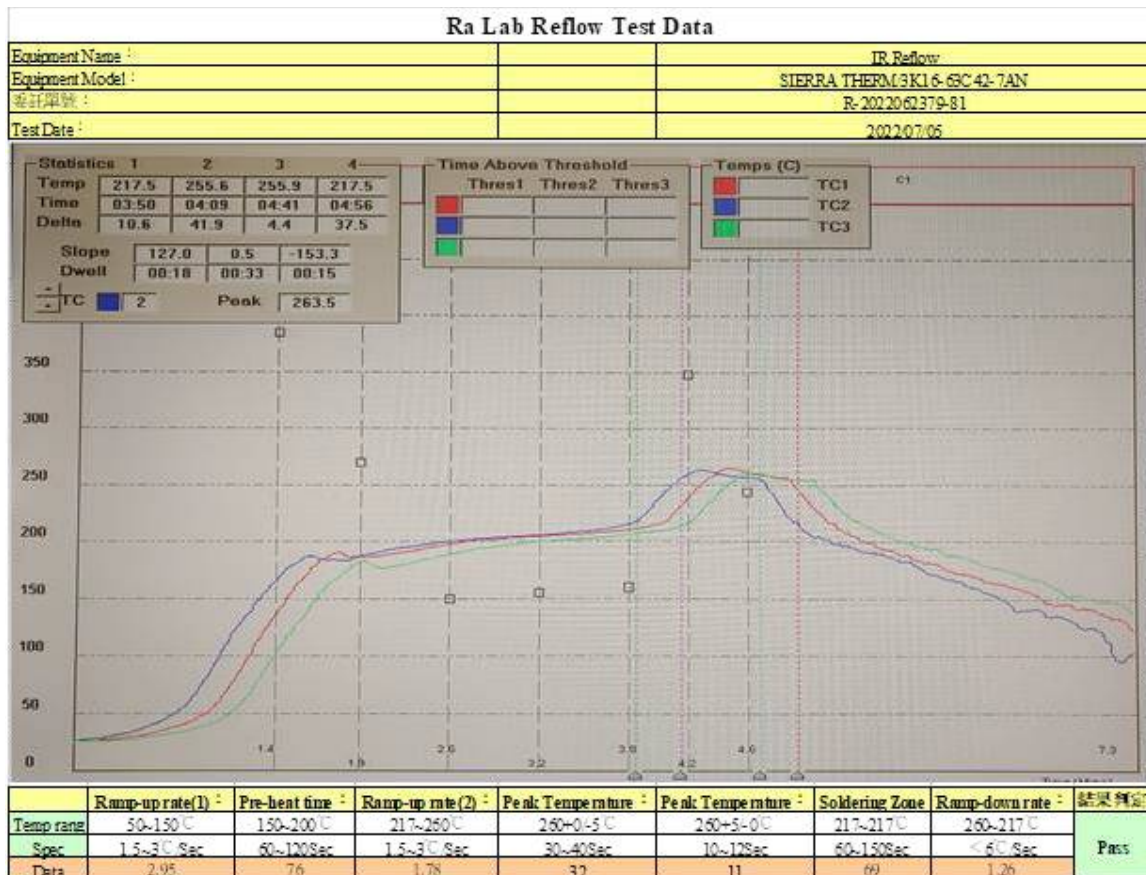
3-2. PRECONDITIONING AND RELIABILITY TEST FLOW:





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3-2-1. REFLOW PROFILE:



Note 1: Subject the samples to 3 cycles of the above defined reflow conditions

Note 2: Time 25°C to peak temperature: 8 minutes max.

Note 3: The time between reflows shall be 5 minutes minimum and 40 minutes maximum.

3-2-2. CRITERIA:

LTPD= 3%, PCT 96 hours and TC 500 cycles and HAST 96 hours

LTPD= 3%, HTSL 1000 hours.

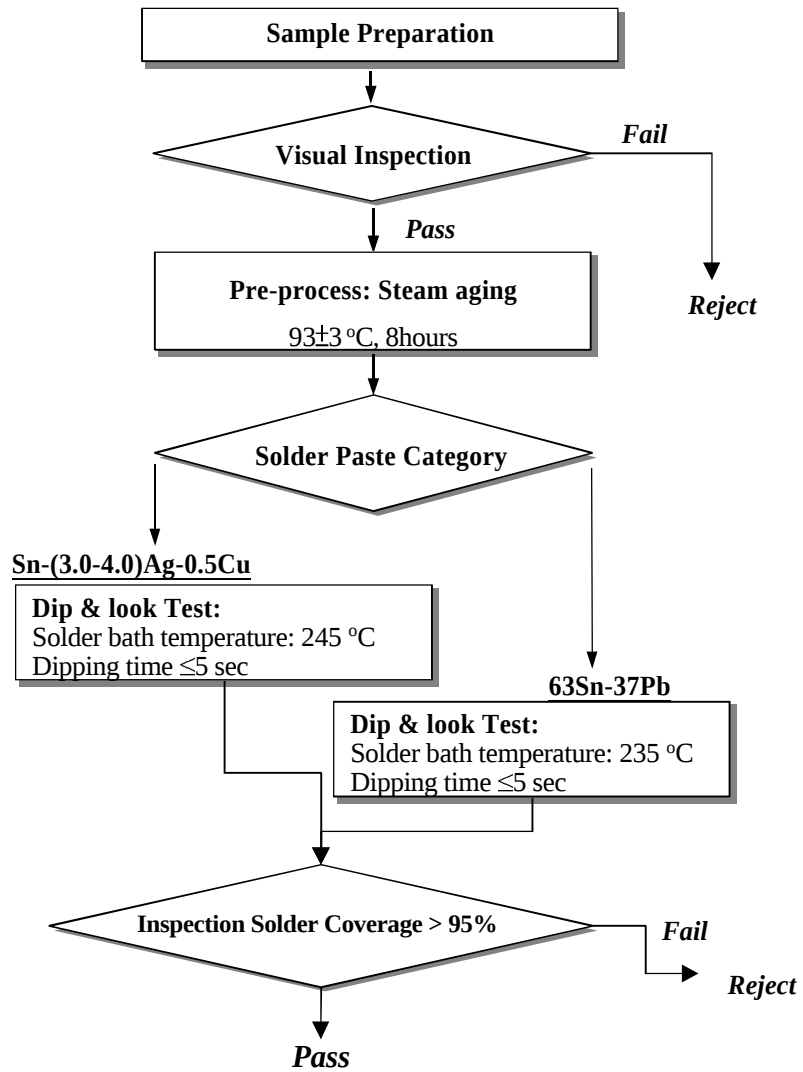
3-2-3. REFERENCE SPECIFICATION:

5650-0901: ASSEMBLY RELIABILITY QUALIFICATION SPEC.



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3-3. SOLDERABILITY TEST FLOW





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4. RESULTS:

4-1. HEAT RESISTANCE TEST AND RELIABILITY TEST RESULTS:

PRODUCT	6115		
LOT#	8J256000J1	8J256000J1	8J256000J1
DATE CODE	a2219	a2219	a2219
SAT 1	0/22	0/22	0/22
PRECON	0/231	0/231	0/231
SAT 2	0/22	0/22	0/22
PCT 96 HRS	0/77	0/77	0/77
TC 500 CYC	0/77	0/77	0/77
HAST 96 HRS	0/77	0/77	0/77
HTSL 1000 HRS	0/77	0/77	0/77

FAIL / SAMPLE SIZE

4-2. SOLDERABILITY TEST RESULTS:

Matte Sn Plating

Plating Material	Matte Sn		
Solder Paste Material	Sn-(3.0-4.0)Ag-0.5Cu		
INSPECTION	0/5	0/5	0/5

FAIL / SAMPLE SIZE

Plating Material	Matte Sn		
Solder Paste Material	63Sn-37Pb		
INSPECTION	0/5	0/5	0/5

FAIL / SAMPLE SIZE

5. CONCLUSION: PASS

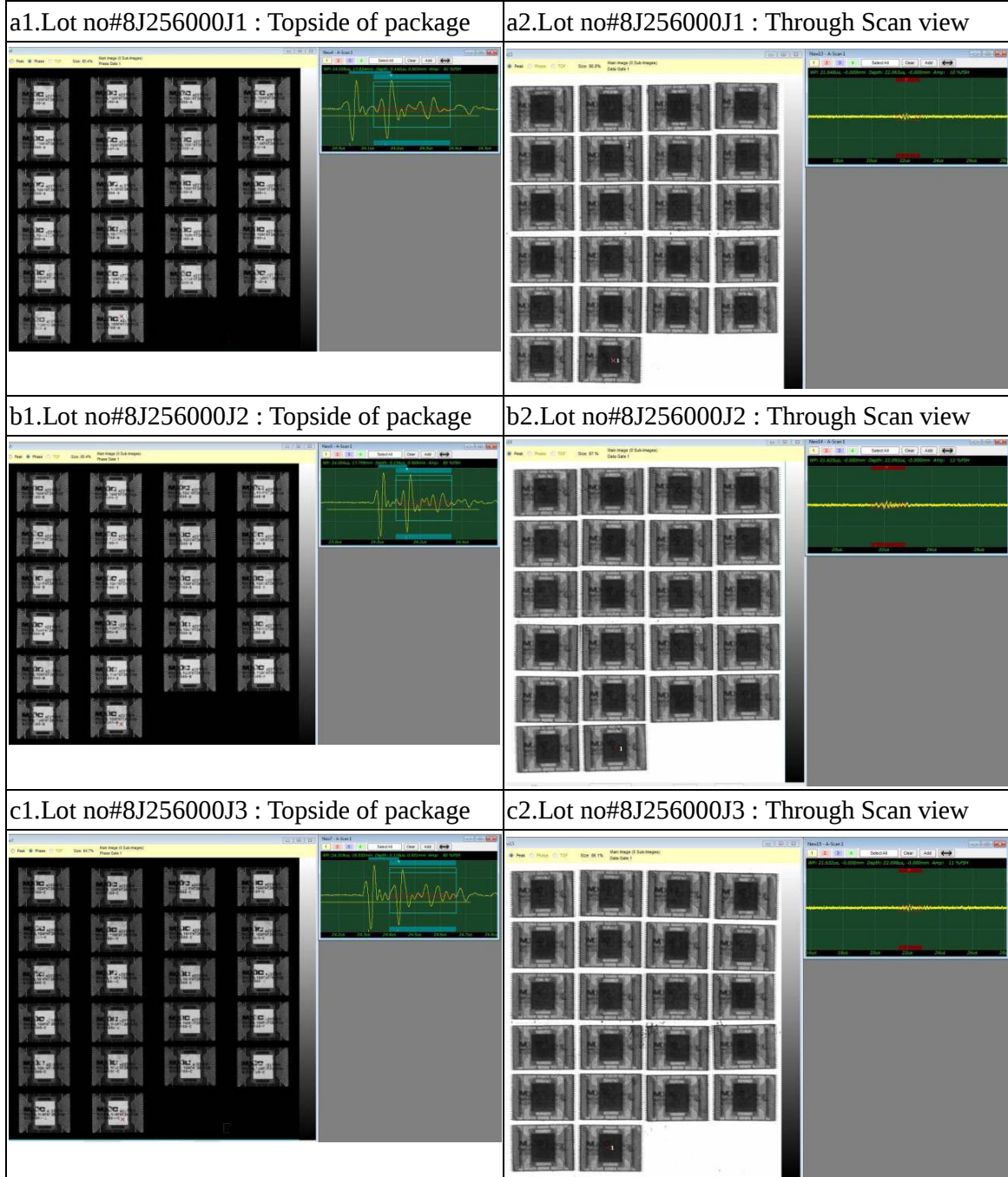


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6. ATTACHED FILE:

6-1. SAT photo

6-1-1. Before pre-condition

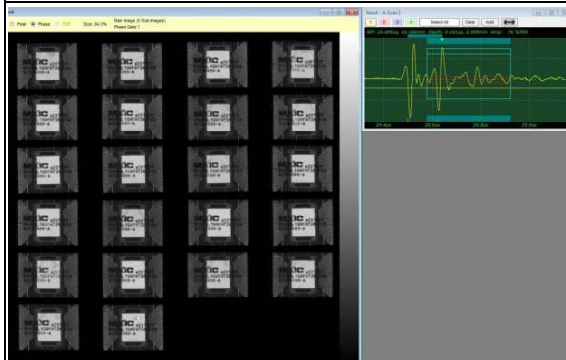




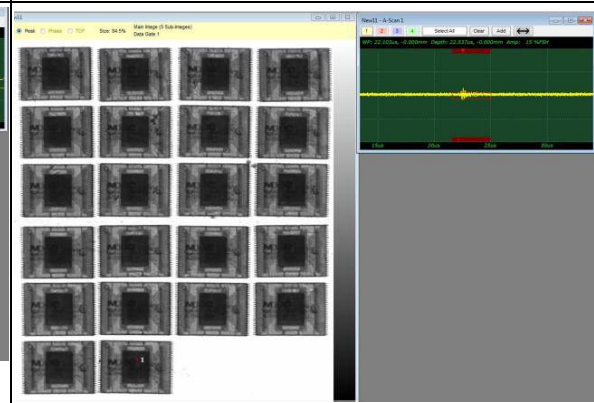
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6-1-2. After pre-condition

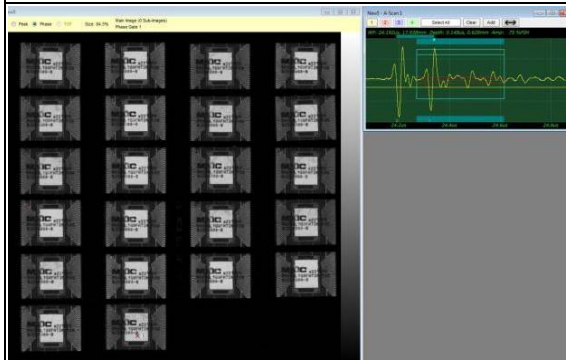
a1.Lot no#8J256000J1 : Topside of package



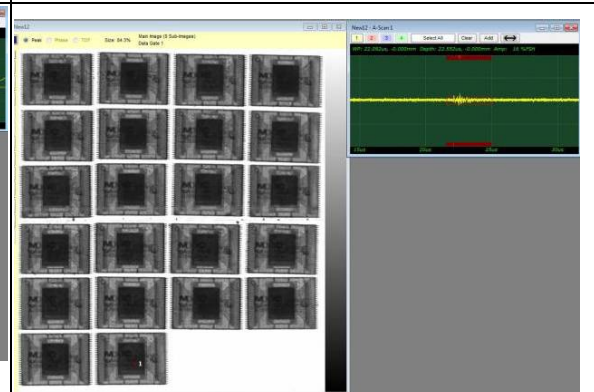
a2.Lot no#8J256000J1 : Through Scan view



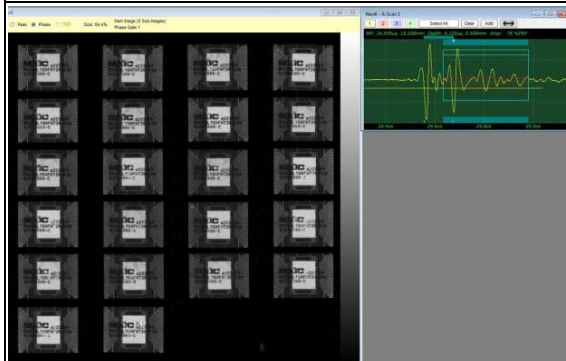
b1.Lot no#8J256000J2 : Topside of package



b2.Lot no#8J256000J2 : Through Scan view



c1.Lot no#8J256000J3 : Topside of package



c2.Lot no#8J256000J3 : Through Scan view

