Product/process change notification

PCN N° 2022-029-A

Dear customer,

Please find attached our Infineon Technologies AG PCN:

Capacity expansion for IPT030N12N3 G at Infineon Technologies AG, Regensburg, Germany

Important information for your attention:

- Please respond to this PCN by indicating your decision on the approval form, sign it and return to your sales partner before **2022-12-16**
- Infineon aligns with the widely recognized JEDEC STANDARD **"JESD46",** which stipulates: **"Lack of acknowledgement of the PCN within 30 days constitutes acceptance of the change."**

Your prompt reply will help Infineon to assure a smooth and well-executed transition. If Infineon does not hear from your side by the due date, we will assume your full acceptance to this proposed change and its implementation.

Your attention and response to this matter is greatly appreciated.

On 16 April 2020, Infineon acquired Cypress.
We are now in the process of merging and consolidating our tools and processes for PCN, Information Notes, Errata and Product Discontinuance.
For further details, please visit our website:
https://www.infineon.com/cms/en/about-infineon/company/cypress-acquisition/

Infineon Technologies AG
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Chairman of the Supervisory Board Dr. Wolfgang Eder
Management Board Jochen Hanebeck (CEO), Constanze Hufenbecher, Dr. Sven Schneider, Andreas Urschitz, Dr. Rutger Wijburg
Registered office Neubiberg Commercial register Amtsgericht München HRB 126492

Product/process change notification

PCN N° 2022-029-A

▶ Products affected

Please refer to attached affected product list 1_cip22029_a

▶ Detailed change information

Subject

Capacity expansion for IPT030N12N3 G at Infineon Technologies AG, Regensburg, Germany

Reason

Introduction of additional Front-End Site to support continuous increasing customer demand

Description

	Old	New
Wafer Production Site	■ Infineon Technologies (Kulim) Sdn. Bhd., Malaysia	■ Infineon Technologies (Kulim) Sdn. Bhd., Malaysia *and* ■ Infineon Technologies AG, Regensburg, Germany
Wafer Lot Number	■ PFxxxxxx (Kulim)	■ PFxxxxxx (Kulim) *and* ■ RUxxxxxx (Regensburg)

▶ Product identification

External traceability is assured via wafer lot number on product barcode label

▶ Impact of change

NO change on electrical, thermal parameters and reliability as proven via product qualification and characterization

NO change of existing datasheet parameters

NO change in quality and reliability. Processes are optimized to meet product performance according to already applied Infineon specifications

▶ Attachments

1_cip22029_a	affected product list
2_cip22029_a	qualification report

Product/process change notification

PCN N° 2022-029-A

Time schedule

Final qualification report	available
First samples available	available
Intended start of delivery	2022-12-31 or earlier based on customer approval

If you have any questions, please do not hesitate to contact your local sales office.

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Capacity expansion for IPT030N12N3 G at Infineon Technologies AG, Regensburg, Germany

Affected products sold to FUTURE ELECTRONICS INC. (4048201)

Sales name	SP number	OPN	Package	Customer part number
IPT030N12N3 G	SP005348026	IPT030N12N3GATMA1	PG-HSOF-8	

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Capacity expansion for IPT030N12N3 G at Infineon Technologies AG, Regensburg, Germany

Qualification Report

2022-10-18

PCN 2022-029-A

Product Referencing Strategy

- **OptiMOS™3 120V technology qualification refers to 80-100V 200mm in PG-TO263, PG-TO220 and PG-TO252 packages**
  - Technology and product qualification:
    - Final Qualification Report for SFET3 100V OptiMOS™3 from Regensburg, Germany in TO Packages Melaka
    - **Reference Products**: IPB027N10N3 G, IPP028N08N3 G and IPD068N10N3 G

- **OptiMOS™3 package qualification refers to PG-HSOF-8 products assembled Infineon Melaka, Malaysia**
  - Package and product qualification:
    - Qualification of SFET5 60V and SFET3 100/150V within TOLL package
    - **Reference Product:** IPT059N15N3 G

PCN 2022-029-A

OptiMOS™3 120V technology qualification refers to 80-100V 200mm in PG-TO263, PG-TO220 and PG-TO252 packages

>> Final Qualification Report for SFET3 100V OptiMOS3 from Regensburg in TO-Packages Malacca <<

Reason for choosing the following as test vehicles:

IPB027N10N3 G	biggest SFET3 100V OptiMOS3 chip from Rbg in package PG-TO263-3 assembled at MAL
IPD068N10N3 G	medium SFET3 100V OptiMOS3 chip from Rbg in package PG-TO252-3 assembled at MAL
IPP030N10N3 G	biggest SFET3 100V OptiMOS3 chip from Rbg in package PG-TO220-3 assembled at MAL
IPP028N08N3 G	biggest SFET3 80V OptiMOS3 chip from Rbg in package PG-TO220-3 assembled at MAL
IPD053N08N3 G	medium SFET3 80V OptiMOS3 chip from Rbg in package PG-TO252-3 assembled at MAL

Reference Product				IPB027N10N3 G	IPD068N10N3 G	IPP030N10N3 G	IPP028N08N3 G [2]	IPD053N08N3 G [2]
Wafer Technology				SFET3 100V OptiMOS3	SFET3 100V OptiMOS3	SFET3 100V OptiMOS3	SFET3 80V OptiMOS3	SFET3 80V OptiMOS3
Chip type				L9166U	L9167T	L9166T	L9166P	L9167P
Chip size (in mm²)				30.1	10.8	30.1	30.1	10.8
Location wafer fab				Regensburg	Regensburg	Regensburg	Regensburg	Regensburg
Package type				PG-TO263-3 Robust	PG-TO252-3	PG-TO220-3	PG-TO220-3	PG-TO252-3
Assembly line location				Malacca	Malacca	Malacca	Malacca	Malacca
Test description	**Abbr.**	**Condition**	**Readout**	**Result:** 1 lot	**Result:** 1 lot	**Result:** 1 lot	**Result:** 1 lot	**Result:** 1 lot
Pre-Conditioning J-STD-020 JESD22 A-113	**PC***	MSL1 (168h 85°C/ 85% rh) 3*IR reflow at 260°C	–	Level 1 260 °C	Level 1 260 °C	n.a	n.a	Level 1 260 °C
High Temperature Reverse Bias JESD22 A-108	**HTRB***	Ta =Tj max for 1000 h V =100V Vdsmax [1] V =80V Vdsmax	0 h 168 h 500 h 1000 h	0 / 77 0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77 0 / 77
High Humidity High Temp. Reverse Bias JESD22 A-101	**H3TRB ***	85 °C / 85 % r.h. V = 80V [1] V = 64V	0 h 168 h 500 h 1000 h	0 / 77 0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77 0 / 77	refer to IPB027N10N3 G	0 / 77 0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77 0 / 77
High Temperature Gate BIAS JESD22 A-108	**HTGS***	VGS= -20V/+20V Tj max=175°C t: 1000 h	0 h 168 h 500 h 1000 h	0 / 77 0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77 0 / 77	refer to IPB027N10N3 G	0 / 77 0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77 0 / 77
Intermittent Operational Life MIL-STD 750 / Meth.1037	**IOL ***	Delta Tj=100 K for 15 000 cycles	0 h 7500 c 15000 c	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	refer to IPB027N10N3 G	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77
Autoclave JA102	**AC ***	T: 121°C P: 100 Kpa RH: 100 % t: 96 h	0 h 96 h	0 / 77 0 / 77	refer to IPD053N08N3 G	refer to IPP028N08N G	0 / 77 0 / 77	0 / 77 0 / 77
Temperature Cycling JA104	**TC ***	T min: -55°C T max: +150°C n: 1000 cycles	0 c 500 c 1000 c	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77

* PC is done only for SMD Packages before AC, TC, IOL, HTGS, HTRB and H3TRB stress tests

Qualification Report SFET3 100V OptiMOS3 2008-06-24.xls page 1 of 1 Dhillon R.S. 26.06.2008

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OptiMOS™3 package qualification refers to PG-HSOF-8 products assembled Infineon Melaka, Malaysia

Final Qualification Report				Date: 2014-02-26	
Qualification of SFET5 60V and SFET3 100V/150V within TOLL Package					
Reference Products				**IPT007N06N**	**IPT059N15N3**
Wafer Technology, location				OptiMOS_5 60V Villach	OptiMOS_3 150V Regensburg
Chip type				L9980	L9168
Chip sizes chip 1 (mm^2) Chip sizes chip 2 (mm^2)				30.15	30.15
Package type, Assembly line location				PG-HSOF-8 Malacca	PG-HSOF-8 Malacca
Test description	**Abbr.**	**Condition**	**Readout**	**1st lot**	**2nd lot**
Pre-Conditioning J-STD020 / JESD22 A113	**PC**	MSL and 3 x reflow at x°C		**MSL1@260°**	**MSL1@260°**
Temperature Cycling JESD22 A104	**TC***	-55°C - +150°C	0 c PC 500 c 1000 c	0 / 77 0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77 0 / 77
Autoclave JESD22 A102	**AC***	121°C / 100% rh	0h PC 96h	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77
High Humidity High Temp. Reverse Bias JESD22 A101	**H3TRB***	85°C / 85%rh V = 80% VDSmax (60V/150V)	0 h PC 500 h 1000 h	0 / 77 0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77 0 / 77
High Temperature Reverse Bias JESD22 A-108 (Q101)	**HTRB***	Ta =150°C V = VDSmax (60V/150V)	0 h PC 168 h 500 h 1000 h	0 / 77 0 / 77 0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77 0 / 77 0 / 77
High Temperature Gate stress JESD22 A108	**HTGS***	Ta =150°C Vg = ±20V	0 h PC 168 h 500 h 1000 h	0 / 77 0 / 77 0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77 0 / 77 0 / 77
Intermitted Operational Life Test MIL-STD 750/Meth.1037	**IOL***	Delta T=100K for 15 000c	0 c PC 7500 c 15000 c	0 / 77 0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77 0 / 77

* PC is done only for SMD Packages before AC, TC, IOL, HTGS, HTRB and H3TRB stress tests

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