Product Change Notification / SYST-12TGFS747

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32-bit Microcontrollers

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Notification Subject:

ERRATA - PIC32MX1XX/2XX 28/44-pin XLP Family Silicon Errata and Data Sheet Clarification.

Affected CPNs:

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Notification Text:

SYST-12TGFS747

Microchip has released a new Errata for the PIC32MX1XX/2XX 28/44-pin XLP Family Silicon Errata and Data Sheet Clarification. of devices. If you are using one of these devices please read the document located at PIC32MX1XX/2XX 28/44-pin XLP Family Silicon Errata and Data Sheet Clarification..

Notification Status: Final

Description of Change: Added Silicon Issue 54. Flash: RTSP

Impacts to Data Sheet: None

Reason for Change: To improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 13 Oct 2022

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

PIC32MX1XX/2XX 28/44-pin XLP Family Silicon Errata and Data Sheet Clarification.

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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PIC32MX1XX/2XX 28/44-pin XLP Family Silicon Errata and Data Sheet Clarification

The PIC32MX1XX/2XX 28/44-pin XLP family devices that you have received conform functionally to the current Device Data Sheet (DS60001404**E**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC32MX1XX/2XX 28/44-pin XLP family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A3**).

Data Sheet clarifications and corrections start on page 13.

The silicon revision level can be identified using the current version of MPLAB® X IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB X IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB X IDE project.
3. Configure the MPLAB X IDE project for the appropriate device and hardware debugger.
4. Select *Window > Dashboard*, and then click the **Refresh Debug Tool Status** icon ( ).
5. The part number and the Device and Revision ID values appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various PIC32MX1XX/2XX 28/44-pin XLP family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(1)	
		A1	A3
PIC32MX154F128B	0x07800053	0x1	0x3
PIC32MX174F256B	0x07801053		
PIC32MX254F128B	0x07808053		
PIC32MX274F256B	0x07803053		
PIC32MX154F128D	0x07804053		
PIC32MX174F256D	0x07805053		
PIC32MX254F128D	0x07806053		
PIC32MX274F256D	0x07807053		

Note 1: Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS60001404**E**) for a detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item	Issue Summary	Affected Revisions(1)	
				A1	A3
ADC	IVREF	1.	Reading internal IVREF from the ADC module is not supported.	X	
CLKO	Clock Output	2.	A clock signal is present on the CLKO pin, regardless of the clock source and setting of the CLKO Enable Configuration bit, during a Power-on Reset (POR) condition.	X	X
Configuration Words	Mismatch	3.	Configuration word mismatch logic is non-functional.	X	X
CTMU	Edge-sensitive Trigger	4.	Edge-sensitive trigger is not functioning for generating an Asynchronous pulse.	X	X
CTMU	CTED Input	5.	The EDGEN bit generates a glitch on the CTED input causing a false trigger.	X	X
CTMU	Temperature Sensor	6.	Temperature sensor measurement is not supported for CTMUCON<1:0> = range 2 or 3.	X	X
CTMU	Temperature Sensor	7.	Internal temperature sensor accuracy does not meet the data sheet specification.	X	X
CTMU	Idle	8.	CTMU current source isn't enabled in Idle mode (CTMUSIDL bit = 1), which prevents ADC, if enabled in Idle mode, from being able to measure the CTMU temperature sensor.	X	X
CTMU	Current Sourcing	9.	The CTMU module does not meet the current sourcing range data sheet specifications.	X	X
CTMU	Time Generation	10.	When Time Generation mode is enabled by setting the TGEN bit (CTMUCON<12>), the manual current sourcing set by the EDG1STAT bit (CTMUCON <24>) from the CTMU is non-functional.	X	X
Deep Sleep	—	11.	The user application must not attempt to enter Deep Sleep mode for a period of 50 µs after exiting Reset on start-up or the device will never recover and is no longer able to be erased and/or reprogrammed.	X	
Deep Sleep	DSGPR1 Register	12.	On transition from Deep Sleep mode to VBAT mode, semaphore DSGPR1 register does not retain data.	X	X
Deep Sleep	Configuration Word	13.	If a rare Configuration Word bit mismatch occurs while in Deep Sleep mode, the device will be non-functional until a POR.	X	
Deep Sleep	DSBOR	14.	Inconsistent DSBOR status bit (DSCON<1>) values occur after a Deep Sleep BOR event.	X	X
Deep Sleep	Current Specification	15.	The Deep Sleep Current specification is not met at less than 0ºC operation.	X	X
Deep Sleep	DSWAKE	16.	Upon wake-up from Deep Sleep mode, the DSWAKE register does not always indicate the correct wake-up event source.	X	X
Deep Sleep	DPSLP Status Bit	17.	The DPSLP Deep Sleep Mode status bit, DPSLP (RSCON<10>), is incorrectly set even though Deep Sleep mode was not entered on a drop from VDD nominal to a VPOR reset trip.	X	
FSCM	Interrupts	18.	The Fail-Safe Clock Monitor should be a NMI interrupt instead of a user-selectable IEC0<29> interrupt.	X	
I^{2}C	Idle	19.	The I^{2}C module resets after Idle mode when the SIDL bit (I2CxCON<13>) is set.	X	X
I^{2}C	Start/Restart	20.	When the I^{2}C module is in Slave mode, Start and Restart Interrupt are not functional on all devices.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item	Issue Summary	Affected Revisions(1)	
				A1	A3
I^2C	Start/Stop	21.	The I^2C Start bit, S (I2C1STAT<3>), is not cleared and the Stop bit, P (I2C1STAT<4>), is not set when an external I^2C master creates a Stop condition immediately after a Start condition.	X	X
TDO	Programming	22.	Hardware automatically configures and enables the TDO output pin function, which toggles when any PGECx/PGEDx pair are used during programming.	X	
I/O	Injection Current	23.	Non-5v tolerant I/O pins do not support the high-side injection current parameter specification (DI60b) V_{IN} > V_{DD}.	X	X
Input Capture	Debug	24.	Freeze in Debug is not supported when using ICAP with DMA.	X	X
LVD	Interrupt	25.	An HLVD interrupt is a NMI type instead of a user-selectable IEC0<29> interrupt.	X	
LVD	—	26.	The LVD module is non-functional and the HLVD module trip thresholds do not meet the data sheet specifications.	X	X
SOSC	SOSC Crystals	27.	SOSC crystals with ESR <= 50 kΩ fail to oscillate at -40ºC.	X	X
PMP	Input/Output Buffers	28.	The PMP input buffer full flag, IB0F, and the output buffer underflow, OBUF, are getting set as soon as the PMP module is enabled in Slave mode (PMPTTL bit (PMCON<10>) is equal to '1').	X	X
PMP	Interrupts	29.	No PMP interrupts are generated in EPSP mode when the WAITE<1:)> bits (PMMODE<1:0>) are equal to '0'.	X	X
RCON	Deep Sleep	30.	If the DSEN bit (DSCON<15>) is equal to '1', Deep Sleep Enable is set during a V_{DD} nominal to BOR back to V_{DD} nominal event, the Deep Sleep Status bit, DPSLP (RCON<10>) is set even though Deep Sleep mode was never entered.	X	
RTCC	RTCC	31.	The RTCC module does not function in VBAT mode.	X	X
SPI	TMR1 Register	32.	The Shift Register Empty Status bit, SRMT (SPIxSTAT<7>), may be incorrect when the shift register becomes empty when a transmit becomes empty at the same time.	X	X
Timer1	TMR1 Register	33.	In Asynchronous mode, the TMR1 register remains at the initial set value for 5 external clock pulses after wake-up from Sleep mode.	X	X
Timer1	Counter Mode	34.	In asynchronous external counter mode, Timer1 does not reflect the first count from an external T1CLK input.	X	X
Timer1	Asynchronous Mode	35.	In Asynchronous mode, Timer 1 counts beyond the period value when the period is 0x01.	X	X
Timer1	Gated Mode	36.	Timer1 does not work properly in Gated mode with the prescaler enabled.	X	X
Timer1	TMR1 Register Writes	37.	Back-to-back writes to the TMR1 register are not allowed for four PBCLK cycles.	X	X
Timer1	Asynchronous Timer	38.	The Asynchronous Timer Write Disable bit, TWDIS (TxCON<12>), and the Asynchronous Timer Write in Progress bit, TWIP (TxCON<11>), are non-functional.	X	X
Timer1	Reset	39.	The Timer1 TCK input propagates undefined values if left floating after a Reset.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item	Issue Summary	Affected Revisions(1)	
				A1	A3
Timer2-Timer5	Debug Breakpoint	40.	On a debug breakpoint, TMRx, x=2-5, may not be representative of the correct value.	X	X
Timer2-Timer5	Internal Output Clock	41.	The Timerx internal output clock to various peripherals, such as Output Compare modules, are not gated OFF on an active TxCK input, despite the TGATE bit (TxCON<7>) being disabled (i.e., set to '0').	X	X
Timer2-Timer5	Period Match	42.	Timer TMR event trigger/interrupt on a period match may not occur if it coincides with entry into Sleep mode.	X	X
USB	Interrupts	43.	UIDLE interrupts cease if the UIDLE interrupt flag is cleared.	X	X
USB	Specifications	44.	USB D+/D- Rise/Fall Times do not meet the data sheet specifications with five meter cable greater than +55ºC.	X	X
USB	Low-Speed Operation	45.	When the USB module is configured for Low-Speed operation, (i.e., LSPD bit (U1EPx<7>) = 1), the interrupt timer sets the T1MSECIF interrupt status flag (U1OTGIR<T1MSECIF>) every 8 ms instead of the expected 1 ms.	X	X
USB	Activity Status	46.	If SYSCLK slowed to less than 16 MHz while the USB link is idle, powered-down, or deattached, software may not receive indication of USB activity Resume, SRP, HNP or reattach soon enough to meet the USB protocol. USB interrupts may also not be asserted in time.	X	X
PMP	Slave Mode	47.	PMP in slave when in TTL mode is de-featured.	X	X
IVREF	Comparator	48.	Internal 1.2v IVREF reference is not supported for use with comparator reference.	X	X
CTMU	CTMU	49.	Capacitive measurement and time measurement features are not supported.	X	X
Deep Sleep	IPD	50.	Deep Sleep current exceeds maximum specification from -40ºc to 0ºc.	X	X
UART	High-Speed Mode	51.	The UART Stop bit duration is shorter than expected in High-Speed mode (UxMODE.BRGH =1) for baud rates less than 7.5 MBPS.	X	X
SOSC	SOSCRDY	52.	SOSCRDY may not properly reflect SOSC status when SOSC is disabled.	X	X
USB Low-Speed Mode	Low-Speed Mode	53.	USB Low-Speed Device and Host modes are not supported.	X	X
Flash: RTSP	RTSP	54.	RTSP of Configuration Words is not functional.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A3**).

1. Module: ADC

Converting the Internal IVREF Band Gap, 1.2V, (internal AN14), the voltage source is not supported and will yield indeterminate results.

Work around

None.

Affected Silicon Revisions

A1	A3						
X							

2. Module: CLKO

During any active reset, the OSC2/CLKO/RPA3/RA3 pin defaults temporarily to the CLKO output pin. A clock signal is present on the CLKO pin, regardless of the clock source and setting of the CLKO Enable Configuration bit, while the device is in Reset.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

3. Module: Configuration Words

Configuration Words mismatch logic is non-functional. Conversely, no device Reset as defined by the CMR bit (RCON<9>) would result from a very rare run-time Flash Configuration Word(s) bit change.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

4. Module: CTMU

Edge Sequencing mode, controlled by the EDGSEQUEN bit (CTMUCON<2>), and Edge mode are not functional.

Work around

Use level modes instead.

Affected Silicon Revisions

A1	A3						
X	X						

5. Module: CTMU

When set, the Edge Enable bit, EDGEN (CTMUCON<11>), generates a glitch on the selected CTEDx input, which causes a false trigger.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

6. Module: CTMU

Temperature sensor measurement is not supported for the IRNG<1:0> bits (CTMUCON<1:0>) = '`0b01` and '`0b10`, current range 1 or 2.

Work around 1

Use IRNG<1:0> bit '`0b00` or '`0b11`.

Work around 2

Set the ADC sample rate for the temperature sensor to less than 1 ksps.

Affected Silicon Revisions

A1	A3						
X	X						

7. Module: CTMU

Internal temperature sensor accuracy does not meet ±2ºC specification, instead it is ±6ºC.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

8. Module: CTMU

If the ADC module is enabled in Idle mode, it should override the setting of the CTMUSIDL bit (CTMUCON<13>) = 1, (i.e., discontinue CTMU module operation when the device enters Idle mode), and if the ADC module attempts to make a CTMU temperature sensor measurement. However, it cannot because CTMU current sources aren't enabled in Idle mode.

Work around

Set the CTMUSIDL bit to '0' to continue module operation when the device enters Idle mode.

Affected Silicon Revisions

A1	A3						
X	X						

9. Module: CTMU

The CTMU is greater than the maximum current sourcing range specifications in the data sheet when the IRNG bits in the CTMUCON register are set to '0b00 (715 μA max.) and '0b11 (71.5 μA max.), and when the device ambient temperature is less than +90ºC.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

10. Module: CTMU

When Time Generation mode is enabled by setting the TGEN bit (CTMUCON<12>), the manual current sourcing set by the EDG1STAT bit (CTMUCON <24>) from the CTMU is non-functional.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

11. Module: Deep Sleep

The user application must not attempt to enter Deep Sleep mode for a period of 50 μs after exiting Reset on start-up or the device will never recover and is no longer able to be erased and/or reprogrammed.

Work around

Insure application does not enter deep sleep mode for at least 50 μs after any reset. Institute 50 μs delay using timer or software delay loop.

Affected Silicon Revisions

A1	A3						
X							

12. Module: Deep Sleep

On transition from Deep Sleep mode to VBAT mode, the semaphore DSGPR1 register does not retain its content as expected.

Work around

Enable DSBOR.

Affected Silicon Revisions

A1	A3						
X	X						

13. Module: Deep Sleep

If a rare Configuration Word bit mismatch occurs while in Deep Sleep, the device will be non-functional until a POR.

Work around

None.

Affected Silicon Revisions

A1	A3						
X							

14. Module: Deep Sleep

Inconsistent DSBOR status bit (DSCON<1>) values occur after a Deep Sleep BOR event.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

15. Module: Deep Sleep

Exceeds maximum Deep Sleep current specification at less than +25ºC:

- At 0ºC, 5000 nA instead of 500 nA
- At -40ºC, 7500 nA instead of 150 nA

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

16. Module: Deep Sleep

Upon wake-up from Deep Sleep, the DSWAKE register does not always indicate the correct wake-up event source.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

17. Module: Deep Sleep

When Deep Sleep is enabled, DPSLP bit (RCON<10>) = 1, the DPSLP Deep Sleep Mode status bit (DPSLP) is incorrectly set on exit from VBAT even though Deep Sleep mode was not entered after a BOR/POR reset event.

Work around

None.

Affected Silicon Revisions

A1	A3						
X							

18. Module: FSCM

The Fail-Safe Clock Monitor should be a Non-maskable Interrupt (NMI) instead of a general purpose user-selectable IEC0<29> interrupt.

Work around

None.

Affected Silicon Revisions

A1	A3						
X							

19. Module: I^{2}C

The I^{2}C module and SFRs are reset after entry into Idle mode when the SIDL bit (I2CxCON<13>) is set to '1' and module operation discontinues when the device enters Idle mode.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

20. Module: I^{2}C

When the I^{2}C module is in Slave mode, Start and Restart Interrupts are not occurring or properly reflected in the IFSx flag bits on all devices.

Work around

Use software polling to test the I^{2}C Start/Restart status bit, S (I2CxSTAT<3>).

Affected Silicon Revisions

A1	A3						
X	X						

21. Module: I^{2}C

The I^{2}C Start bit, S (I2C1STAT<3>), is not cleared and the Stop bit, P (I2C1STAT<4>), is not set when an external I^{2}C master creates a Stop condition immediately after a Start condition.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

22. Module: TDO

Hardware automatically configures and enables the TDO output pin function, which toggles when any PGECx/PGEDx pair is used during programming.

Work around

None.

Affected Silicon Revisions

A1	A3						
X							

23. Module: I/O

Non-5v tolerant I/O pins do not support the high-side injection current parameter specification DI60b (i.e., $V_{IN} > V_{DD}$). Even if the injection current is limited to less than 5 mA, a device reset can occur.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

24. Module: Input Capture

Freeze in Debug not supported when using ICAP with DMA.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

25. Module: LVD

A HLVD interrupt is a NMI type instead of a general purpose user selectable IEC0<29> interrupt.

Work around

None

Affected Silicon Revisions

A1	A3						
X							

26. Module: LVD

The LVD module is non-functional the HLVD module trip thresholds do not meet the data sheet specifications.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

27. Module: SOSC

SOSC crystals with ESR less than or equal to 50 kΩ fail to oscillate at -40ºc.

Work around

Select SOSC crystals with an ESR greater than 50 kΩ.

Affected Silicon Revisions

A1	A3						
X	X						

28. Module: PMP

The PMP input buffer full flag, IB0F, and the output buffer underflow flag, OBUF, are set as soon as the PMP module is enabled in Slave mode (PMPTTL bit (PMCON<10>) is equal to '`1`').

Work around

During PMP slave mode initialization and before PMP interrupts are enabled, clear the input buffer full flag (IB0F bit (PMSTAT<8>) and the output buffer underflow flag (OBUF bit (PMSTAT<6>) when clearing any pending IFSx interrupt flags.

Affected Silicon Revisions

A1	A3						
X	X						

29. Module: PMP

No PMP interrupts are generated in Enhanced Parallel Salve Port (EPSP) mode when the WAITE<1:0> bits (PMMODE<1:0>) are equal to ‘0’.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

30. Module: RCON

If the DSEN bit (DSCON<15>) is equal to ‘1’, Deep Sleep Enable is set during a VDD to BOR back to VDD event, the Deep Sleep Status bit, DPSLP (RCON<10>) is set even though Deep Sleep mode was never entered.

Work around

None.

Affected Silicon Revisions

A1	A3						
X							

31. Module: RTCC

The RTCC module does not function in VBAT mode. The RTCC timer does not increment, and therefore, does not keep time.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

32. Module: SPI

The Shift Register Empty status bit, SRMT (SPIxSTAT<7>), may be incorrect when the shift register becomes empty when a transmit becomes empty at the same time.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

33. Module: Timer1

In Asynchronous mode, (i.e., TCS bit (T1CON<1> = 1, TSYNC bit (T1CON<2> = 0, and TECS<1:0> (T1CON<9:8> = ‘0b01), the TMR1 register remains at the initial set value for 5 external clock pulses after wake-up from Sleep mode.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

34. Module: Timer1

In Asynchronous mode, (i.e., TCS bit (T1CON<1> = 1, TSYNC bit (T1CON<2> = 0, and TECS<1:0> (T1CON<9:8> = ‘0b01), Timer1 does not reflect the first count from an external T1CLK input

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

35. Module: Timer1

Timer1 counts beyond the period value in Asynchronous mode when the period is 0x01.

Work around

Set Timer1 period, PR1 to greater than 1.

Affected Silicon Revisions

A1	A3						
X	X						

36. Module: Timer1

Timer1 does not work properly in Gated mode (i.e., TGATE bit (T1CON<7>) = 1, TCS bit (T1CON<1> = 0) with the prescaler enabled (TCKPS<1:0> bits (T1CON<5:4>) = ‘0b00).

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

37. Module: Timer1

Back-to-back CPU writes to the TMR1 register are not allowed for at least four PBCLK cycles.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

38. Module: Timer1

The Asynchronous Timer Write Disable bit, TWDIS (TxCON<12>), and the Asynchronous Timer Write in Progress bit, TWIP (TxCON<11>), are non-functional.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

39. Module: Timer1

The Timer1 external TCK input pin propagates undefined values if left floating after a Reset.

Work around

Place a 10k pull-down resistor on the T1CLK pin.

Affected Silicon Revisions

A1	A3						
X	X						

40. Module: Timer2-Timer5

On a debug breakpoint, TMRx, where ‘x’ = 2-5, may not be representative of the correct count value.

Work around

None

Affected Silicon Revisions

A1	A3						
X	X						

41. Module: Timer2-Timer5

The Timerx internal output clock to various peripherals, such as Output Compare modules, are not gated OFF on an active TxCK input, despite the TGATE bit (TxCON<7>) being disabled (i.e., set to ‘0’). This condition may affect other peripherals that may utilize them.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

42. Module: Timer2-Timer5

A Timer TMR event trigger/interrupt on a period match may not occur if it coincides with entry into Sleep mode.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

43. Module: USB

If the Idle Detect Interrupt Enable bit (IDLEIE bit (U1IE<4>)), is equal to ‘1’ and the bus has been idle for more than 3 ms while the UIDLE interrupt flag is set; if software clears the interrupt flag and the bus remains idle, the UIDLE interrupt flag will not re-trigger a second time even after an additional 3 ms of J-state bus Idle condition.

Work around

Software can leave the UIDLE bit set until it has received some indication of bus resumption like “Resume” or “Reset”. If, any time, the UIDLE bit is set, it would be acceptable to suspend the USB module, as long as this code is protected by USB Sleep Entry Guard (USLPGRD (U1PWRC<4>)) and USB Activity Pending (UACTPND (U1PWRC<7>)). Note that this will require software to clear the UIDLE interrupt enable bit to exit the USB ISR if using interrupt-driven code.

Affected Silicon Revisions

A1	A3						
X	X						

44. Module: USB

USB D+/D- Rise/Fall Times do not meet the specification with a 5 meter cable greater than +55ºC. This will not affect certification as it is performed at +25ºC.

Work around 1

Insure the USB cable is less than 3 meters in length.

Work around 2

Insure ambient device temperature of less than +55ºC.

Affected Silicon Revisions

A1	A3						
X	X						

45. Module: USB

When the USB module is configured for Low-Speed operation, (i.e., LSPD bit (U1EPx<7>) = 1), the interrupt timer sets the T1MSECIF interrupt status flag (U1OTGIR<T1MSECIF>) every 8 ms instead of the expected 1 ms.

Work around

Instead, use a general purpose timer for a period of 1 ms.

Affected Silicon Revisions

A1	A3						
X	X						

46. Module: USB

If SYSCLK is slowed to less than 16 MHz while the USB link is idle, powered-down, or deattached the software may not receive indication of USB activity Resume, SRP, HNP, or reattach soon enough to meet the USB protocol. USB interrupts may also not be asserted in time.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

47. Module: PMP

PMP in Slave mode PMMODE<9:8> = 0b00 or 0b01 (i.e., MODE<1:0>) and PMCON<10>=1, (i.e., PMPTTL). The PMP module uses TTL input buffers then CS de-asserts before RD or WR strobe violating hold time requirements.

Work around

Use in Schmitt Trigger input buffer mode PMCON<10>=0 (i.e., PMPTTL=0).

Affected Silicon Revisions

A1	A3						
X	X						

48. Module: IVREF

Internal 1.2v IVREF reference is not supported for use with comparator reference.

Work around

Use CMxCON<4> (i.e., CREF) instead as the comparator voltage reference source.

Affected Silicon Revisions

A1	A3						
X	X						

49. Module: CTMU

The current sources of the various ranges are not constant as expected, therefore the capacitive and time measurement features of the CTMU are not supported.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

50. Module: Deep Sleep

Exceeds maximum Deep Sleep current specification upon initial entry into Deep Sleep from -40ºc to 0ºc:

Temp	DS <35 sec	DS +45 sec	DS +100 sec	DS >150 sec
-40ºc	500 µA	80 µA	20 µA	3 µA

Temp	DS <32 sec	DS +60 sec	DS +90 sec	DS >130 sec
0ºc	180 µA	45 µA	15 µA	0.5 µA

Note: "DS" stands for Deep Sleep entry.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

51. Module: UART

The UART TX Stop bit duration is shorter than the expected in High-Speed mode (BRGH (UxMODE<3>) = 1) for baud rates less than 7.5 MBPS.

Work around

For baud rates less than 7.5 MBPS, operate the UART in Standard-Speed mode, that is, BRGH (UxMODE<3>) = 0. For baud rates greater than 7.5 MBPS operate the UART in High-Speed mode, that is. BRGH (UxMODE<3>) =1.

Affected Silicon Revisions

A1	A3						
X	X						

52. Module: SOSC

CLKSTAT.SOSCRDY remains a high when the SOSC is Off (OSCCON.SOSCEN = 0). CLKSTAT.SOSCRDY accurately reflects crystal status when SOSC is On (OSCCON.SOSCEN = 1).

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

53. Module: USB Low-Speed Mode

USB Low-Speed mode is not functional in both Device and Host modes due to signal integrity compliance issues.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

54. Module: Flash: RTSP

Real-Time Serial Programming (RTSP) of Configuration Words is not functional.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001404**E**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

There are no new data sheet clarifications to report at this time.

APPENDIX A: REVISION HISTORY

Rev A Document (4/2017)

Initial release of this document for revision A1 silicon, which includes the following silicon issues:

1. ADC, 2. CLKO, 3. Configuration Words, 4. CTMU, 4. CTMU, 5. CTMU, 6. CTMU, 7. CTMU, 8. CTMU, 9. CTMU, 10. CTMU, 11. Deep Sleep, 12. Deep Sleep, 13. Deep Sleep, 14. Deep Sleep, 15. Deep Sleep, 16. Deep Sleep, 17. Deep Sleep, 18. FSCM, 19. I^2C, 20. I^2C, 21. I^2C, 22. TDO, 23. I/O, 24. Input Capture, 25. LVD, 26. LVD, 27. SOSC, 28. PMP, 29. PMP, 30. RCON, 31. RTCC, 32. SPI, 33. Timer1, 34. Timer1, 35. Timer1, 36. Timer1, 37. Timer1, 38. Timer1, 39. Timer1, 40. Timer2-Timer5, 41. Timer2-Timer5, 42. Timer2-Timer5, 43. USB, 44. USB, 45. USB, and 46. USB.

Rev B Document (8/2017)

Data Sheet Clarification 1. 28-Lead QFN-S Package was added.

Added silicon issues: 47 (PMP), 48 (IVREF), 49 (CTMU), 50 (Deep Sleep).

Updated 1.

Rev C Document (9/2018)

Added silicon issue: 51. UART.

Rev D Document (01/2019)

Added Silicon Revision A3.

Added Silicon Issue: 52. SOSC

Rev E Document (04/2020)

Added Silicon Issue 53. USB Low-Speed Mode.

Rev F Document (10/2022)

Added Silicon Issue 54. Flash: RTSP

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