Product/Process Change Notification

N° 2021-106-A

CORRECTION!
Additional data sheet update information added in blue font

Dear customer,

please find attached our Infineon Technologies AG PCN:

Several changes affecting products TLE75x

Important information for your attention:

- Please respond to this PCN by indicating your decision on the approval form, sign it and return to your sales partner before 2022-08-14.
- Infineon aligns with the widely-recognized JEDEC STANDARD "JESD46", which stipulates:
  "Lack of acknowledgement of the PCN within 30 days constitutes acceptance of the change."

  Notwithstanding the aforesaid individual agreements shall prevail.

Your prompt reply will help Infineon to assure a smooth and well-executed transition. If Infineon does not hear from your side by the due date, we will assume your full acceptance to this proposed change and its implementation.

Your attention and response to this matter is greatly appreciated.

On 16 April 2020, Infineon acquired Cypress.
We are now in the process of merging and consolidating our tools and processes for PCN, Information Notes, Errata and Product Discontinuance.
For further details, please visit our website:
https://www.infineon.com/cms/en/about-infineon/company/cypress-acquisition/

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Product/Process Change Notification

N° 2021-106-A

Products affected	Please refer to attached affected product list PCN_2021-106-A_[customer-no].pdf

Detailed change information

Subject:	Several changes affecting products TLE75x
Reason/Motivation:	Support further growth: Conversion to new V93k power tester platform. Our volume growth is triggering further growing tester demand. The existing Teradyne µFlex tester platform was discontinued in 2020. Maintenance and spare parts for Teradyne µFlex are secured. For further growth a move to the next generation power tester is needed. Editorial changes in data sheet to update the package name, marking, foot note and back cover information.

Description	**Old**	**New**
EQUIPMENT: **Change in final test platform**	Teradyne µFlex	Teradyne µFlex AND Advantest V93k
TEST FLOW: **Move of all or part of electrical wafer test and/or final test to a different test site**	**TLE75x-ESx:** Infineon Technologies Asia Pacific Pte. Ltd., Singapore, Singapore AND Infineon Technologies Batam P.T., Batam, Indonesia **TLE75004-EPD:** Infineon Technologies Asia Pacific Pte. Ltd., Singapore, Singapore	**TLE75x-ESx:** Infineon Technologies Asia Pacific Pte. Ltd., Singapore, Singapore AND Infineon Technologies Batam P.T., Batam, Indonesia AND Infineon Technologies (Malaysia) Sdn. Bhd., Melaka, Malaysia **TLE75004-EPD:** Infineon Technologies Asia Pacific Pte. Ltd., Singapore, Singapore AND Infineon Technologies Batam P.T., Batam, Indonesia AND Infineon Technologies (Malaysia) Sdn. Bhd., Melaka, Malaysia
Data sheet update	**TLE75004-EPD only:** Rev. 1.00	**TLE75004-EPD only:** Rev. 1.10

Product/Process Change Notification

N° 2021-106-A

Product identification	No change in marking of samples. Traceability assured via date code. No change in SP ordering number.
Anticipated impact of change	Based on the qualification performed, Infineon does not expect any negative impact on quality, function and reliability. No change in form, fit and function expected. DeQuMa-ID(s): SEM-EQ-03 / SEM-TF-01

Attachments

PCN_2021-106-A_[customer-no].pdf	affected product list
4_cip21106_A	data sheet

Time schedule

Final qualification report	available
First samples available	on request
Intended start of delivery [1]	2023-01-09
Last order date (LOD) [2]	2023-01-09
Last delivery date (LDD) [3]	2023-07-10

[1] Provided date or earlier after customer approval.
[2] Last date where orders for unchanged products will be accepted.
[3] Last date for delivery of unchanged products. Delivery of changed products can be earlier (see Intended start of delivery) and depends on approval.

If you have any questions, please do not hesitate to contact your local sales office.

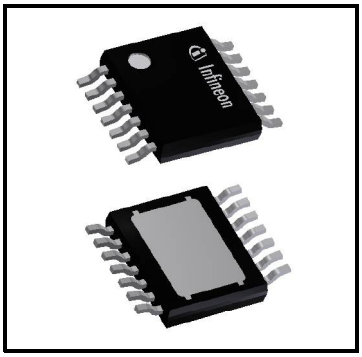
TLE75004-EPD

SPIDER+ 12V

SPI Driver for Enhanced Relay Control

AEC Qualified RoHS

Package	PG-TSDSO-14
Marking	TLE75004



1 Overview

Applications

- Low-side switches for 12 V in automotive or industrial applications such as lighting, heating, motor driving, energy and power distribution
- Especially designed for driving relays, LEDs and motors.

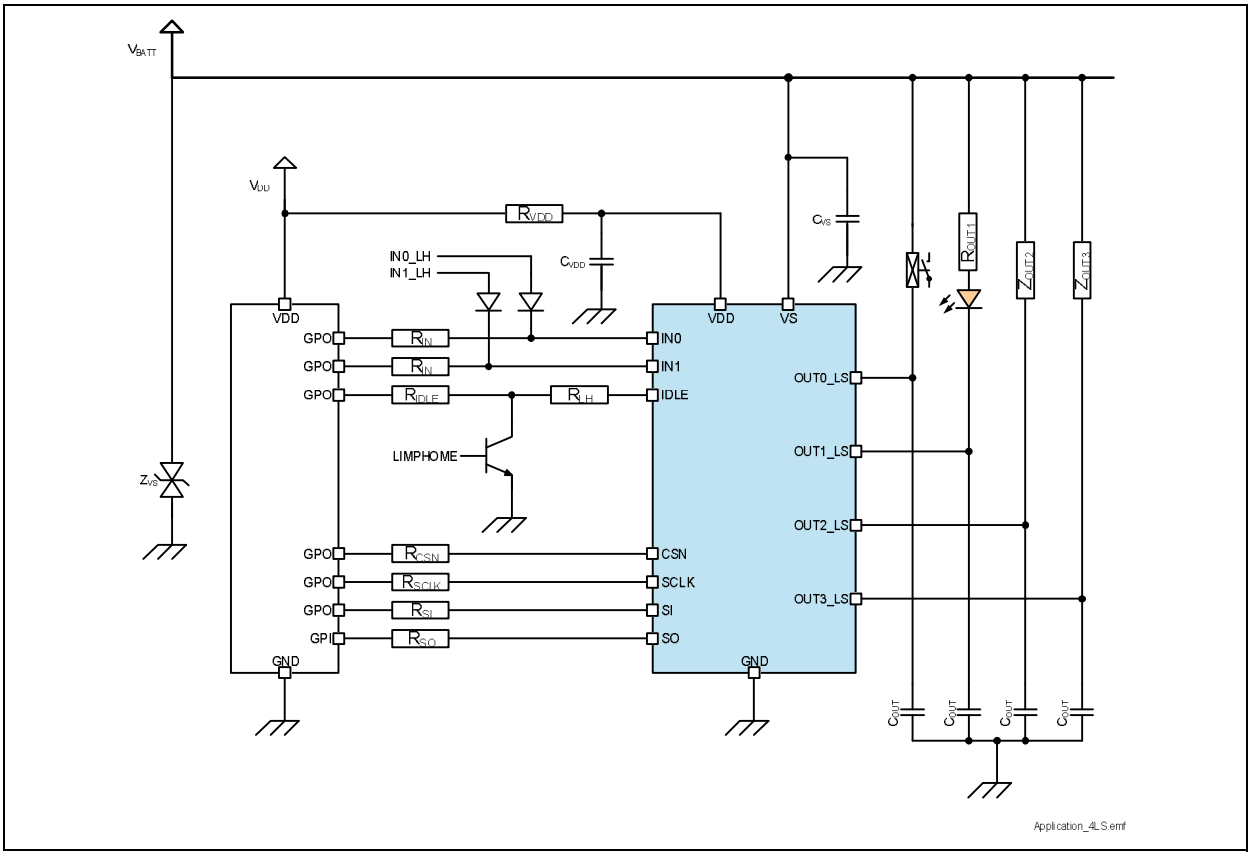


Figure 1 TLE75004-EPD Application Diagram

Overview

Basic Features

- 16-bit serial peripheral interface for control and diagnosis
- Daisy Chain capability SPI also compatible with 8-bit SPI devices
- 2 CMOS compatible parallel input pins with Input Mapping functionality
- Cranking capability down to V_S = 3.0 V (supports LV124)
- Digital supply voltage range compatible with 3.3 V and 5 V microcontrollers
- Very low quiescent current (with usage of IDLE pin)
- Limp Home mode (with usage of IDLE and IN pins)
- Green Product (RoHS compliant)
- AEC Qualified

Protection Features

- Reverse battery protection on V_S without external components
- Short circuit to ground and battery protection
- Stable behavior at under voltage conditions (“Lower Supply Voltage Range for Extended Operation”)
- Over Current latch OFF
- Thermal shutdown latch OFF
- Overvoltage protection
- Loss of ground protection
- Loss of battery protection
- Electrostatic discharge (ESD) protection

Diagnostic Features

- Latched diagnostic information via SPI register
- Over Load detection at ON state
- Open Load detection at OFF state using Output Status Monitor function
- Output Status Monitor
- Input Status Monitor

Application Specific Features

- Fail-safe activation via Input pins in Limp-Home Mode
- SPI with Daisy Chain capability
- Safe operation at low battery voltage (cranking)

Description

The TLE75004-EPD is a four channel low-side power switch in PG-TSDSO-14 package providing embedded protective functions. It is specially designed to control relays and LEDs in automotive and industrial applications.

A serial peripheral interface (SPI) is utilized for control and diagnosis of the loads as well as of the device. For direct control and PWM there are two input pins available connected to two outputs by default. Additional or different outputs can be controlled by the same input pins (programmable via SPI).

Table 1 Product Summary

Parameter	Symbol	Values
Analog supply voltage	V_S	3.0 V … 28 V
Digital supply voltage	V_{DD}	3.0 V … 5.5 V
Minimum overvoltage protection	$V_{S(AZ)}$	42 V (see **Chapter 8.5** for details)
Maximum on-state resistance at T_J = 150 °C	$R_{DS(ON)}$	2.2 Ω
Nominal load current (T_A = 85 °C, all channels)	$I_{L(NOM)}$	470 mA
Maximum Energy dissipation - repetitive	E_{AR}	10 mJ @ $I_{L(EAR)}$ = 220 mA
Minimum Drain to Source clamping voltage	$V_{DS(CL)}$	42 V
Maximum overload switch OFF threshold	$I_{L(OVL0)}$	2.3 A
Maximum total quiescent current at $T_J \leq 85$ °C	I_{SLEEP}	5 µA
Maximum SPI clock frequency	f_{SCLK}	5 MHz

Detailed Description

The TLE75004-EPD is a four channel low-side switch providing embedded protective functions. The output stages incorporate four low-side switches (typical $R_{DS(ON)}$ at T_J = 25°C is 1 Ω).

The 16-bit serial peripheral interface (SPI) is utilized to control and diagnose the device and the loads. The SPI interface provides daisy chain capability in order to assemble multiple devices (also devices with 8 bit SPI) in one SPI chain by using the same number of microcontroller pins.

This device is designed for low supply voltage operation, therefore being able to keep its state at low battery voltage ($V_S \geq 3.0$ V). The SPI functionality, including the possibility to program the device, is available only when the digital power supply is present (see **Chapter 6** for more details).

The TLE75004-EPD is equipped with two input pins that are connected to two outputs, making them controllable even when the digital supply voltage is not available. With the Input Mapping functionality it is possible to connect the input pins to different outputs, or assign more outputs to the same input pin. In this case more channels can be controlled with one signal applied to one input pin.

In Limp Home mode (Fail-Safe mode) the input pins are directly routed to channels 2 and 3. When IDLE pin is “low”, it is possible to activate the two channels using the input pins independently from the presence of the digital supply voltage.

The device provides diagnosis of the load via Open Load at OFF state (with **DIAG_OSM.OUTn** bits) and short circuit detection. For Open Load at OFF state detection, a internal current source I_{OL} can be activated via SPI.

Each output stage is protected against short circuit. In case of Overload, the affected channel switches OFF when the Overload Detection Current $I_{L(OVLn)}$ is reached and can be reactivated via SPI. In Limp Home mode operation, the channels connected to an input pin set to “high” restart automatically after Output Restart time $t_{RETRY(LH)}$ is elapsed. Temperature sensors are available for each channel to protect the device against Over Temperature.

The power transistors are built by N-channel power MOSFET . The inputs are ground referenced TTL compatible. The device is monolithically integrated in Smart Power Technology.

2 Block Diagram and Terms

2.1 Block Diagram

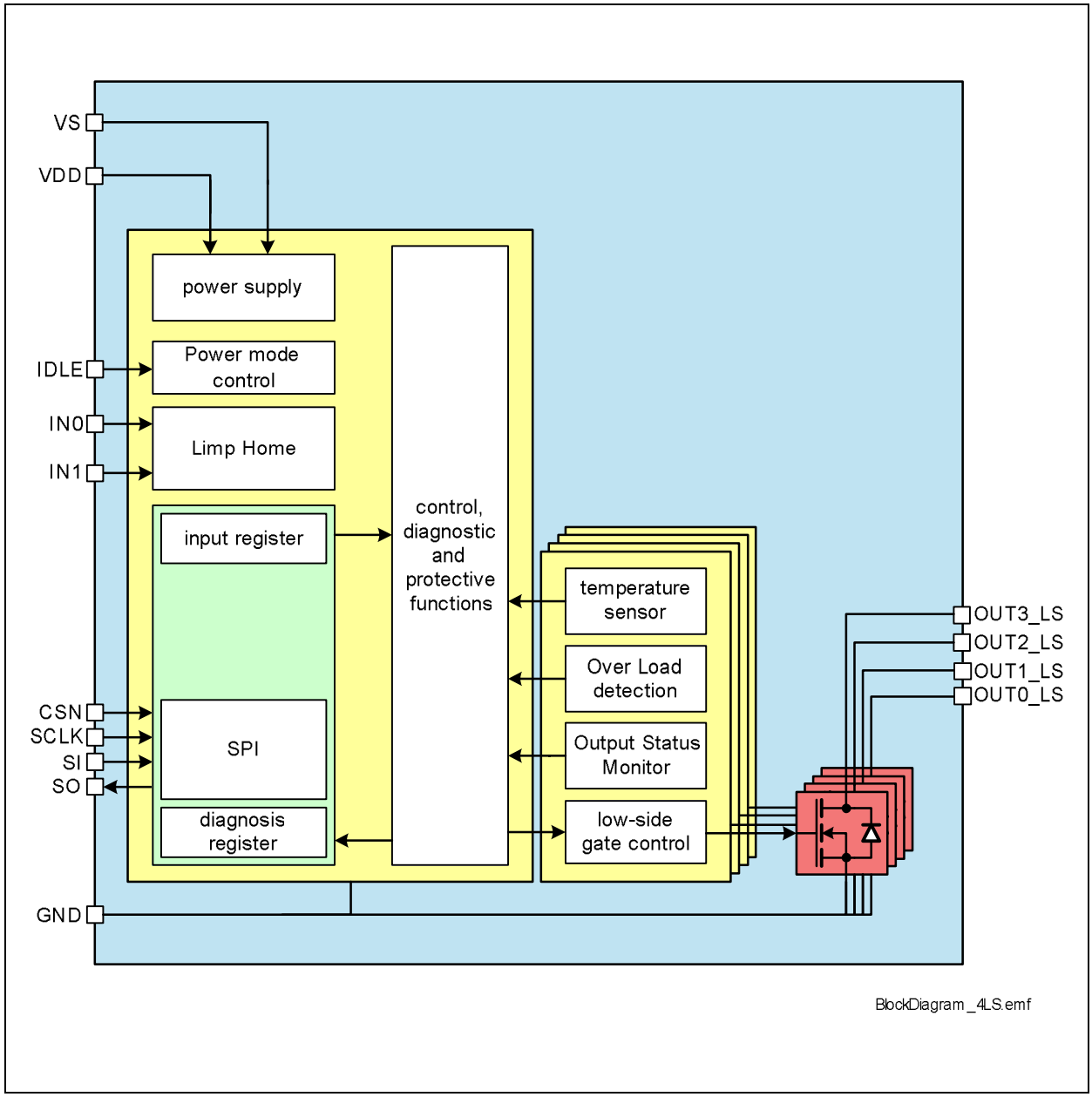


Figure 2 Block Diagram of TLE75004-EPD

2.2 Terms

Figure 3 shows all terms used in this data sheet, with associated convention for positive values.

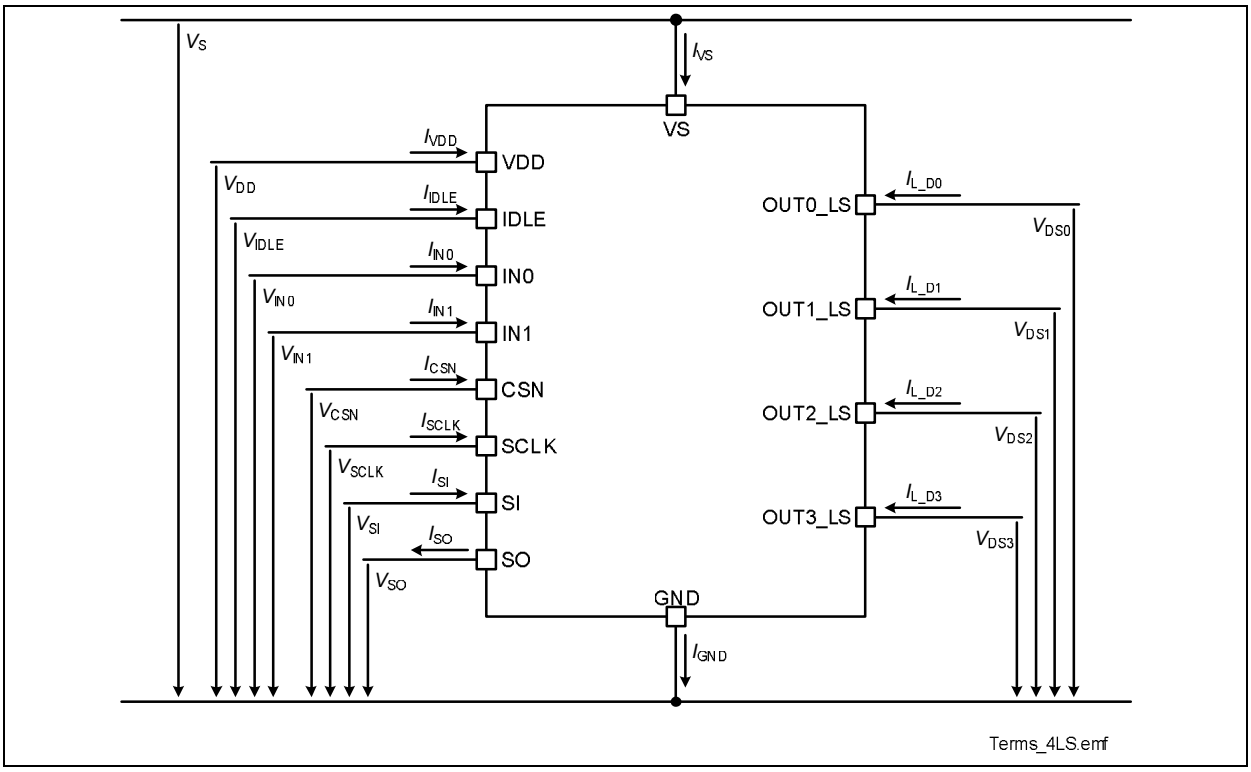


Figure 3 Voltage and Current definition

In all tables of electrical characteristics the channel related symbols without channel numbers are valid for each channel separately (e.g. V_{DS} specification is valid for V_{DS0} ... V_{DS3}).

Furthermore, parameters relative to output current can be indicated without specifying whether the current is going into the Drain pin or going out of the Source pin, unless otherwise specified. For instance, nominal output current can be indicated in the following ways: $I_{L(NOM)}$ $I_{L\_LS(NOM)}$ $I_{L\_D(NOM)}$

All SPI registers bits are marked as follows: `ADDR.PARAMETER` (e.g. `HWCR.RST`) with the exception of the bits in the Diagnosis frames which are marked only with `PARAMETER` (e.g. `UVRVS`).

3 Pin Configuration

3.1 Pin Assignment

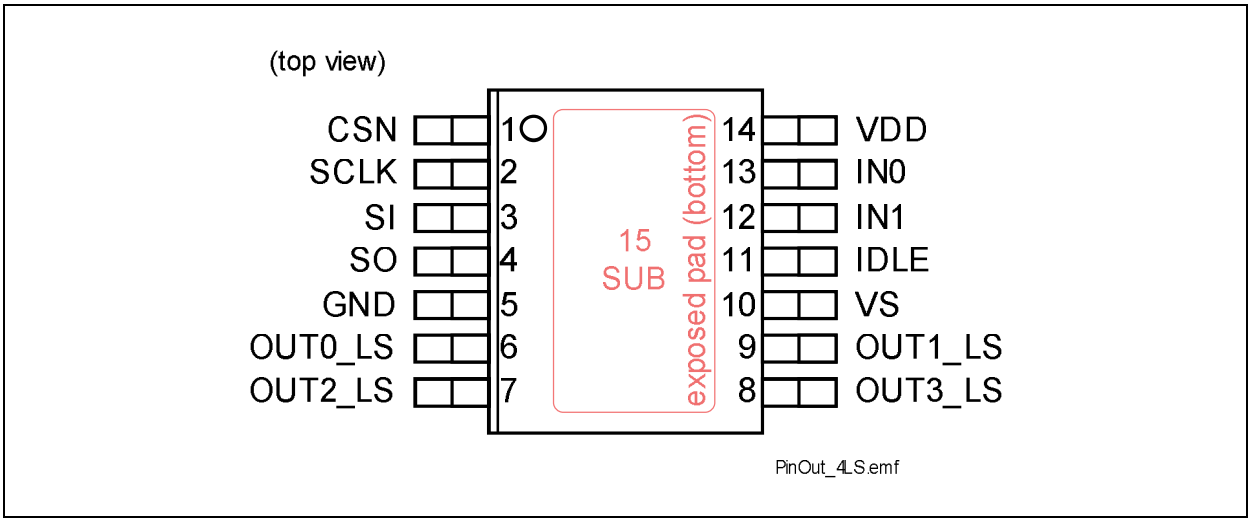


Figure 4 Pin Configuration TLE75004-EPD in PG-TSDSO-14

3.2 Pin Definitions and Functions

Pin	Symbol	I/O	Function
Power Supply Pins			
10	VS	–	**Analog supply V_S** Positive supply voltage for power switches gate control (incl. protections)
14	VDD	–	**Digital supply V_{DD}** Supply voltage for SPI with support function to V_S
5	GND	–	**Ground** Ground connection
SPI Pins			
1	CSN	I	**Chip Select** “low” active, integrated pull-up to V_{DD}
2	SCLK	I	**Serial Clock** “high” active, integrated pull-down to ground
3	SI	I	**Serial Input** “high” active, integrated pull-down to ground
4	SO	O	**Serial Output** “Z” (tri-state) when CSN is “high”
Input and Stand-by Pins			
11	IDLE	I	**Idle mode** power mode control, “high” active, integrated pull-down to ground
13	IN0	I	**Input pin 0** connected to channel 2 by default and in Limp Home mode, “high” active, integrated pull-down to ground
12	IN1	I	**Input pin 1** connected to channel 3 by default and Limp Home mode, “high” active, integrated pull-down to ground
Power Ouput Pins			
6	OUT0_LS	O	Drain of low-side power transistor (channel 0)
7	OUT2_LS	O	Drain of low-side power transistor (channel 2)
8	OUT3_LS	O	Drain of low-side power transistor (channel 3)
9	OUT1_LS	O	Drain of low-side power transistor (channel 1)
Cooling Tab			
15	GND	–	**Exposed pad** It is recommended to connect it to PCB ground for cooling and EMC - not usable as electrical GND pin. Electrical ground must be provided by pin 5.

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings [1)]

T_J = -40 °C to +150 °C
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltages							
Analog Supply voltage	V_S	-0.3	–	28	V	–	P_4.1.1
Digital Supply voltage	V_{DD}	-0.3	–	5.5	V	–	P_4.1.2
Supply voltage for load dump protection	$V_{S(LD)}$	–	–	42	V	[2)]	P_4.1.3
Supply voltage for short circuit protection (single pulse)	$V_{S(SC)}$	0	–	28	V	–	P_4.1.4
Reverse polarity voltage	$-V_{S(REV)}$	–	–	16	V	[3)] $T_{J(0)}$ = 25 °C $t \leq 2$ min See **Chapter 11** for general setup. R_L = 70 Ω on all channels	P_4.1.5
Current through VS pin	I_{VS}	-10	–	10	mA	$t \leq 2$ min	P_4.1.7
Current through VDD pin	I_{VDD}	-50	–	10	mA	$t \leq 2$ min	P_4.1.8
Power Stages							
Load current	$\|I_L\|$	–	–	$I_{L(OVL0)}$	A	single channel	P_4.1.9
Voltage at power transistor	V_{DS}	-0.3	–	42	V	–	P_4.1.10
Maximum energy dissipation single pulse	E_{AS}	–	–	50	mJ	[4)] $T_{J(0)}$ = 25 °C $I_{L(0)} = 2 * I_{L(EAR)}$	P_4.1.13
Maximum energy dissipation single pulse	E_{AS}	–	–	25	mJ	[4)] $T_{J(0)}$ = 150 °C $I_{L(0)}$ = 400 mA	P_4.1.14
Maximum energy dissipation repetitive pulses - $I_{L(EAR)}$	E_{AR}	–	–	10	mJ	[4)] $T_{J(0)}$ = 85 °C $I_{L(0)} = I_{L(EAR)}$ $2*10^6$ cycles	P_4.1.16
IDLE pin							
Voltage at IDLE pin	V_{IDLE}	-0.3		5.5	V	–	P_4.1.23
Current through IDLE pin	I_{IDLE}	-0.75		0.75	mA	–	P_4.1.25

Table 2 Absolute Maximum Ratings (cont'd)[1)]

T_J = -40 °C to +150 °C
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current through IDLE pin	I_{IDLE}	-10.0		2.0	mA	$t \leq 2$ min.	P_4.1.26
Input Pins							
Voltage at input pins	V_{IN}	-0.3		5.5	V	–	P_4.1.28
Current through input pins	I_{IN}	-0.75		0.75	mA	–	P_4.1.30
Current through input pins	I_{IN}	-10.0		2.0	mA	$t \leq 2$ min.	P_4.1.31
SPI Pins							
Voltage at chip select pin	V_{CSN}	-0.3		5.5	V	–	P_4.1.33
Current through chip select pin	I_{CSN}	-0.75		0.75	mA	–	P_4.1.34
Current through chip select pin	I_{CSN}	-10.0		2.0	mA	$t \leq 2$ min.	P_4.1.35
Voltage at serial clock pin	V_{SCLK}	-0.3		5.5	V		P_4.1.37
Current through serial clock pin	I_{SCLK}	-0.75		0.75	mA	–	P_4.1.38
Current through serial clock pin	I_{SCLK}	-10.0		2.0	mA	$t \leq 2$ min.	P_4.1.39
Voltage at serial input pin	V_{SI}	-0.3		5.5	V		P_4.1.41
Current through serial input pin	I_{SI}	-0.75		0.75	mA	–	P_4.1.42
Current through serial input pin	I_{SI}	-10.0		2.0	mA	$t \leq 2$ min.	P_4.1.43
Voltage at serial output pin SO	V_{SO}	-0.3		V_{DD}+0.3	V		P_4.1.58
Current through serial output pin SO	I_{SO}	-0.75		0.75	mA		P_4.1.45
Current through serial output pin SO	I_{SO}	-2.0		10.0	mA	$t \leq 2$ min.	P_4.1.46
Temperatures							
Junction Temperature	T_J	-40	–	150	°C	–	P_4.1.48
Storage Temperature	T_{stg}	-55	–	150	°C	–	P_4.1.49
ESD Susceptibility							
ESD Susceptibility HBM OUT pins vs. V_S or GND	V_{ESD}	-4	–	4	kV	[5)] HBM	P_4.1.50
ESD Susceptibility HBM other pins	V_{ESD}	-2	–	2	kV	[5)] HBM	P_4.1.51
ESD Susceptibility CDM Pin 1, 7, 8, 14 (corner pins)	V_{ESD}	-750	–	750	V	[6)] CDM	P_4.1.53
ESD Susceptibility CDM	V_{ESD}	-500	–	500	V	[6)] CDM	P_4.1.54

1) Not subject to production test, specified by design.
2) For a duration of t_{on} = 400 ms; t_{on}/t_{off} = 10%; limited to 100 pulses
3) Device is mounted on a FR4 2s2p board according to Jedec JESD51-2,-5,-7 at natural convection; the Product (Chip+Package) was simulated on a 76.2 *114.3 *1.5 mm board with 2 inner copper layers (2 * 70 µm Cu, 2 * 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

4) Pulse shape represents inductive switch off: $I_L(t) = I_L(0)$ x (1 - t / t_{pulse}); 0 < t < t_{pulse}
5) ESD susceptibility, Human Body Model “HBM” according to AEC Q100-002
6) ESD susceptibility, Charged Device Mode “CDM” according to AECQ100-011 Rev D

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional Range

Table 3 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltage Range for Normal Operation	$V_{S(NOR)}$	7	–	18	V	–	P_4.2.1
Upper Supply Voltage Range for Extended Operation	$V_{S(EXT,UP)}$	18	–	28	V	Parameter deviation possible	P_4.2.2
Lower Supply Voltage Range for Extended Operation	$V_{S(EXT,LOW)}$	3	–	7	V	Parameter deviation possible	P_4.2.3
Junction Temperature	T_J	-40	–	150	°C	–	P_4.2.4
Logic supply voltage	V_{DD}	3	–	5.5	V	–	P_4.2.5

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 4 Thermal Resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Soldering Point	R_{thJSP}	–	5	7	K/W	1) measured to exposed pad (pin 15)	P_4.3.2
Junction to Ambient	R_{thJA}	–	40	–	K/W	2)	P_4.3.6

1) not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the Product (Chip+Package) was simulated on a 76.2 * 114.3 * 1.5 mm board with 2 inner copper layers (2 * 70 µm Cu, 2 * 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

4.3.1 PCB set up

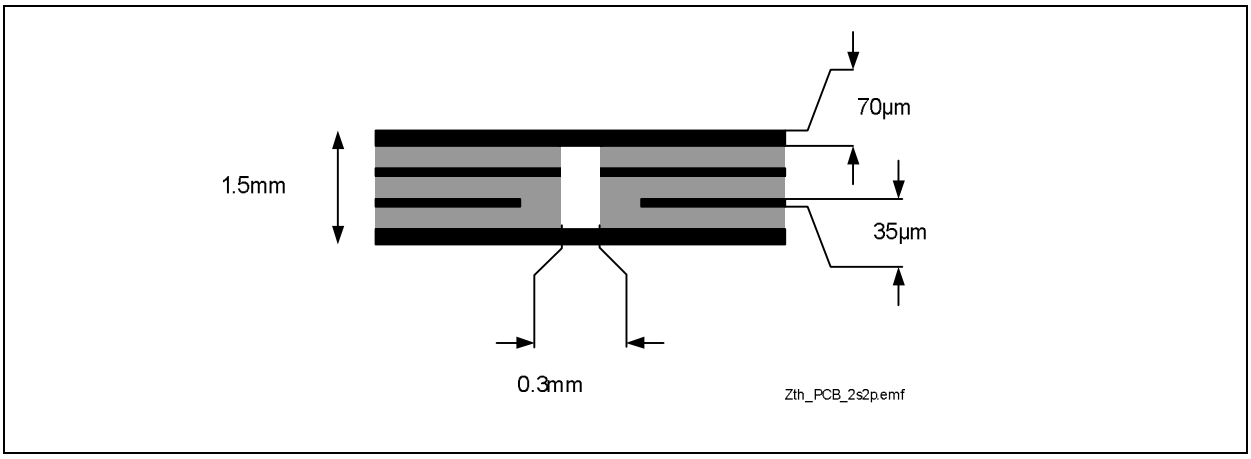


Figure 5 2s2p PCB Cross Section

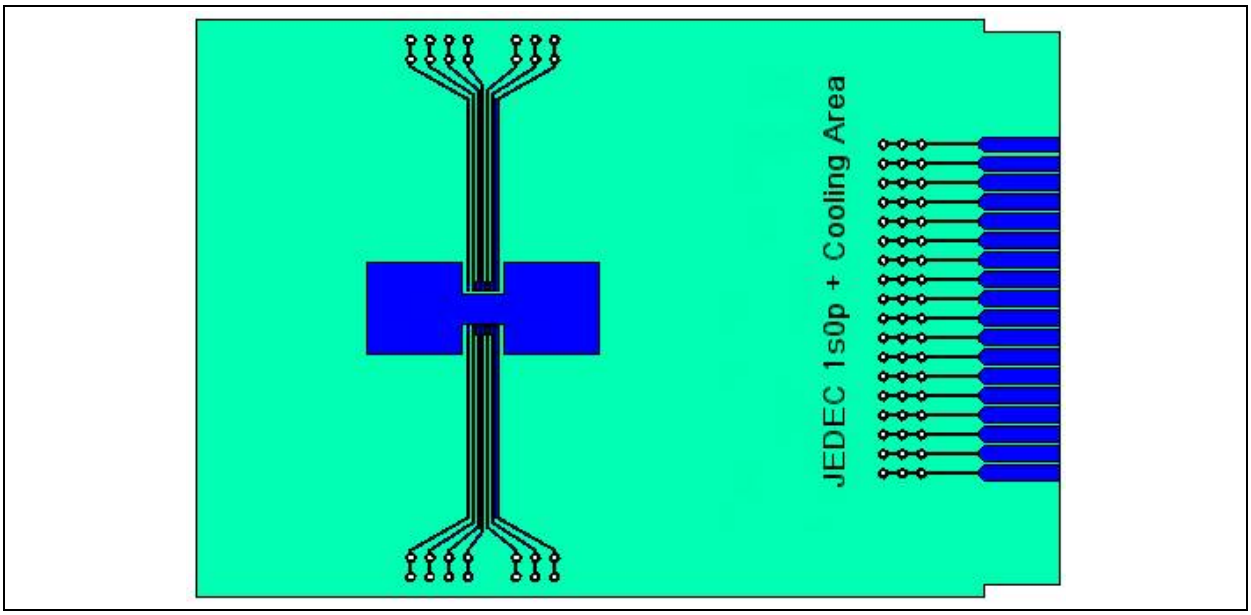


Figure 6 PC Board for Thermal Simulation with 600 mm² Cooling Area

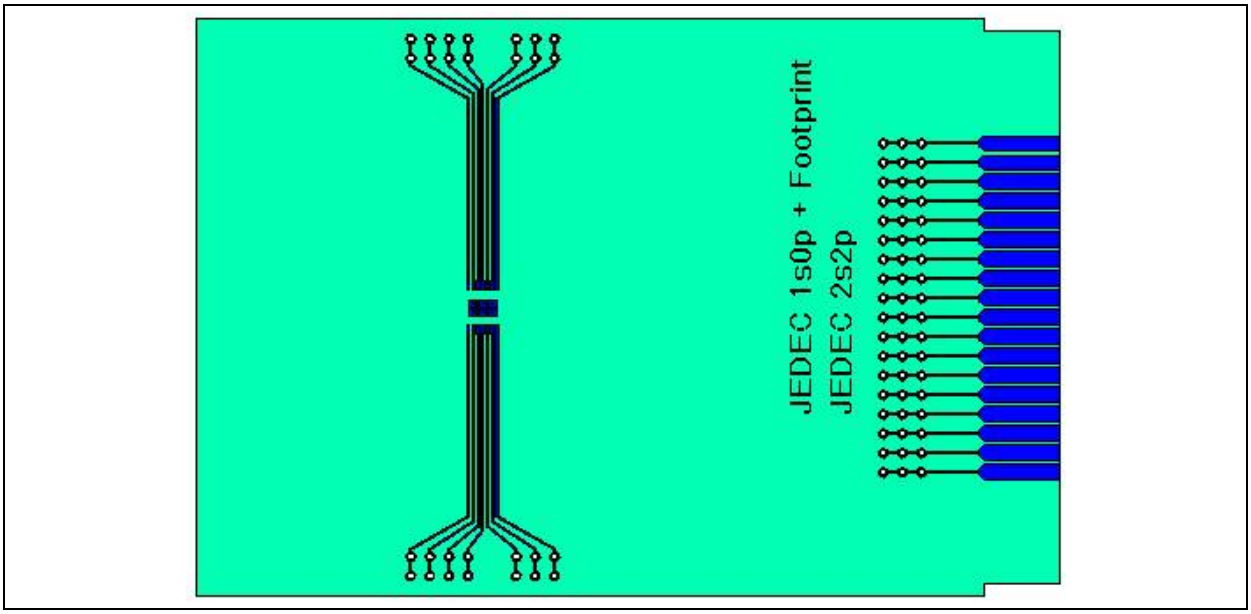


Figure 7 PC Board for Thermal Simulation with 2s2p Cooling Area

4.3.2 Thermal Impedance

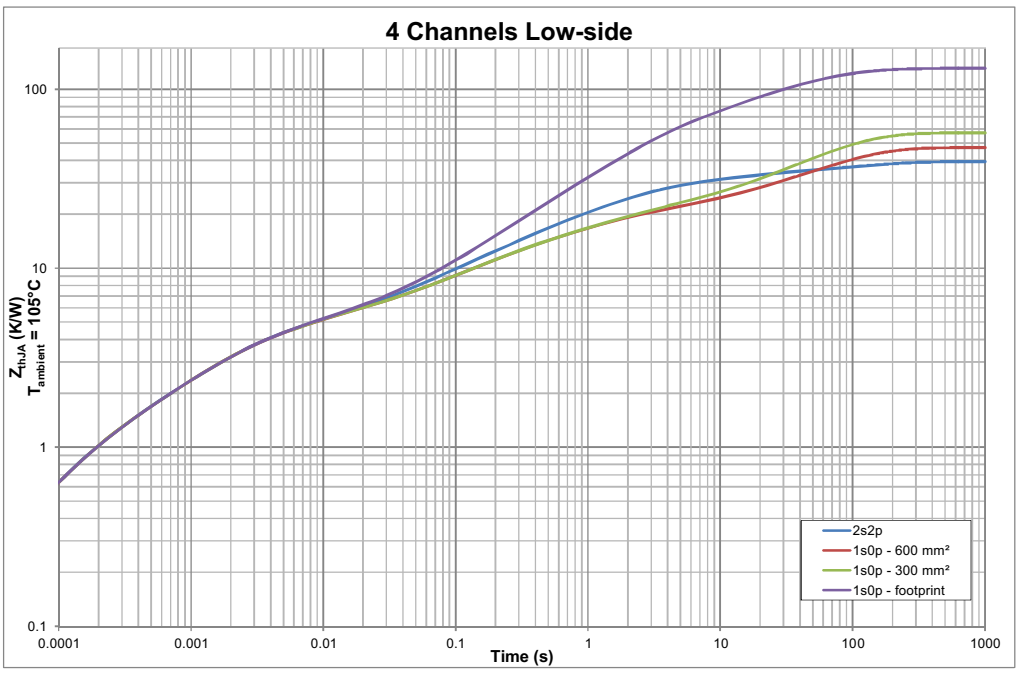


Figure 8 Typical Thermal Impedance. PCB setup according Chapter 4.3.1

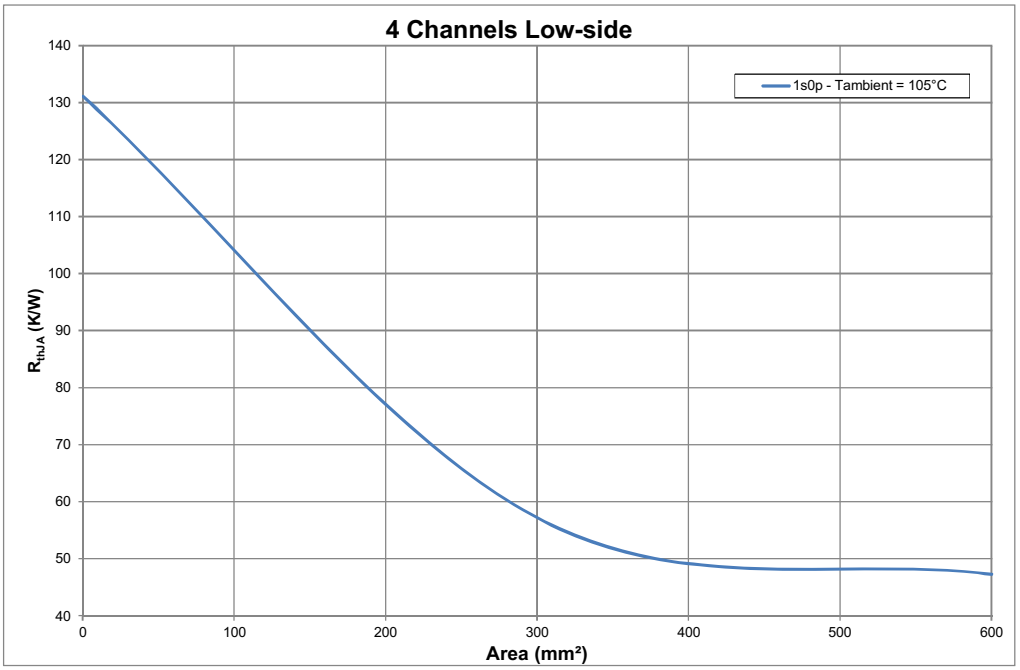


Figure 9 Typical Thermal Resistance. PCB setup 1s0p

5 Control Pins

The device has three pins (IN0, IN1 and IDLE) to control directly the device without using SPI.

5.1 Input pins

TLE75004-EPD has two input pins available. Each input pin is connected by default to one channel (IN0 to channel 2, IN1 to channel 3). Input Mapping Registers **MAPIN0** and **MAPIN1** can be programmed to connect additional or different channels to each input pin, as shown in **Figure 10**. The signals driving the channels are an OR combination between **OUT** register status, IN0 and IN1 (according to Input Mapping registers status).

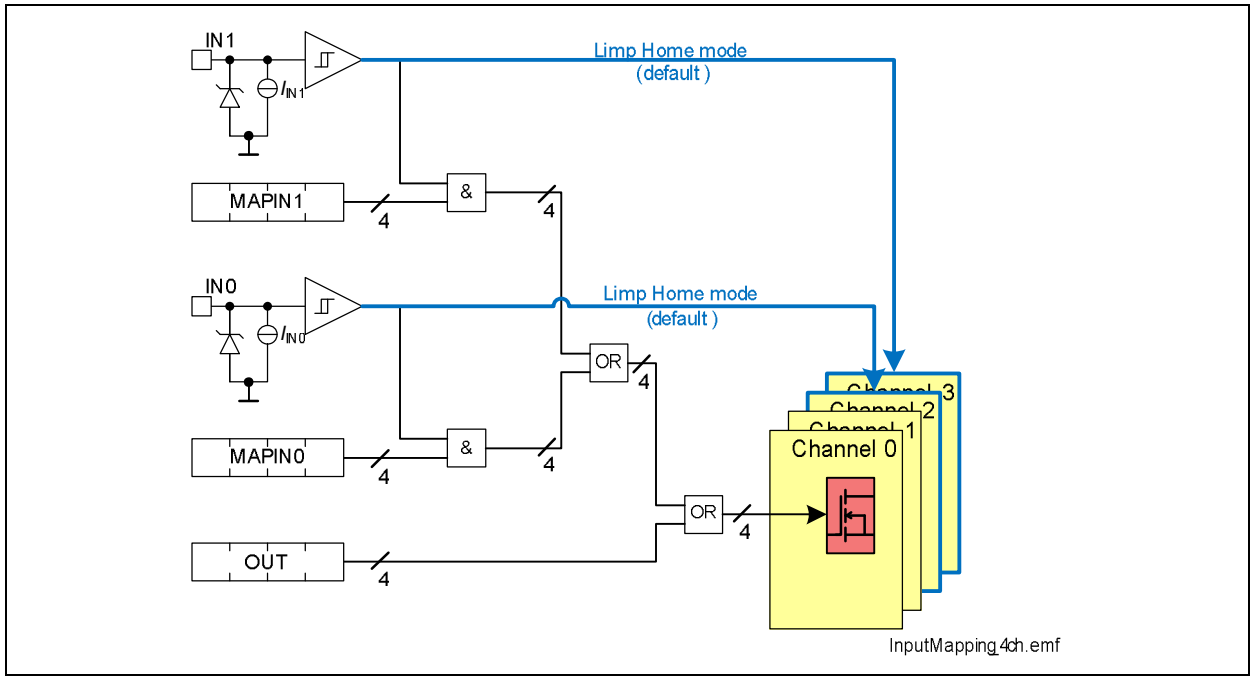


Figure 10 Input Mapping

The logic level of the input pins can be monitored via the Input Status Monitor Register (**INST**). The Input Status Monitor is operative also when TLE75004-EPD is in Limp Home mode. If one of the Input pins is set to “high” and the IDLE pin is set to “low”, the device switches into Limp Home mode and activates the channel mapped by default to the input pins. See **Chapter 6.1.5** for further details.

5.2 IDLE pin

The IDLE pin is used to bring the device into Sleep mode operation when is set to “low” and all input pins are set to “low”.When IDLE pin is set to “low” while one of the input pins is set to “high” the device enters Limp Home mode.

To ensure a proper mode transition, IDLE pin must be set for at least $t_{IDLE2SLEEP}$ (P_6.3.54, transition from “high” to “low”) or $t_{SLEEP2IDLE}$ (P_6.3.53, transition from “low” to “high”).

Setting the IDLE pin to “low” has the following consequences:

- All registers in the SPI are reset to default values
- V_{DD} and V_S Undervoltage detection circuits are disabled to decrease current consumption (if both inputs are set to “low”)

Control Pins

- No SPI communication is allowed (SO pin remains in high impedance state also when CSN pin is set to “low”) if both input pins are set to “low”

5.3 Electrical Characteristics Control Pins

Table 5 Electrical Characteristics: Control Pins

V_{DD} = 3 V to 5.5 V, V_S = 7 V to 18 V, T_J = -40 °C to +150 °C (unless otherwise specified)
Typical values: V_{DD} = 5 V, V_S = 13.5 V, T_J = 25 °C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
IDLE pin							
L-input level	$V_{IDLE(L)}$	0		0.8	V	–	P_5.3.1
H-input level	$V_{IDLE(H)}$	2.0		5.5	V	–	P_5.3.2
L-input current	$I_{IDLE(L)}$	5	12	20	µA	V_{IDLE} = 0.8 V	P_5.3.3
H-input current	$I_{IDLE(H)}$	14	28	45	µA	V_{IDLE} = 2.0 V	P_5.3.4
Input Pins							
L-input level	$V_{IN(L)}$	0		0.8	V	–	P_5.3.5
H-input level	$V_{IN(H)}$	2.0		5.5	V	–	P_5.3.6
L-input current	$I_{IN(L)}$	5	12	20	µA	V_{IN} = 0.8 V	P_5.3.7
H-input current	$I_{IN(H)}$	14	28	45	µA	V_{IN} = 2.0 V	P_5.3.8

6 Power Supply

The TLE75004-EPD is supplied by two supply voltages:

- V_S (analog supply voltage used also for the logic)
- V_{DD} (digital supply voltage)

The V_S supply line is connected to a battery feed and used, in combination with V_{DD} supply, for the driving circuitry of the power stages. In situations where V_S voltage drops below V_{DD} voltage (for instance during cranking events down to 3.0 V), an increased current consumption may be observed at VDD pin.

V_S and V_{DD} supply voltages have an undervoltage detection circuit, which prevents the activation of the associated function in case the measured voltage is below the undervoltage threshold. More in detail:

- An undervoltage on both V_S and V_{DD} supply voltages prevents the activation of the power stages and any SPI communication (the SPI registers are reset)
- An undervoltage on V_{DD} supply prevents any SPI communication. SPI read/write registers are reset to default values.
- An undervoltage on V_S supply forces the TLE75004-EPD to drain all needed current for the low-side switches and for the logic from V_{DD} supply.

Figure 11 shows a basic concept drawing of the interaction between supply pins VS and VDD, the output stage drivers and SO supply line.

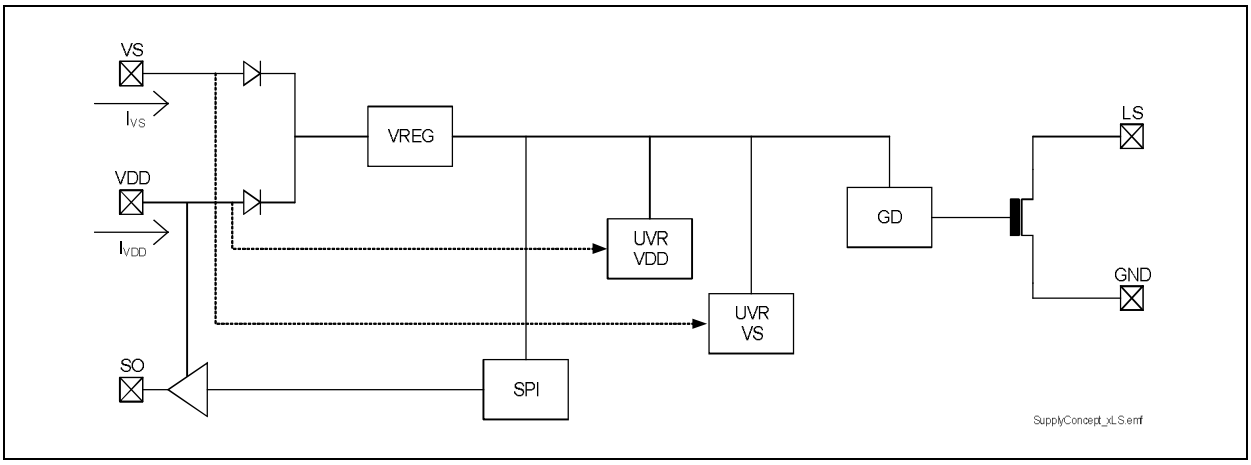


Figure 11 TLE75004-EPD Internal Power Supply concept

When 3.0 V ≤ V_S ≤ V_{DD} - V_{SDIFF} TLE75004-EPD operates in “Cranking Operative Range” (COR). In this condition the current consumption from VDD pin increases while it decreases from VS pin where the total current consumption remains within the specified limits. **Figure 12** shows the voltage levels at VS pin where the device goes in and out of COR. During the transition to and from COR operative region, I_{VS} and I_{VDD} change between values defined for normal operation and for COR operation. The sum of both current remains within limits specified in “Overall current consumption” section (see **Table 8**).

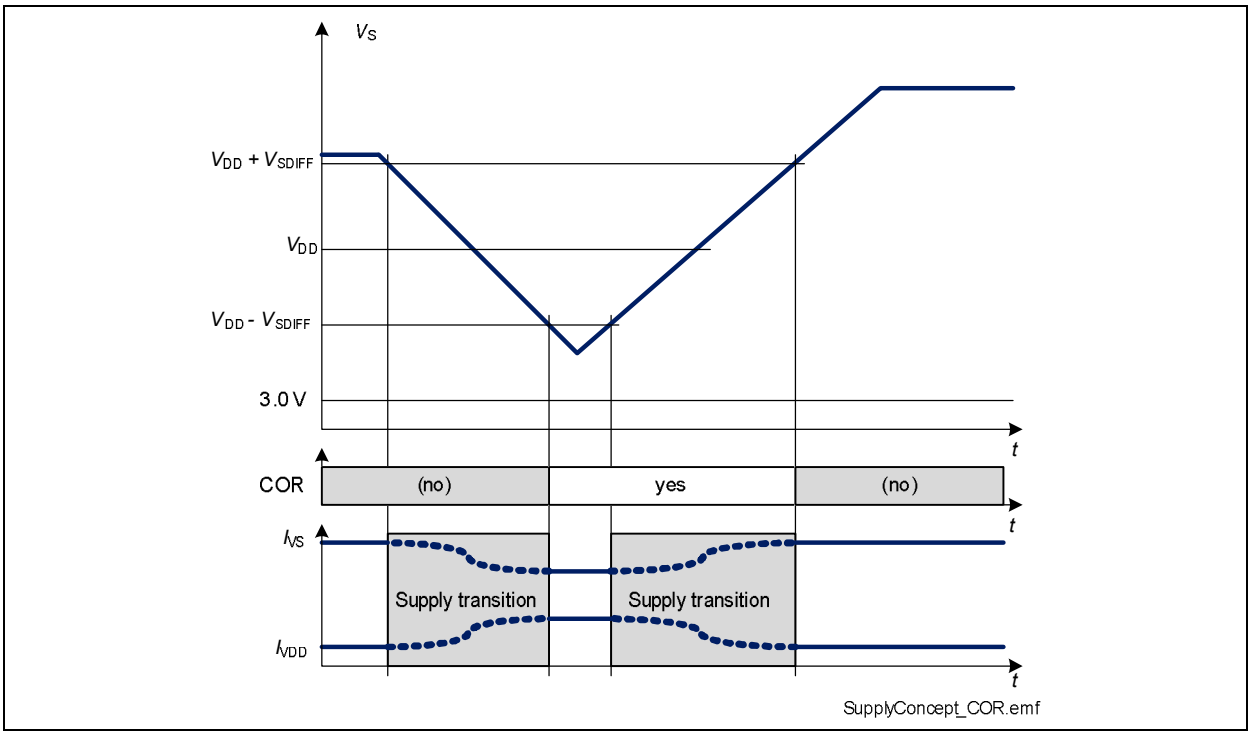


Figure 12 “Cranking Operative Range”

Furthermore, when $V_{S(UV)} \leq V_S \leq V_{S(OP)}$ it may be not possible to switch ON a channel that was previously OFF. All channels that are already ON keep their state unless they are switched OFF via SPI or via INn pins. An overview of channel behavior according to different V_S and V_{DD} supply voltages is shown in **Table 6** (the table is valid after a successful power-up, see **Chapter 6.1.1** for more details).

Table 6 Device capability as function of V_S and V_{DD}

	$V_{DD} \le V_{DD(UV)}$ ($V_{DD(UV)}$ = P_6.3.25)	$V_{DD} = V_{DD(LOP)}$ ($V_{DD(LOP)}$ = P_6.3.24)	$V_{DD} > V_{DD(LOP)}$
$V_S \le 3.0$ V 3.0 V = $V_{S(UV),max}$ (P_6.3.1)	channels cannot be controlled	channels can be switched ON and OFF (SPI control) ($R_{DS(ON)}$ deviations possible)	channels can be switched ON and OFF (SPI control) ($R_{DS(ON)}$ deviations possible)
	SPI registers reset	SPI registers available	SPI registers available
	SPI communication not available (f_{SCLK} = 0 MHz)	SPI communication possible (f_{SCLK} = 1 MHz) (P_10.4.34)	SPI communication possible (f_{SCLK} = 5 MHz) (P_10.4.22)
	Limp Home mode not available	Limp Home mode available ($R_{DS(ON)}$ deviations possible)	Limp Home mode available ($R_{DS(ON)}$ deviations possible)
3.0 V < $V_S \le V_{S(OP)}$ ($V_{S(OP)}$ = P_6.3.2)	channels cannot be controlled by SPI	channels can be switched ON and OFF (SPI control)[1] ($R_{DS(ON)}$ deviations possible)	channels can be switched ON and OFF (SPI control)[1] ($R_{DS(ON)}$ deviations possible)
	SPI registers reset	SPI registers available	SPI registers available
	SPI communication not available (f_{SCLK} = 0 MHz)	SPI communication possible (f_{SCLK} = 1 MHz) (P_10.4.34)	SPI communication possible (f_{SCLK} = 5 MHz) (P_10.4.22)
	Limp Home mode available[1] ($R_{DS(ON)}$ deviations possible)	Limp Home mode available[1] ($R_{DS(ON)}$ deviations possible)	Limp Home mode available ($R_{DS(ON)}$ deviations possible)
$V_S > V_{S(OP)}$	channels cannot be controlled by SPI	channels can be switched ON and OFF (small $R_{DS(ON)}$ dev. possible when $V_S = V_{S(EXT,LOW)}$)	channels can be switched ON and OFF (small $R_{DS(ON)}$ dev. possible when $V_S = V_{S(EXT,LOW)}$)
	SPI registers reset	SPI registers available	SPI registers available
	SPI communication not available (f_{SCLK} = 0 MHz)	SPI communication possible (f_{SCLK} = 5 MHz) (P_10.4.22)	SPI communication possible (f_{SCLK} = 5 MHz) (P_10.4.22)
	Limp Home mode available ($R_{DS(ON)}$ dev. possible when $V_S = V_{S(EXT,LOW)}$)	Limp Home mode available ($R_{DS(ON)}$ dev. possible when $V_S = V_{S(EXT,LOW)}$)	Limp Home mode available ($R_{DS(ON)}$ dev. possible when $V_S = V_{S(EXT,LOW)}$)

1) undervoltage condition on V_S must be considered - see **Chapter 6.2.1** for more details

6.1 Operation Modes

TLE75004-EPD has the following operation modes:

- Sleep mode
- Idle mode
- Active mode
- Limp Home mode

The transition between operation modes is determined according to following levels and states:

- logic level at IDLE pin
- logic level at INn pins
- **OUT.OUTn** bits state
- **HWCR.ACT** bit state

The state diagram including the possible transitions is shown in **Figure 13**. The behaviour of TLE75004-EPD as well as some parameters may change in dependence from the operation mode of the device. Furthermore, due to the undervoltage detection circuitry which monitors V_S and V_{DD} supply voltages, some changes within the same operation mode can be seen accordingly.

The operation mode of the TLE75004-EPD can be observed by:

- status of output channels
- status of SPI registers
- current consumption at VDD pin (I_{VDD})
- current consumption at VS pin (I_{VS})

The default operation mode to switch ON the loads is Active mode. If the device is not in Active mode and a request to switch ON one or more outputs comes (via SPI or via Input pins), it will switch into Active or Limp Home mode, according to IDLE pin status. Due to the time needed for such transitions, output turn-on time t_{ON} will be extended due to the mode transition latency.

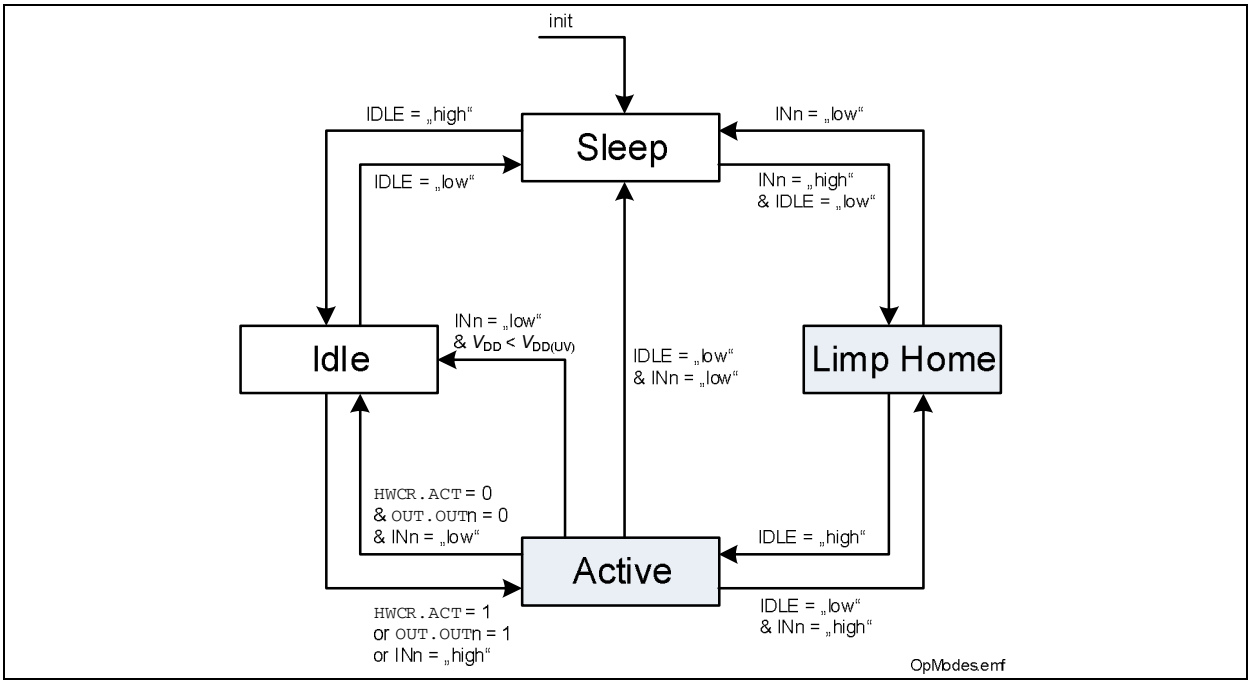


Figure 13 Operation Mode state diagram

Table 7 shows the correlation between device operation modes, V_S and V_{DD} supply voltages, and state of the most important functions (channels operativity, SPI communication and SPI registers).

Table 7 Device function in relation to operation modes, V_S and V_{DD} voltages

Operation Mode	Function	Undervoltage condition on V_S [1] $V_{DD} \le V_{DD(UV)}$	Undervoltage condition on V_S $V_{DD} > V_{DD(UV)}$	V_S not in undervoltage $V_{DD} \le V_{DD(UV)}$	V_S not in undervoltage $V_{DD} > V_{DD(UV)}$
Sleep	Channels	not available	not available	not available	not available
	SPI comm.	not available	not available	not available	not available
	SPI registers	reset	reset	reset	reset
Idle	Channels	not available	not available	not available	not available
	SPI comm.	not available	✓	not available	✓
	SPI registers	reset	✓	reset	✓
Active	Channels	not available	✓	✓ (IN pins only)	✓
	SPI comm.	not available	✓	not available	✓
	SPI registers	reset	✓	reset	✓
Limp Home	Channels	not available	✓ (IN pins only)	✓ (IN pins only)	✓ (IN pins only)
	SPI comm.	not available	✓ (read-only)	not available	✓ (read-only)
	SPI registers	reset	✓ (read-only)[2]	reset	✓ (read-only)[2]

1) see **Chapter 6.2.1** for more details

2) see **Chapter 6.1.5** for a detailed overview

6.1.1 Power-up

The Power-up condition is satisfied when one of the supply voltages (V_S or V_{DD}) is applied to the device and the INn or IDLE pins are set to “high”. If V_S is above the threshold $V_{S(OP)}$ or if V_{DD} is above the threshold $V_{DD(LOP)}$ the internal power-on signal is set.

6.1.2 Sleep mode

When TLE75004-EPD is in Sleep mode, all outputs are OFF and the SPI registers are reset, independently from the supply voltages. The current consumption is minimum. See parameters $I_{VDD(SLEEP)}$ and $I_{VS(SLEEP)}$, or parameter I_{SLEEP} for the whole device.

6.1.3 Idle mode

In Idle mode, the current consumption of the device can reach the limits given by parameters $I_{VDD(IDLE)}$ and $I_{VS(IDLE)}$, or by parameter I_{IDLE} for the whole device. The internal voltage regulator is working. Diagnosis functions are not available. The output channels are switched OFF, independently from the supply voltages. When V_{DD} is available, the SPI registers are working and SPI communication is possible. In Idle mode the **ERRn** bits are not cleared for functional safety reasons.

6.1.4 Active mode

Active mode is the normal operation mode of TLE75004-EPD when no Limp Home condition is set and it is necessary to drive some or all loads. Voltage levels of V_{DD} and V_S influence the behavior as described at the beginning of **Chapter 6**. Device current consumption is specified with $I_{VDD(ACTIVE)}$ and $I_{VS(ACTIVE)}$ (I_{ACTIVE} for the whole device). The device enters Active mode when IDLE pin is set to “high” and one of the input pins is set to “high” or one **OUT.OUTn** bit is set to “1”. If **HWCR.ACT** is set to “0”, the device returns to Idle mode as soon as all inputs pins are set to “low” and **OUT.OUTn** bits are set to “0”. If **HWCR.ACT** is set to “1”, the device remains in Active mode independently of the status of input pins and **OUT.OUTn** bits. An undervoltage condition on V_{DD} supply brings the device into Idle mode, if all input pins are set to “low”. Even if the registers **MAPIN0** and **MAPIN1** are both set to “00_H” but one of the input pins INn is set to “high”, the device goes into Active mode.

6.1.5 Limp Home mode

TLE75004-EPD enters Limp Home mode when IDLE pin is “low” and one of the input pins is set to “high”, switching ON the channel connected to it. SPI communication is possible but only in read-only mode (SPI registers can be read but cannot be written). More in detail:

- **UVRVS** and **LOPVDD** are set to “1”
- **MODE** bits are set to “01_B” (Limp Home mode)
- **TER** bit is set to “1” on the first SPI command after entering Limp Home mode. Afterwards it works normally
- **OLOFF** bits is set to “0”
- **ERRn** bits work normally
- **DIAG_OSM.OUTn** bits can be read and work normally
- All other registers are set to their default value and cannot be programmed as long as the device is in Limp Home mode

See **Table 6** for a detailed overview of supply voltage conditions required to switch ON channels 2 and 3 during Limp Home. All other channels are OFF.

A transmission of SPI commands during transition from Active to Limp Home mode or Limp Home to Active mode may result in undefined SPI responses.

6.1.6 Definition of Power Supply modes transition times

The channel turn-ON time is as defined by parameter t_{ON} when TLE75004-EPD is in Active mode or in Limp Home mode. In all other cases, it is necessary to add the transition time required to reach one of the two aforementioned Power Supply modes (as shown in **Figure 14**).

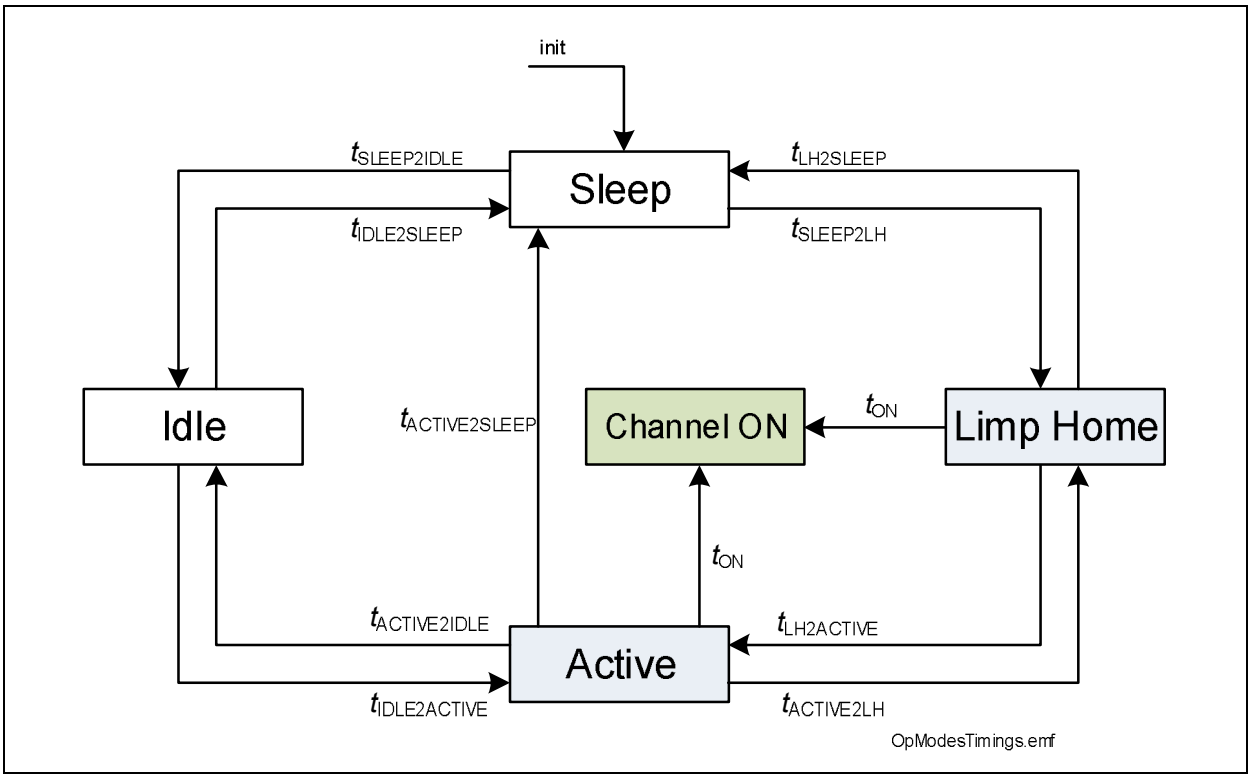


Figure 14 Transition Time diagram

6.2 Reset condition

One of the following 3 conditions resets the SPI registers to the default value:

- V_{DD} is not present or below the undervoltage threshold $V_{DD(UV)}$
- IDLE pin is set to “low”
- a reset command (**HWCR.RST** set to “1”) is executed
  - **ERRn** bits are not cleared by a reset command (for functional safety)
  - **UVRVS** and **LOPVDD** bits are cleared by a reset command

In particular, all channels are switched OFF (if there are no input pin set to “high”) and the Input Mapping configuration is reset.

6.2.1 Undervoltage on V_S

Between $V_{S(UV)}$ and $V_{S(OP)}$ the undervoltage mechanism is triggered. If the device is operative and the supply voltage drops below the undervoltage threshold $V_{S(UV)}$, the logic set the bit **UVRVS** to “1”. As soon as the supply voltage VS is above the minimum voltage operative threshold $V_{S(OP)}$, the bit **UVRVS** is set to “0” after the first Standard Diagnosis readout. Undervoltage condition on VS influences the status of the channels, as described in **Table 6**. **Figure 15** sketches the undervoltage behavior.

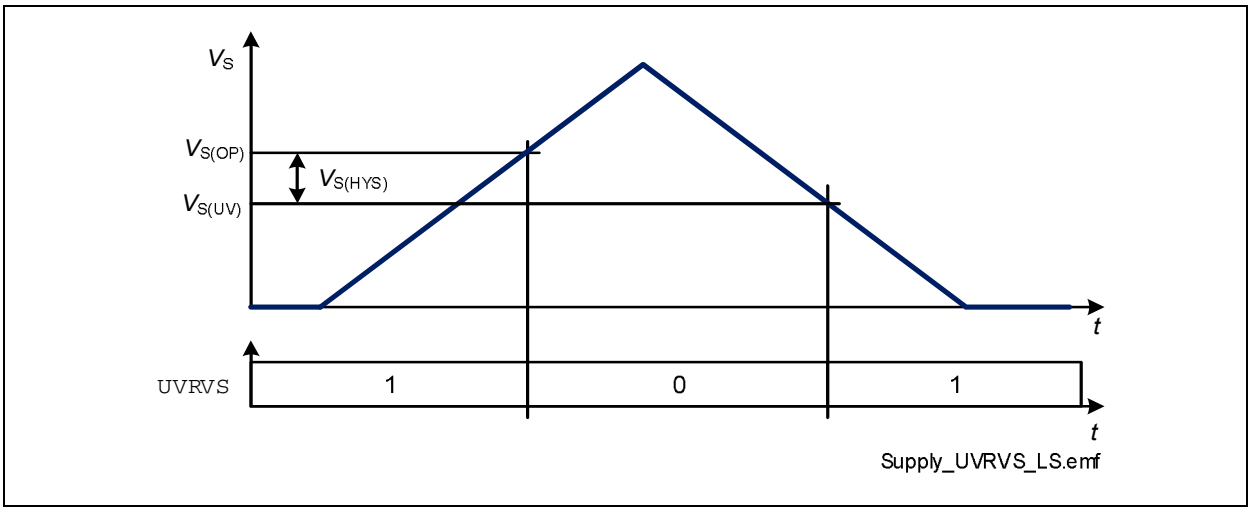


Figure 15 V_S Undervoltage Behavior

6.2.2 Low Operating Power on V_{DD}

When V_{DD} supply voltage is in the range indicated by $V_{DD(LOP)}$, the bit **LOPVDD** is set to “1”. As soon as V_{DD} > $V_{DD(LOP)}$ the bit **LOPVDD** is set to “0” after the first Standard Diagnosis readout.

If V_{DD} supply voltage is not present, a voltage applied to pins CSN or SO can supply the internal logic (not recommended in normal operation due to internal design limitations).

6.3 Electrical Characteristics Power Supply

Table 8 Electrical Characteristics Power Supply

V_{DD} = 3 V to 5.5 V, V_S = 7 V to 18 V, T_J = -40 °C to +150 °C, all voltages with respect to ground, positive currents flowing as described in **Figure 3** (unless otherwise specified)
Typical values: V_{DD} = 5 V, V_S = 13.5 V, T_J = 25 °C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
VS pin							
Analog supply undervoltage shutdown	$V_{S(UV)}$	1.5	–	3.0	V	OUTn = ON from $V_{DS} \leq$ 1 V to **UVRVS** = 1_B R_L = 50 Ω	P_6.3.1
Analog supply minimum operative voltage	$V_{S(OP)}$	–	–	4.0	V	**OUT.OUTn** = 1_B from **UVRVS** = 1_B to $V_{DS} \leq$ 1 V R_L = 50 Ω	P_6.3.2
Undervoltage shutdown hysteresis	$V_{S(HYS)}$	–	1	–	V	1)	P_6.3.3
Analog supply current consumption in Sleep mode with loads	$I_{VS(SLEEP)}$	–	0.1	3	µA	1) V_{IDLE} floating V_{INn} floating $V_{CSN} = V_{DD}$ $T_J \leq$ 85 °C	P_6.3.4
Analog supply current consumption in Sleep mode with loads	$I_{VS(SLEEP)}$	–	0.1	–	µA	1) V_{IDLE} floating V_{INn} floating $V_{CSN} = V_{DD}$ $T_J \leq$ 85 °C VS = 13.5 V	P_6.3.63
Analog supply current consumption in Sleep mode with loads	$I_{VS(SLEEP)}$	–	0.1	20	µA	V_{IDLE} floating V_{INn} floating $V_{CSN} = V_{DD}$ T_J = 150 °C	P_6.3.5
Analog supply current consumption in Idle mode with loads	$I_{VS(IDLE)}$	–	–	2.2	mA	IDLE = “high” V_{INn} floating f_{SCLK} = 0 MHz **HWCR.ACT** = 0_B **OUT.OUTn** = 0_B **DIAG_IOL.OUTn** = 0_B $V_{CSN} = V_{DD}$	P_6.3.6

Table 8 Electrical Characteristics Power Supply (cont'd)

V_{DD} = 3 V to 5.5 V, V_S = 7 V to 18 V, T_J = -40 °C to +150 °C, all voltages with respect to ground, positive currents flowing as described in **Figure 3** (unless otherwise specified)
Typical values: V_{DD} = 5 V, V_S = 13.5 V, T_J = 25 °C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Analog supply current consumption in Idle mode with loads (COR)	$I_{VS(IDLE)}$	–	–	0.3	mA	IDLE = "high" V_{INn} floating f_{SCLK} = 0 MHz **HWCR.ACT** = 0_B **OUT.OUTn** = 0_B **DIAG_IOL.OUTn** = 0_B $V_{CSN} = V_{DD}$ $V_S \leq V_{DD}$ - 1 V	P_6.3.7
Analog supply current consumption in Active mode with loads - channels OFF	$I_{VS(ACTIVE)}$	–	–	3.2	mA	IDLE = "high" V_{INn} floating f_{SCLK} = 0 MHz **HWCR.ACT** = 1_B **OUT.OUTn** = 0_B **DIAG_IOL.OUTn** = 0_B $V_{CSN} = V_{DD}$	P_6.3.11
Analog supply current consumption in Active mode with loads - channels OFF (COR)	$I_{VS(ACTIVE)}$	–	0.1	0.3	mA	IDLE = "high" V_{INn} floating f_{SCLK} = 0 MHz **HWCR.ACT** = 1_B **OUT.OUTn** = 0_B **DIAG_IOL.OUTn** = 0_B $V_{CSN} = V_{DD}$ $V_S \leq V_{DD}$ - 1 V	P_6.3.12
Analog supply current consumption in Active mode with loads - channels ON	$I_{VS(ACTIVE)}$	–	–	3.2	mA	IDLE = "high" V_{INn} floating f_{SCLK} = 0 MHz **HWCR.ACT** = 1_B **OUT.OUTn** = 1_B **DIAG_IOL.OUTn** = 0_B $V_{CSN} = V_{DD}$	P_6.3.19

Table 8 Electrical Characteristics Power Supply (cont'd)

V_{DD} = 3 V to 5.5 V, V_S = 7 V to 18 V, T_J = -40 °C to +150 °C, all voltages with respect to ground, positive currents flowing as described in **Figure 3** (unless otherwise specified)
Typical values: V_{DD} = 5 V, V_S = 13.5 V, T_J = 25 °C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Analog supply current consumption in Active mode with loads - channels ON (COR)	$I_{VS(ACTIVE)}$	–	0.1	0.3	mA	IDLE = "high" V_{INn} floating f_{SCLK} = 0 MHz **HWCR.ACT** = 1_B **OUT.OUTn** = 1_B **DIAG_IOL.OUTn** = 0_B $V_{CSN} = V_{DD}$ $V_S \leq V_{DD}$ - 1 V	P_6.3.20
VDD pin							
Logic Supply Operating voltage	$V_{DD(OP)}$	3.0	–	5.5	V	f_{SCLK} = 5 MHz	P_6.3.23
Logic Supply Lower Operating Voltage	$V_{DD(LOP)}$	3.0	–	4.5	V	–	P_6.3.24
Undervoltage shutdown	$V_{DD(UV)}$	1	–	3.0	V	V_{SI} = 0 V V_{SCLK} = 0 V V_{CSN} = 0 V SO from "low" to high impedance	P_6.3.25
Logic supply current in Sleep mode	$I_{VDD(SLEEP)}$	–	0.1	2.5	µA	[1] V_{IDLE} floating V_{INn} floating $V_{CSN} = V_{DD}$ $T_J \leq 85$ °C	P_6.3.26
Logic supply current in Sleep mode	$I_{VDD(SLEEP)}$	–	–	10	µA	V_{IDLE} floating V_{INn} floating $V_{CSN} = V_{DD}$ T_J = 150 °C	P_6.3.27
Logic supply current in Idle mode	$I_{VDD(IDLE)}$	–	–	0.3	mA	IDLE = "high" V_{INn} floating f_{SCLK} = 0 MHz **HWCR.ACT** = 0_B **OUT.OUTn** = 0_B $V_{CSN} = V_{DD}$	P_6.3.28
Logic supply current in Idle mode (COR)	$I_{VDD(IDLE)}$	–	–	2.2	mA	IDLE = "high" V_{INn} floating f_{SCLK} = 0 MHz **HWCR.ACT** = 0_B **OUT.OUTn** = 0_B $V_{CSN} = V_{DD}$ $V_S \leq V_{DD}$ - 1 V	P_6.3.29

Table 8 Electrical Characteristics Power Supply (cont'd)

V_{DD} = 3 V to 5.5 V, V_S = 7 V to 18 V, T_J = -40 °C to +150 °C, all voltages with respect to ground, positive currents flowing as described in **Figure 3** (unless otherwise specified)
Typical values: V_{DD} = 5 V, V_S = 13.5 V, T_J = 25 °C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Logic supply current in Active mode - channels OFF	$I_{VDD(ACTIVE)}$	–	–	0.3	mA	IDLE = "high" V_{INn} floating f_{SCLK} = 0 MHz **HWCR.ACT** = 1_B **OUT.OUTn** = 0_B $V_{CSN} = V_{DD}$	P_6.3.30
Logic supply current in Active mode - channels OFF (COR)	$I_{VDD(ACTIVE)}$	–	–	3.2	mA	IDLE = "high" V_{INn} floating f_{SCLK} = 0 MHz **HWCR.ACT** = 1_B **OUT.OUTn** = 0_B $V_{CSN} = V_{DD}$ $V_S \leq V_{DD}$ - 1 V	P_6.3.34
Logic supply current in Active mode - channels ON	$I_{VDD(ACTIVE)}$	–	–	0.3	mA	IDLE = "high" V_{INn} floating f_{SCLK} = 0 MHz **HWCR.ACT** = 1_B **OUT.OUTn** = 1 $V_{CSN} = V_{DD}$	P_6.3.35
Logic supply current in Active mode - channels ON (COR)	$I_{VDD(ACTIVE)}$	–	–	3.2	mA	IDLE = "high" V_{INn} floating f_{SCLK} = 0 MHz **HWCR.ACT** = 1_B **OUT.OUTn** = 1_B $V_{CSN} = V_{DD}$ $V_S = V_{DD}$ - 1 V	P_6.3.38
Overall current consumption							
Overall current consumption in Sleep mode $I_{VS(SLEEP)} + I_{VDD(SLEEP)}$	I_{SLEEP}	–	–	5	µA	[1] V_{IDLE} floating V_{INn} floating $V_{CSN} = V_{DD}$ $T_J \leq 85$ °C	P_6.3.40
Overall current consumption in Sleep mode $I_{VS(SLEEP)} + I_{VDD(SLEEP)}$	I_{SLEEP}	–	–	5	µA	[1] V_{IDLE} floating V_{INn} floating $V_{CSN} = V_{DD}$ $T_J \leq 85$ °C V_S = 13.5 V	P_6.3.64

Table 8 Electrical Characteristics Power Supply (cont'd)

V_{DD} = 3 V to 5.5 V, V_S = 7 V to 18 V, T_J = -40 °C to +150 °C, all voltages with respect to ground, positive currents flowing as described in **Figure 3** (unless otherwise specified)
Typical values: V_{DD} = 5 V, V_S = 13.5 V, T_J = 25 °C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Overall current consumption in Sleep mode $I_{VS(SLEEP)} + I_{VDD(SLEEP)}$	I_{SLEEP}	–	–	30	µA	V_{IDLE} floating V_{INn} floating $V_{CSN} = V_{DD}$ T_J = 150 °C	P_6.3.41
Overall current consumption in Idle mode $I_{VS(IDLE)} + I_{VDD(IDLE)}$	I_{IDLE}	–	–	2.5	mA	IDLE = "high" V_{INn} floating f_{SCLK} = 0 MHz **HWCR.ACT** = 0_B **OUT.OUTn** = 0_B **DIAG_IOL.OUTn** = 0_B $V_{CSN} = V_{DD}$	P_6.3.42
Overall current consumption in Active mode - channels OFF $I_{VS(ACTIVE)} + I_{VDD(ACTIVE)}$	I_{ACTIVE}	–	–	3.5	mA	IDLE = "high" V_{INn} floating f_{SCLK} = 0 MHz **HWCR.ACT** = 1_B **OUT.OUTn** = 0_B **DIAG_IOL.OUTn** = 0_B $V_{CSN} = V_{DD}$	P_6.3.46
Overall current consumption in Active mode - channels ON $I_{VS(ACTIVE)} + I_{VDD(ACTIVE)}$	I_{ACTIVE}	–	–	3.5	mA	IDLE = "high" V_{INn} floating f_{SCLK} = 0 MHz **HWCR.ACT** = 1_B **OUT.OUTn** = 1_B **DIAG_IOL.OUTn** = 0_B $V_{CSN} = V_{DD}$	P_6.3.51
Voltage difference between V_S and V_{DD} supply lines	V_{SDIFF}	–	200	–	mV	1)	P_6.3.52
Timings							
Sleep to Idle delay	$t_{SLEEP2IDLE}$	–	200	400	µs	1) from IDLE pin to **TER** + **INST** register = 8680_H (see **Chapter 10.6.1** for details)	P_6.3.53

Table 8 Electrical Characteristics Power Supply (cont'd)

V_{DD} = 3 V to 5.5 V, V_S = 7 V to 18 V, T_J = -40 °C to +150 °C, all voltages with respect to ground, positive currents flowing as described in **Figure 3** (unless otherwise specified)
Typical values: V_{DD} = 5 V, V_S = 13.5 V, T_J = 25 °C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Idle to Sleep delay	$t_{IDLE2SLEEP}$	–	100	200	µs	[1] from IDLE pin to Standard Diagnosis = 0000_H (see **Chapter 10.5** for details) external pull-down SO to GND required	P_6.3.54
Idle to Active delay	$t_{IDLE2ACTIVE}$	–	100	200	µs	[1] from INn or CSN pins to **MODE** = 10_B	P_6.3.55
Active to Idle delay	$t_{ACTIVE2IDLE}$	–	100	200	µs	[1] from INn or CSN pins to **MODE** = 11_B	P_6.3.56
Sleep to Limp Home delay	$t_{SLEEP2LH}$	–	300 $+t_{ON}$	600 $+t_{ON}$	µs	[1] from INn pins to V_{DS} = 10% V_S	P_6.3.57
Limp Home to Sleep delay	$t_{LH2SLEEP}$	–	200 $+t_{OFF}$	400 $+t_{OFF}$	µs	[1] from INn pins to Standard Diagnosis = 0000_H (see **Chapter 10.6.1** for details). External pull-down SO to GND required	P_6.3.58
Limp Home to Active delay	$t_{LH2ACTIVE}$	–	50	100	µs	[1] from IDLE pin to **MODE** = 10_B	P_6.3.59

Table 8 Electrical Characteristics Power Supply (cont'd)

V_{DD} = 3 V to 5.5 V, V_S = 7 V to 18 V, T_J = -40 °C to +150 °C, all voltages with respect to ground, positive currents flowing as described in **Figure 3** (unless otherwise specified)
Typical values: V_{DD} = 5 V, V_S = 13.5 V, T_J = 25 °C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Active to Limp Home delay	$t_{ACTIVE2LH}$	–	50	100	µs	1) from IDLE pin to **TER** + **INST** register = 8683_H (IN0 = IN1 = "high") or 8682_H(IN1 = "high", IN0 = "low") or 8681_H (IN1 = "low", IN0 = "high") (see **Chapter 10.5** for details)	P_6.3.60
Active to Sleep delay	$t_{ACTIVE2SLEEP}$	–	50	100	µs	1) from IDLE pin to Standard Diagnosis = 0000_H (see **Chapter 10.6.1** for details). External pull-down SO to GND required.	P_6.3.61

1) Not subject to production test - specified by design

7 Power Stages

The TLE75004-EPD is an four channels low-side relay switch. The power stages are built by N-channel lateral power MOSFET transistors.

7.1 Output ON-state resistance

The ON-state resistance $R_{DS(ON)}$ depends on the supply voltage as well as the junction temperature T_J.

7.1.1 Switching Resistive Loads

When switching resistive loads the following switching times and slew rates can be considered.

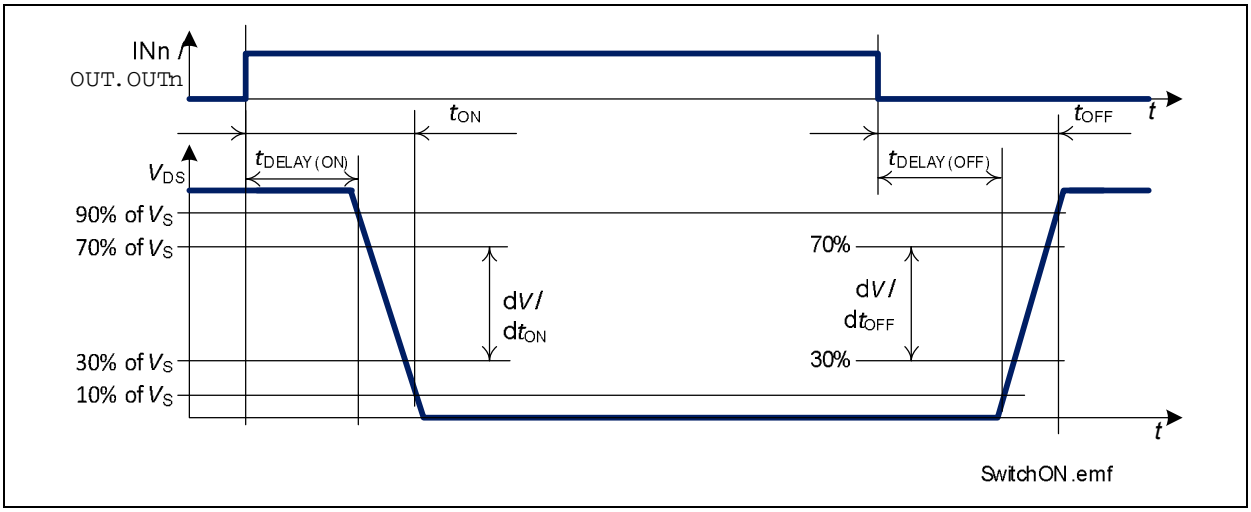


Figure 16 Switching a Resistive Load

7.1.2 Inductive Output Clamp

When switching off inductive loads, the voltage across the power switch rises to $V_{DS(CL)}$ potential, because the inductance intends to continue driving the current. The voltage clamping is necessary to prevent device destruction.

Figure 17 shows a concept drawing of the implementation. Nevertheless, the maximum allowed load inductance is limited. The clamping structure protects the device in all operative modes (Sleep, Idle, Active, Limp Home).

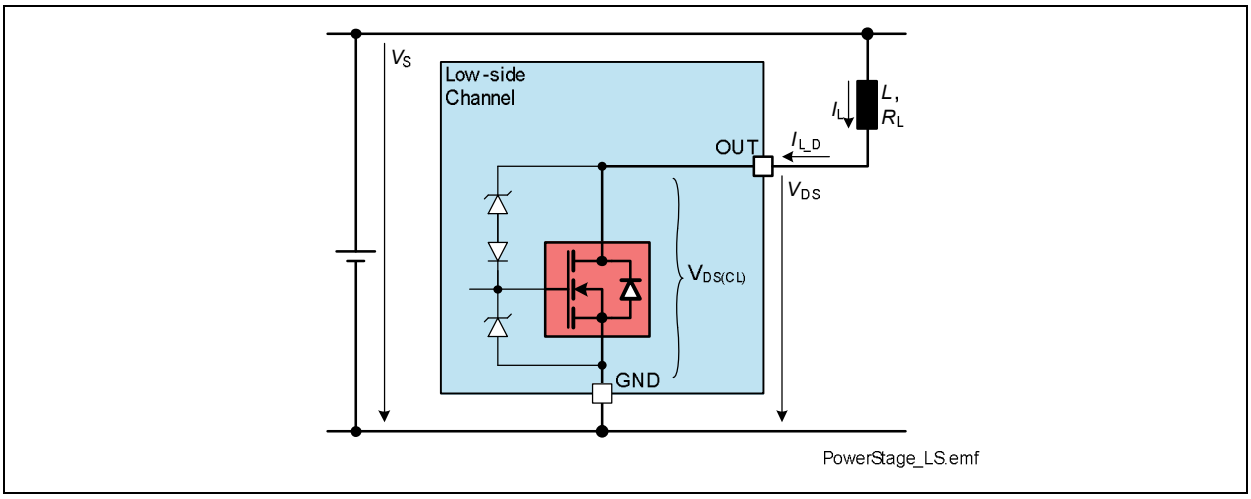


Figure 17 Output Clamp concept

7.1.3 Maximum Load Inductance

During demagnetization of inductive loads, energy has to be dissipated in the TLE75004-EPD. **Equation (7.1)** shows how to calculate the energy for low-side switches:

$$E = V_{DS(CL)} \cdot \left[\frac{V_S - V_{DS(CL)}}{R_L} \cdot \ln\left(1 - \frac{R_L \cdot I_L}{V_S - V_{DS(CL)}}\right) + I_L \right] \cdot \frac{L}{R_L} \quad (7.1)$$

The maximum energy, which is converted into heat, is limited by the thermal design of the component. The E_{AR} value provided in **Table 2** assumes that all channels can dissipate the same energy when the inductances connected to the outputs are demagnetized at the same time.

7.2 Switching Channels in parallel

In case of appearance of a short circuit with channels in parallel, it may happen that the two channels switch OFF asynchronously, therefore bringing an additional thermal stress to the channel that switches OFF last. In order to avoid this condition, it is possible to parametrize in the SPI registers the parallel operation of two neighbour channels (bits **HWCR.PAR**). When operating in this mode, the fastest channel to react to an Over Load or Over Temperature condition will deactivate also the other. The inductive energy that two channels can handle once set in parallel is lower than twice the single channel energy (see P_7.6.11). It is possible to synchronize the following couples of channels:

- channel 0 and channel 2 → **HWCR.PAR** (0) set to “1”
- channel 1 and channel 3 → **HWCR.PAR** (1) set to “1”

The synchronization bits influence only how the channels react to Over Load or Over Temperature conditions. Synchronized channels have to be switched ON and OFF individually by the micro-controller.

7.3 Electrical Characteristics Power Stages

Table 9 Electrical Characteristics: Power Stage

V_{DD} = 3 V to 5.5 V, V_S = 7 V to 18 V, T_J = -40 °C to +150 °C (unless otherwise specified)
Typical values: V_{DD} = 5 V, V_S = 13.5 V, T_J = 25 °C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output Characteristics							
On-State Resistance	$R_{DS(ON)}$	–	1.0	–	Ω	1) T_J = 25 °C	P_7.6.1
On-State Resistance	$R_{DS(ON)}$	–	1.8	2.2	Ω	T_J = 150 °C $I_L = I_{L(EAR)}$ = 220 mA	P_7.6.2
Nominal load current (all channels active)	$I_{L(NOM)}$	–	470	500 2)3)	mA	1) T_A = 85 °C $T_J \leq$ 150 °C	P_7.6.6
Nominal load current (all channels active)	$I_{L(NOM)}$	–	370	500 2)3)	mA	1) T_A = 105 °C $T_J \leq$ 150 °C	P_7.6.7
Load current for maximum energy dissipation - repetitive (all channels active)	$I_{L(EAR)}$	–	220	–	mA	1) T_A = 85 °C $T_J \leq$ 150 °C	P_7.6.8
Maximum energy dissipation repetitive pulses - 2*$I_{L(EAR)}$ (two channels in parallel)	E_{AR}	–	–	15	mJ	1) $T_{J(0)}$ = 85 °C $I_{L(0)} = 2*I_{L(EAR)}$ $2*10^6$ cycles **HWCR.PAR** = “1” for affected channels	P_7.6.11
Power stage voltage drop at low battery	$V_{DS(OP)}$	–	–	1	V	R_L = 50 Ω supplied by V_S = 4 V $V_S = V_{S(OP),max}$ or V_{DD} = 4.5 V, VS pin open refer to **Figure 17**	P_7.6.12
Drain to Source Output clamping voltage	$V_{DS(CL)}$	42	46	55	V	I_L = 20 mA	P_7.6.16
Output leakage current (each channel) $T_J \leq$ 85 °C	$I_{L(OFF)}$	–	0.01	0.5	µA	1) V_{IN} = 0 V or floating V_{DS} = 28 V **OUT.OUTn** = 0 $T_J \leq$ 85 °C	P_7.6.19

Table 9 Electrical Characteristics: Power Stage (cont'd)

V_{DD} = 3 V to 5.5 V, V_S = 7 V to 18 V, T_J = -40 °C to +150 °C (unless otherwise specified)
Typical values: V_{DD} = 5 V, V_S = 13.5 V, T_J = 25 °C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output leakage current (each channel) T_J = 150 °C (Low-Side channels)	$I_{L(OFF)}$	–	0.1	5	µA	1) V_{IN} = 0 V or floating V_{DS} = 28 V **OUT.OUTn** = 0 T_J = 150 °C	P_7.6.20
Timings							
Turn-ON delay (from INn pin or bit to V_{OUT} = 90% V_S)	$t_{DELAY(ON)}$	1	4	8	µs	R_L = 50 Ω V_S = 13.5 V Active mode or Limp Home mode	P_7.6.21
Turn-OFF delay (from INn pin or bit to V_{OUT} = 10% V_S)	$t_{DELAY(OFF)}$	1	6	12	µs	R_L = 50 Ω V_S = 13.5 V Active mode or Limp Home mode	P_7.6.22
Turn-ON time (from INn pin or bit to V_{OUT} = 10% V_S)	t_{ON}	6	15	35	µs	R_L = 50 Ω V_S = 13.5 V Active mode or Limp Home mode	P_7.6.23
Turn-OFF time (from INn pin or bit to V_{OUT} = 90% V_S)	t_{OFF}	6	15	35	µs	R_L = 50 Ω V_S = 13.5 V Active mode or Limp Home mode	P_7.6.24
Turn-ON/OFF matching	t_{ON} - t_{OFF}	-10	0	10	µs	R_L = 50 Ω V_S = 13.5 V Active mode or Limp Home mode	P_7.6.25
Turn-ON slew rate V_{DS} = 70% to 30% V_S	dV/dt_{ON}	0.7	1.3	1.9	V/µs	R_L = 50 Ω V_S = 13.5 V Active mode or Limp Home mode	P_7.6.26
Turn-OFF slew rate V_{DS} = 30% to 70% V_S	$-dV/dt_{OFF}$	0.7	1.3	1.9	V/µs	R_L = 50 Ω V_S = 13.5 V Active mode or Limp Home mode	P_7.6.27
Internal reference frequency synchronization time	t_{SYNC}	–	5	10	µs	1)	P_7.6.45

1) Not subject to production test - specified by design
2) If one channel has $I_{L(NOM),max}$ applied, the remaining channels must be underloaded accordingly so that T_J < 150°C
3) $I_{L(NOM),max}$ can reach $I_{L(OVL1),min}$

8 Protection Functions

8.1 Over Load Protection

The TLE75004-EPD is protected in case of over load or short circuit of the load. There are two over load current thresholds (see **Figure 18**):

- $I_{L(OVL0)}$ between channel switch ON and t_{OVLIN}
- $I_{L(OVL1)}$ after t_{OVLIN}

Every time the channel is switched OFF for a time longer than 2 * t_{SYNC} the over load current threshold is set back to $I_{L(OVL0)}$.

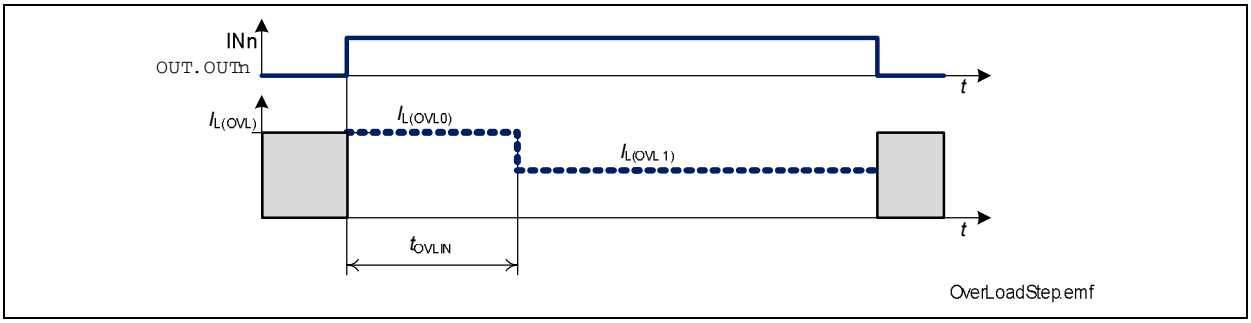


Figure 18 Over Load current thresholds

In case the load current is higher than $I_{L(OVL0)}$ or $I_{L(OVL1)}$, after time $t_{OFF(OVL)}$ the over loaded channel is switched OFF and the according diagnosis bit **ERRn** is set. The channel can be switched ON after clearing the protection latch by setting the corresponding **HWCR_OCL.OUTn** bit to “1”. This bit is set back to “0” internally after de-latching the channel. Please refer to **Figure 19** for details.

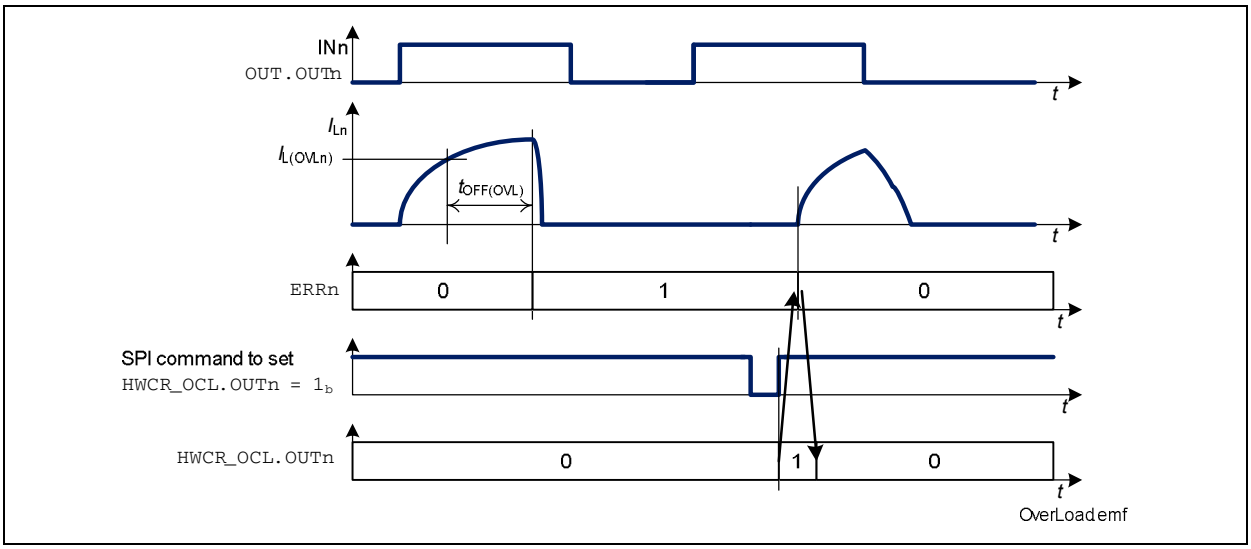


Figure 19 Latch OFF at Over Load

8.2 Over Temperature Protection

A temperature sensor is integrated for each channel, causing an overheated channel to switch OFF to prevent destruction. The according diagnosis bit **ERRn** is set (combined with Over Load protection). The channel can

be switched ON after clearing the protection latch by setting the corresponding **HWCR_OCL.OUTn** bit to “1”. This bit is set back to “0” internally after de-latching the channel.

8.3 Over Temperature and Over Load Protection in Limp Home mode

When TLE75004-EPD is in Limp Home mode, channels 2 and 3 can be switched ON using the input pins. In case of Over Load, Short Circuit or Over Temperature the channels switch OFF. If the input pins remain “high”, the channels restart with the following timings:

- 10 ms (first 8 retries)
- 20 ms (following 8 retries)
- 40 ms (following 8 retries)
- 80 ms (as long as the input pin remains “high” and the error is still present)

If at any time the input pin is set to “low” for longer than 2*t_{SYNC}, the restart timer is reset. At the next channel activation while in Limp Home mode the timer starts from 10 ms again. See **Figure 20** for details. Over Load current thresholds behave as described in **Chapter 8.1**.

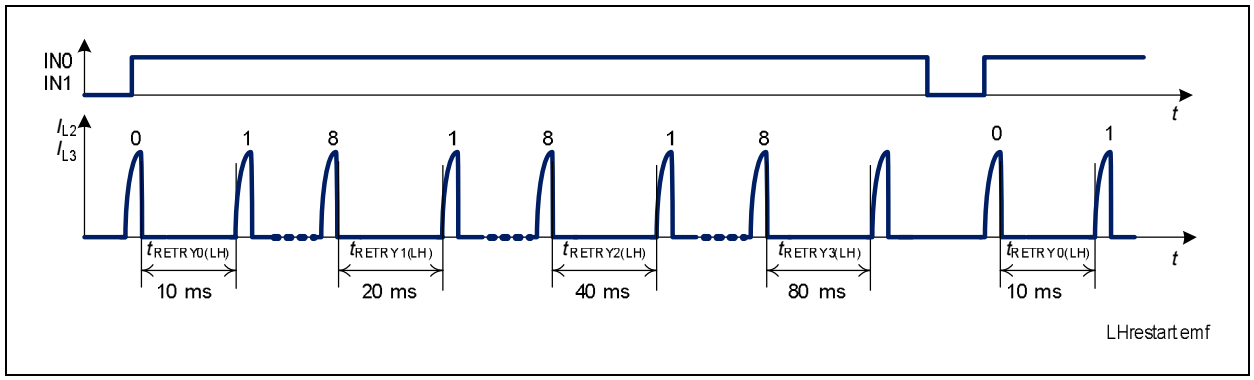


Figure 20 Restart timer in Limp Home mode

8.4 Reverse Polarity Protection

In Reverse Polarity (also known as Reverse Battery) condition, power dissipation is caused by the intrinsic body diode of each DMOS channel. Each ESD diode of the logic and supply pins contributes to total power dissipation. The reverse current through the channels has to be limited by the connected loads. The current through digital power supply V_{DD} and input pins has to be limited as well (please refer to the Absolute Maximum Ratings listed on **Chapter 4.1**).

Note: No protection mechanism like temperature protection or current limitation is active during reverse polarity.

8.5 Over Voltage Protection

In the case of supply voltages between $V_{S(SC)}$ and $V_{S(LD)}$ the output transistors are still operational and follow the input pins or the **OUT** register.

In addition to the output clamp for inductive loads as described in **Chapter 7.1.2**, there is a clamp mechanism available for over voltage protection for the logic and all channels, monitoring the voltage between VS and GND pins ($V_{S(AZ)}$).

8.6 Electrical Characteristics Protection

Table 10 Electrical Characteristics Protection

V_{DD} = 3 V to 5.5 V, V_S = 7 V to 18 V, T_J = -40 °C to +150 °C (unless otherwise specified)
Typical values: V_{DD} = 5 V, V_S = 13.5 V, T_J = 25 °C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Over Load							
Over Load detection current	$I_{L(OVL0)}$	1.3	1.7	2.3	A	T_J = -40 °C	P_8.8.19
Over Load detection current	$I_{L(OVL0)}$	1.25	1.55	2.3	A	1) T_J = 25 °C	P_8.8.20
Over Load detection current	$I_{L(OVL0)}$	1	1.45	2	A	T_J = 150 °C	P_8.8.21
Over Load detection current	$I_{L(OVL1)}$	0.7	0.95	1.3	A	T_J = -40 °C	P_8.8.22
Over Load detection current	$I_{L(OVL1)}$	0.65	0.85	1.3	A	1) T_J = 25 °C	P_8.8.23
Over Load detection current	$I_{L(OVL1)}$	0.5	0.8	1.25	A	T_J = 150 °C	P_8.8.24
Over Load threshold switch delay time	t_{OVLIN}	110	170	260	µs	1)	P_8.8.5
Over Load shut-down delay time	$t_{OFF(OVL)}$	4	7	11	µs	1)	P_8.8.26
Over Temperature and Over Voltage							
Thermal shut-down temperature	$T_{J(SC)}$	150	175[1)]	220[1)]	°C		P_8.8.7
Over voltage protection	$V_{S(AZ)}$	42	50	60	V	I_{VS} = 10 mA Sleep mode	P_8.8.8
Reverse Polarity							
Drain Source diode during reverse polarity	$V_{DS(REV)}$	–	800	–	mV	1) I_L = -10 mA T_J = 25 °C Sleep mode	P_8.8.9
Drain Source diode during reverse polarity	$V_{DS(REV)}$	–	650	–	mV	I_L = -10 mA T_J = 150 °C Sleep mode	P_8.8.10
Timings							
Restart time in Limp Home mode	$t_{RETRY0(LH)}$	7	10	13	ms	1)	P_8.8.13
Restart time in Limp Home mode	$t_{RETRY1(LH)}$	14	20	26	ms	1)	P_8.8.14
Restart time in Limp Home mode	$t_{RETRY2(LH)}$	28	40	52	ms	1)	P_8.8.15
Restart time in Limp Home mode	$t_{RETRY3(LH)}$	56	80	104	ms	1)	P_8.8.16

1) Not subject to production test - specified by design

9 Diagnosis

The SPI of TLE75004-EPD provides diagnosis information about the device and the load status. Each channel diagnosis information is independent from other channels. An error condition on one channel has no influence on the diagnostic of other channels in the device (unless configured to work in parallel, see **Chapter 7.2** for more details).

9.1 Over Load and Over Temperature

When either an Over Load or an Over Temperature occurs on one channel, the diagnosis bit **ERRn** is set accordingly. As described in **Chapter 8.1** and **Chapter 8.2**, the channel latches OFF and must be reactivated setting corresponding **HWCR_OCL.OUTn** bit to “1”.

9.2 Output Status Monitor

The device compares each channel V_{DS} with $V_{DS(OL)}$ and sets the corresponding **DIAG_OSM.OUTn** bits accordingly. The bits are updated every time **DIAG_OSM** register is read.

- $V_{DS} < V_{DS(OL)} \rightarrow$ **DIAG_OSM.OUTn** = “1”

A diagnosis current I_{OL} in parallel to the power switch can be enabled by programming the **DIAG_IOL.OUTn** bit, which can be used for Open Load at OFF detection. Each channel has its dedicated diagnosis current source. If the diagnosis current I_{OL} is enabled or if the channel changes state (ON → OFF or OFF → ON) it is necessary to wait a time t_{OSM} for a reliable diagnosis. Enabling I_{OL} current sources increases the current consumption of the device. Even if an Open Load is detected, the channel is not latched OFF.

See **Figure 21** for a timing overview (the values of **DIAG_IOL.OUTn** refer to a channel in normal operation properly connected to the load).

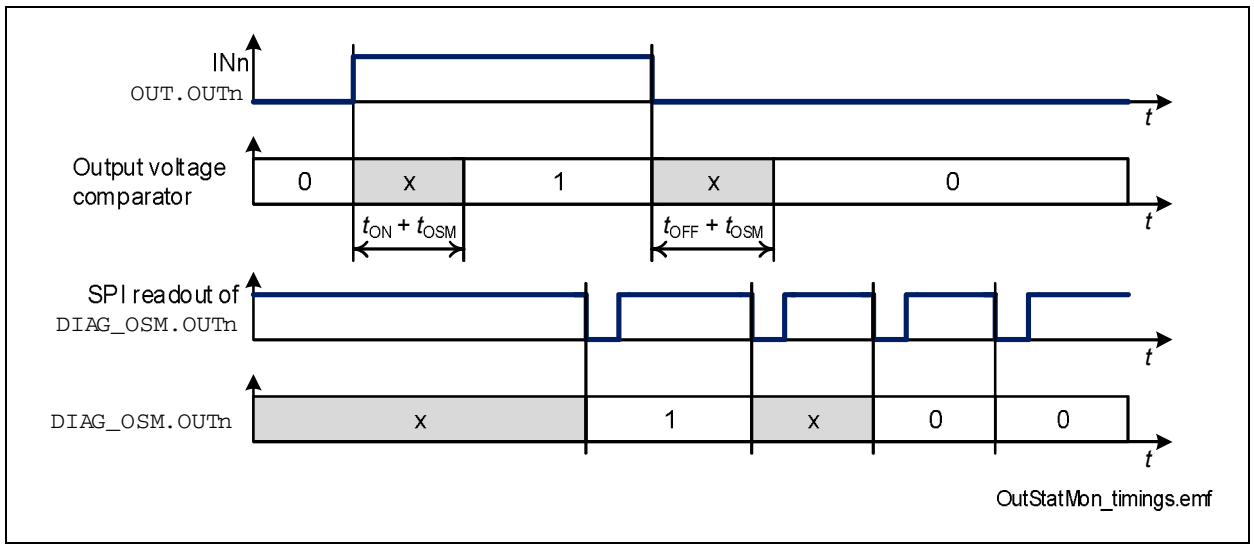


Figure 21 Output Status Monitor timing

Output Status Monitor diagnostic is available when $V_S = V_{S(NOR)}$ and $V_{DD} \geq V_{DD(UV)}$.

Due to the fact that Output Status Monitor checks the voltage level at the outputs in real time, for Open Load in OFF diagnostic it is necessary to synchronize the reading of **DIAG_OSM** register with the OFF state of the channels.

Figure 22 shows how Output Status Monitor is implemented at concept level.

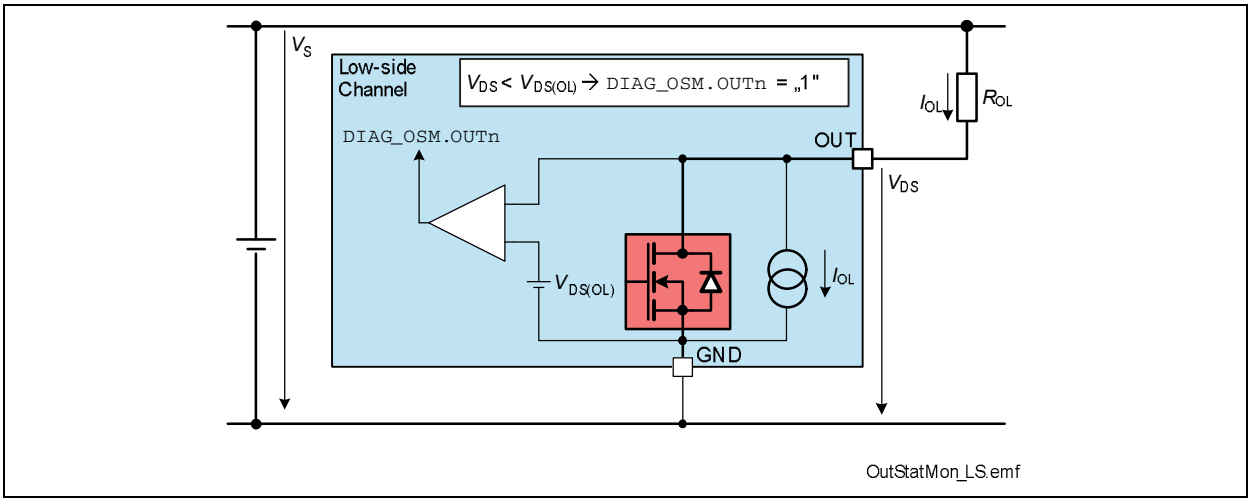


Figure 22 Output Status Monitor - concept

In Standard Diagnosis the bit **OLOFF** represents the OR combination of all **DIAG_OSM.OUTn** bits for all channels in OFF state which have the corresponding current source I_{OL} activated.

9.3 Electrical Characteristics Diagnosis

Table 11 Electrical Characteristics Diagnosis

V_{DD} = 3 V to 5.5 V, V_S = 7 V to 18 V, T_J = -40 °C to +150 °C (unless otherwise specified)
Typical values: V_{DD} = 5 V, V_S = 13.5 V, T_J = 25 °C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output Status Monitor							
Output Status Monitor comparator settling time	t_{OSM}	–	–	20	µs	1)	P_9.5.1
Output Status Monitor threshold voltage	$V_{DS(OL)}$	3	3.3	3.6	V		P_9.5.2
Output diagnosis current	I_{OL}	70	85	100	µA	V_{DS} = 3.3 V	P_9.5.5
Open Load equivalent resistance	R_{OL}	30	–	300	kΩ	1)	P_9.5.6

1) Not subject to production test - specified by design

10 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a full duplex synchronous serial slave interface, which uses four lines: SO, SI, SCLK and CSN. Data is transferred by the lines SI and SO at the rate given by SCLK. The falling edge of CSN indicates the beginning of an access. Data is sampled in on line SI at the falling edge of SCLK and shifted out on line SO at the rising edge of SCLK. Each access must be terminated by a rising edge of CSN. A modulo 8/16 counter ensures that data is taken only when a multiple of 8 bit has been transferred after the first 16 bits. Otherwise a TER bit is asserted. In this way the interface provides daisy chain capability with 16 bit as well as with 8 bit SPI devices.

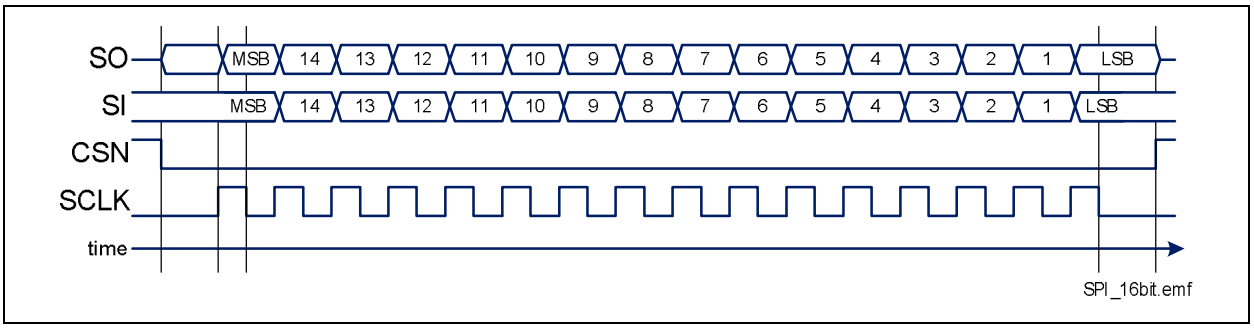


Figure 23 Serial Peripheral Interface

10.1 SPI Signal Description

CSN - Chip Select

The system microcontroller selects the TLE75004-EPD by means of the CSN pin. Whenever the pin is in “low” state, data transfer can take place. When CSN is in "high" state, any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state.

CSN “high” to “low” Transition

- The requested information is transferred into the shift register.
- SO changes from high impedance state to "high" or “low” state depending on the logic OR combination between the transmission error flag (TER) and the signal level at pin SI. This allows to detect a faulty transmission even in daisy chain configuration.
- If the device is in Sleep mode, SO pin remains in high impedance state and no SPI transmission occurs.

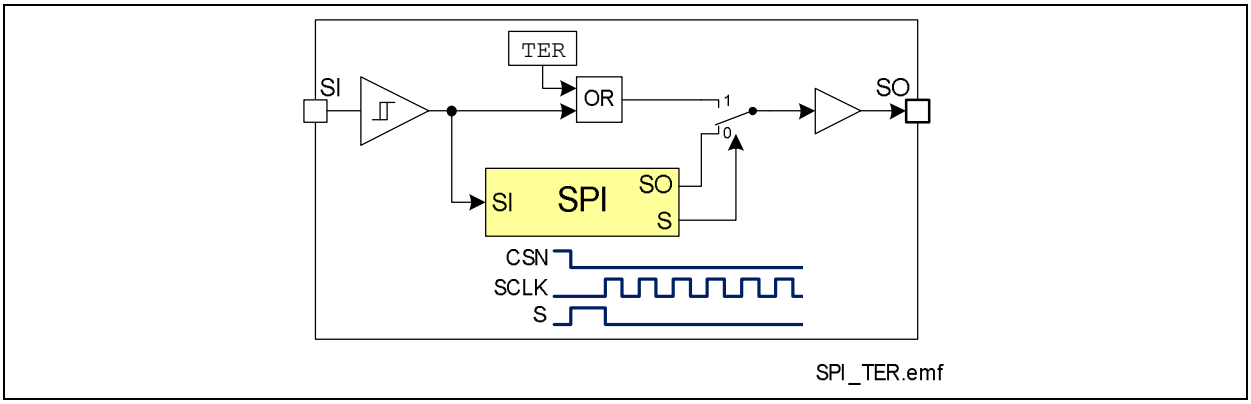


Figure 24 Combinatorial Logic for TER bit

CSN “low” to "high" Transition

- Command decoding is only done, when after the falling edge of CSN exactly a multiple (1, 2, 3, …) of eight SCLK signals have been detected after the first 16 SCLK pulses. In case of faulty transmission, the transmission error bit (**TER**) is set and the command is ignored.
- Data from shift register is transferred into the addressed register.

SCLK - Serial Clock

This input pin clocks the internal shift register. The serial input (SI) transfers data into the shift register on the falling edge of SCLK while the serial output (SO) shifts diagnostic information out on the rising edge of the serial clock. It is essential that the SCLK pin is in “low” state whenever chip select CSN makes any transition, otherwise the command may be not accepted.

SI - Serial Input

Serial input data bits are shift-in at this pin, the most significant bit first. SI information is read on the falling edge of SCLK. The input data consists of two parts, control bits followed by data bits. Please refer to **Chapter 10.5** for further information.

SO Serial Output

Data is shifted out serially at this pin, the most significant bit first. SO is in high impedance state until the CSN pin goes to “low” state. New data appears at the SO pin following the rising edge of SCLK.

Please refer to **Chapter 10.5** for further information.

10.2 Daisy Chain Capability

The SPI of TLE75004-EPD provides daisy chain capability. In this configuration several devices are activated by the same CSN signal MCSN. The SI line of one device is connected with the SO line of another device (see **Figure 25**), in order to build a chain. The end of the chain is connected to the output and input of the master device, MO and MI respectively. The master device provides the master clock MCLK which is connected to the SCLK line of each device in the chain.

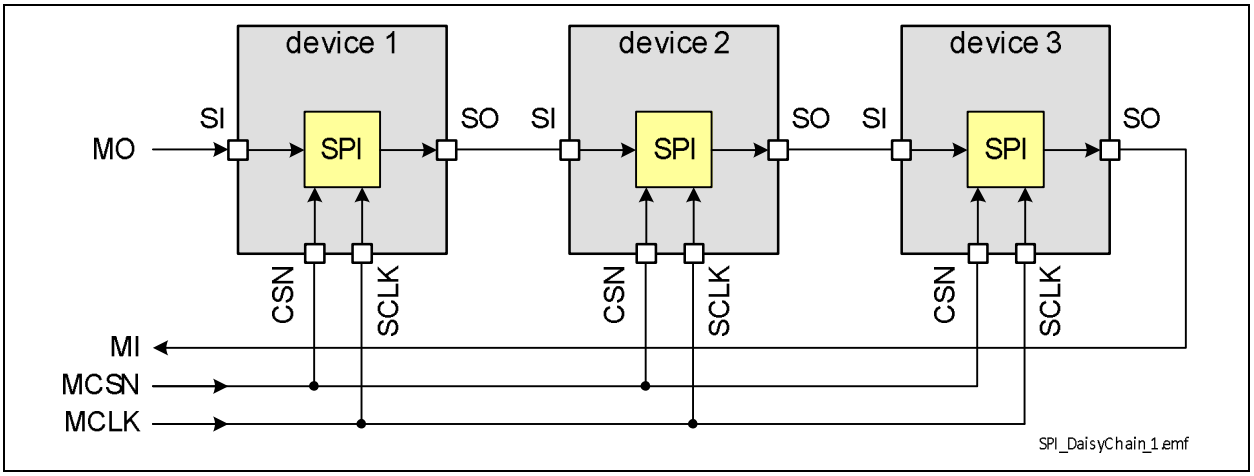


Figure 25 Daisy Chain Configuration

In the SPI block of each device, there is one shift register where each bit from SI line is shifted in each SCLK. The bit shifted out occurs at the SO pin. After sixteen SCLK cycles, the data transfer for one device is finished.

In single chip configuration, the CSN line must turn “high” to make the device acknowledge the transferred data. In daisy chain configuration, the data shifted out at device 1 has been shifted in to device 2. When using three devices in daisy chain, several multiples of 8 bits have to be shifted through the devices (depending on how many devices with 8 bit SPI and how many with 16 bit SPI). After that, the MCSN line must turn “high” (see **Figure 26**).

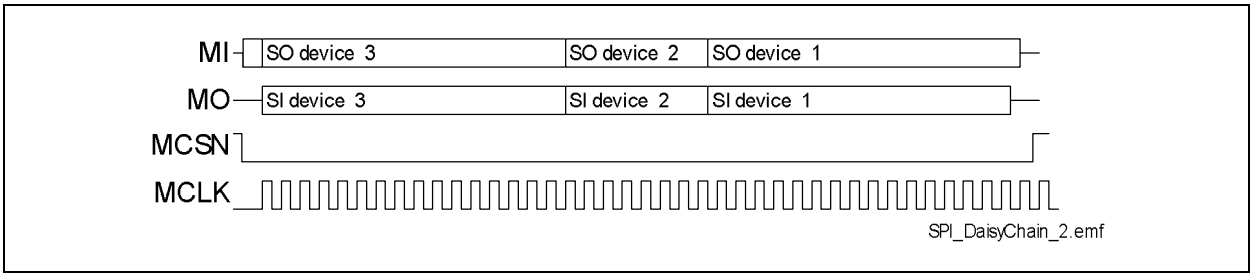


Figure 26 Data Transfer in Daisy Chain Configuration

10.3 Timing Diagrams

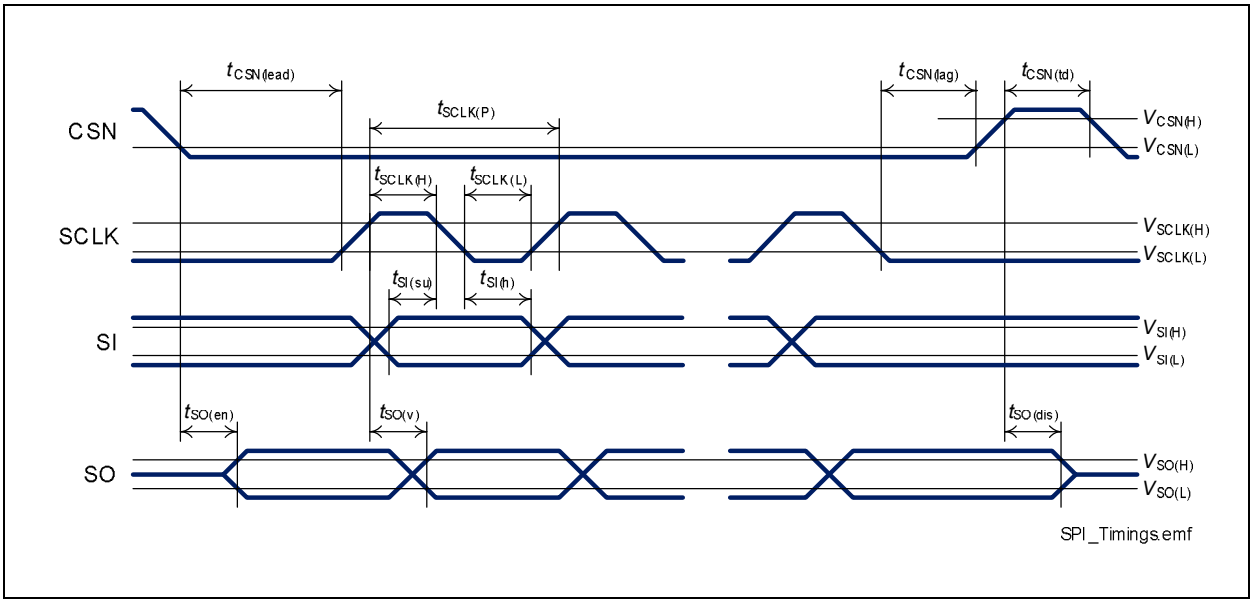


Figure 27 Timing Diagram SPI Access

10.4 Electrical Characteristics

V_{DD} = 3 V to 5.5 V, V_S = 7 V to 18 V, T_J = -40 °C to +150 °C (unless otherwise specified)
Typical values: V_{DD} = 5 V, V_S = 13.5 V, T_J = 25 °C

Table 12 Electrical Characteristics Serial Peripheral Interface (SPI)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input Characteristics (CSN, SCLK, SI) - "low" level of pin							
CSN	$V_{CSN(L)}$	0	–	0.8	V	–	P_10.4.1
SCLK	$V_{SCLK(L)}$	0	–	0.8	V	–	P_10.4.2
SI	$V_{SI(L)}$	0	–	0.8	V	–	P_10.4.3
Input Characteristics (CSN, SCLK, SI) - "high" level of pin							
CSN	$V_{CSN(H)}$	2	–	V_{DD}	V	–	P_10.4.4
SCLK	$V_{SCLK(H)}$	2	–	V_{DD}	V	–	P_10.4.5
SI	$V_{SI(H)}$	2	–	V_{DD}	V	–	P_10.4.6
Input Pull-Up Current at Pin CSN							
L-input pull-up current at CSN pin	$-I_{CSN(L)}$	30	60	90	µA	V_{DD} = 5 V V_{CSN} = 0.8 V	P_10.4.7
H-input pull-up current at CSN pin	$-I_{CSN(H)}$	20	40	65	µA	V_{DD} = 5 V V_{CSN} = 2 V	P_10.4.8
L-Input Pull-Down Current at Pin							
SCLK	$I_{SCLK(L)}$	5	12	20	µA	V_{SCLK} = 0.8 V	P_10.4.9
SI	$I_{SI(L)}$	5	12	20	µA	V_{SI} = 0.8 V	P_10.4.10
H-Input Pull-Down Current at Pin							
SCLK	$I_{SCLK(H)}$	14	28	45	µA	V_{SCLK} = 2 V	P_10.4.11
SI	$I_{SI(H)}$	14	28	45	µA	V_{SI} = 2 V	P_10.4.12
Output Characteristics (SO)							
L level output voltage	$V_{SO(L)}$	0	–	0.4	V	I_{SO} = -1.5 mA	P_10.4.13
H level output voltage	$V_{SO(H)}$	V_{DD} - 0.4	–	V_{DD}	V	I_{SO} = 1.5 mA	P_10.4.14
Output tristate leakage current	$I_{SO(OFF)}$	-1	–	1	µA	V_{CSN} =V_{DD} V_{SO} = 0 V	P_10.4.15
Output tristate leakage current	$I_{SO(OFF)}$	-1	–	1	µA	V_{CSN} =V_{DD} V_{SO} = V_{DD}	P_10.4.16
Timings							
Enable lead time (falling CSN to rising SCLK)	$t_{CSN(lead)}$	200	–	–	ns	[1] V_{DD} = 4.5 V or V_S > 7 V	P_10.4.17
Enable lag time (falling SCLK to rising CSN)	$t_{CSN(lag)}$	200	–	–	ns	[1] V_{DD} = 4.5 V or V_S > 7 V	P_10.4.18

Table 12 Electrical Characteristics Serial Peripheral Interface (SPI) (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Transfer delay time (rising CSN to falling CSN)	$t_{CSN(td)}$	250	–	–	ns	[1] V_{DD} = 4.5 V or V_S > 7 V	P_10.4.19
Output enable time (falling CSN to SO valid)	$t_{SO(en)}$	–	–	200	ns	[1] V_{DD} = 4.5 V or V_S > 7 V C_L = 20 pF at SO pin	P_10.4.20
Output disable time (rising CSN to SO tristate)	$t_{SO(dis)}$	–	–	200	ns	[1] V_{DD} = 4.5 V or V_S > 7 V C_L = 20 pF at SO pin	P_10.4.21
Serial clock frequency	f_{SCLK}	–	–	5	MHz	[1] V_{DD} = 4.5 V or V_S > 7 V	P_10.4.22
Serial clock period	$t_{SCLK(P)}$	200	–	–	ns	[1] V_{DD} = 4.5 V or V_S > 7 V	P_10.4.23
Serial clock "high" time	$t_{SCLK(H)}$	75	–	–	ns	[1] V_{DD} = 4.5 V or V_S > 7 V	P_10.4.24
Serial clock "low" time	$t_{SCLK(L)}$	75	–	–	ns	[1] V_{DD} = 4.5 V or V_S > 7 V	P_10.4.25
Data setup time (required time SI to falling SCLK)	$t_{SI(su)}$	20	–	–	ns	[1] V_{DD} = 4.5 V or V_S > 7 V	P_10.4.26
Data hold time (falling SCLK to SI)	$t_{SI(h)}$	20	–	–	ns	[1] V_{DD} = 4.5 V or V_S > 7 V	P_10.4.27
Output data valid time with capacitive load	$t_{SO(v)}$	–	–	100	ns	[1] V_{DD} = 4.5 V or V_S > 7 V C_L = 20 pF at SO pin	P_10.4.28
Enable lead time (falling CSN to rising SCLK)	$t_{CSN(lead)}$	1	–	–	µs	[1] V_{DD} = V_S = 3.0 V	P_10.4.29
Enable lag time (falling SCLK to rising CSN)	$t_{CSN(lag)}$	1	–	–	µs	[1] V_{DD} = V_S = 3.0 V	P_10.4.30
Transfer delay time (rising CSN to falling CSN)	$t_{CSN(td)}$	1.25	–	–	µs	[1] V_{DD} = V_S = 3.0 V	P_10.4.31

Table 12 Electrical Characteristics Serial Peripheral Interface (SPI) (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output enable time (falling CSN to SO valid)	$t_{SO(en)}$	–	–	1	µs	[1] $V_{DD} = V_S = 3.0$ V $C_L = 20$ pF at SO pin	P_10.4.32
Output disable time (rising CSN to SO tristate)	$t_{SO(dis)}$	–	–	1	µs	[1] $V_{DD} = V_S = 3.0$ V $C_L = 20$ pF at SO pin	P_10.4.33
Serial clock frequency	f_{SCLK}	–	–	1	MHz	[1] $V_{DD} = V_S = 3.0$ V	P_10.4.34
Serial clock period	$t_{SCLK(P)}$	1	–	–	µs	[1] $V_{DD} = V_S = 3.0$ V	P_10.4.35
Serial clock "high" time	$t_{SCLK(H)}$	375	–	–	ns	[1] $V_{DD} = V_S = 3.0$ V	P_10.4.36
Serial clock "low" time	$t_{SCLK(L)}$	375	–	–	ns	[1] $V_{DD} = V_S = 3.0$ V	P_10.4.37
Data setup time (required time SI to falling SCLK)	$t_{SI(su)}$	100	–	–	ns	[1] $V_{DD} = V_S = 3.0$ V	P_10.4.38
Data hold time (falling SCLK to SI)	$t_{SI(h)}$	100	–	–	ns	[1] $V_{DD} = V_S = 3.0$ V	P_10.4.39
Output data valid time with capacitive load	$t_{SO(v)}$	–	–	500	ns	[1] $V_{DD} = V_S = 3.0$ V $C_L = 20$ pF at SO pin	P_10.4.40

1) Not subject to production test, specified by design

10.5 SPI Protocol

The relationship between SI and SO content during SPI communication is shown in **Figure 28**. SI line represents the frame sent from the µC and SO line is the answer provided by TLE75004-EPD.

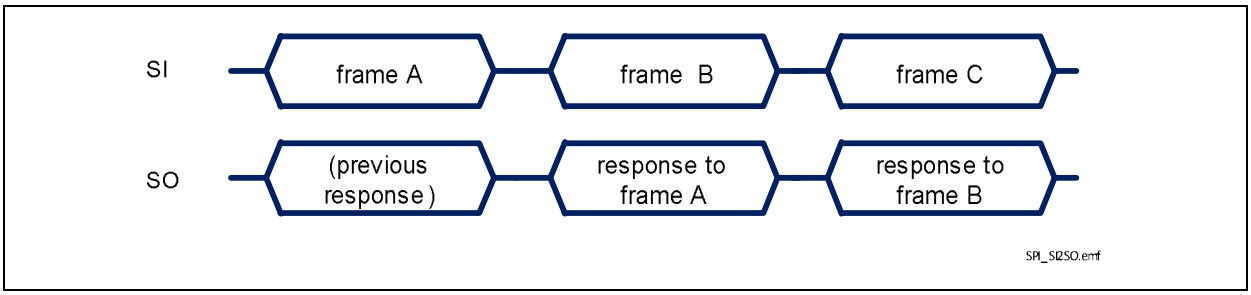


Figure 28 Relationship between SI and SO during SPI communication

The SPI protocol provides the answer to a command frame only with the next transmission triggered by the µC. Although the biggest majority of commands and frames implemented in TLE75004-EPD can be decoded without the knowledge of what happened before, it is advisable to consider what the µC sent in the previous transmission to decode TLE75004-EPD response frame completely.

More in detail, the sequence of commands to “read” and “write” the content of a register looks as follows:

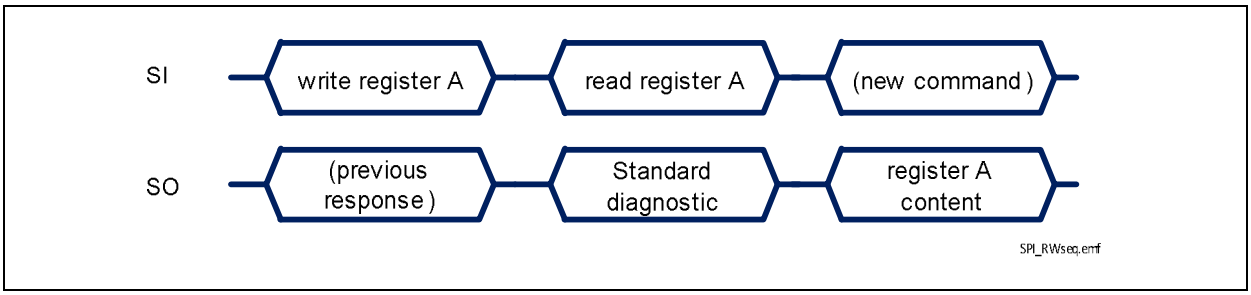


Figure 29 Register content sent back to µC

There are 3 special situations where the frame sent back to the µC is not related directly to the previous received frame:

- in case an error in transmission happened during the previous frame (for instance, the clock pulses were not multiple of 8 with a minimum of 16 bits), shown in **Figure 30**
- when TLE75004-EPD logic supply comes out of Power-On reset condition or after a Software Reset, as shown in **Figure 31**
- in case of command syntax errors
  - “write” command starting with “11” instead of “10”
  - “read” command starting with “00” instead of “01”
  - “read” or “write” commands on registers which are “reserved” or “not used”

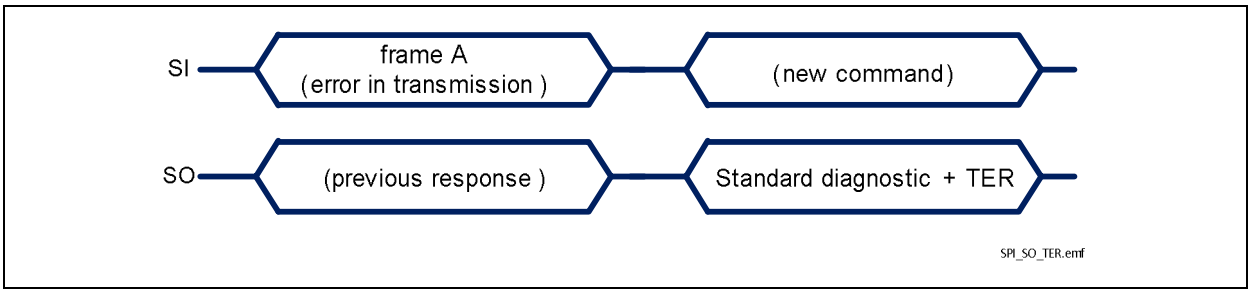


Figure 30 TLE75004-EPD response after a error in transmission

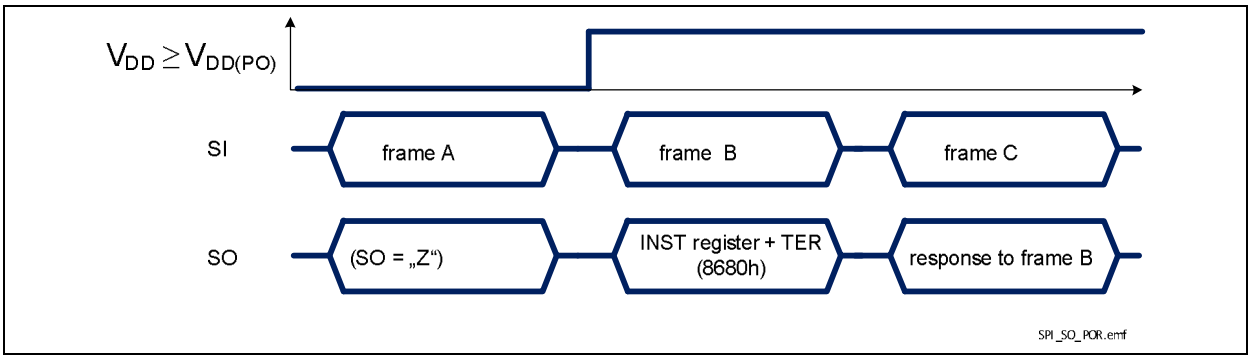


Figure 31 TLE75004-EPD response after coming out of Power-On reset at V_{DD}

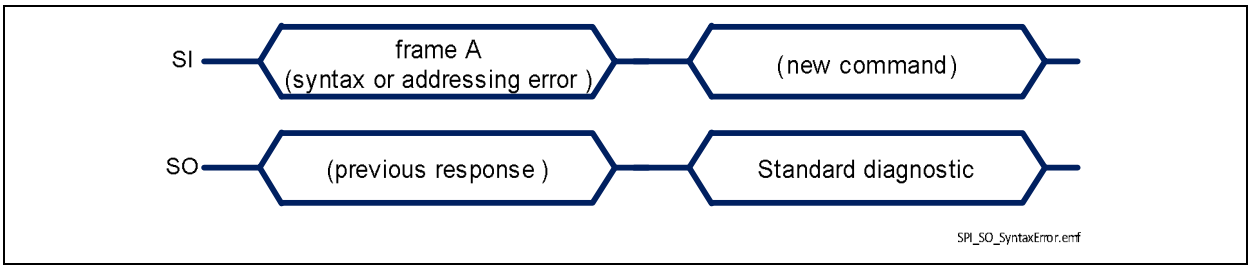


Figure 32 TLE75004-EPD response after a command syntax error

A summary of all possible SPI commands is presented in **Table 13**, including the answer that TLE75004-EPD sends back at the next transmission.

Table 13 SPI Command summary[1)]

Requested Operation	Frame sent to SPIDER+ (SI pin)	Frame received from SPIDER+ (SO pin) with the next command
Read Standard Diagnosis	$0xxxxxxxxxxxxx01_B$ (“$xxxxxxxxxxxxx_B$” = don´t care)	$0ddddddddddddddd_B$ (Standard Diagnosis)
Write 8 bit register	$10aaaabbcccccccc_B$ where: “$aaaa_B$” = register address ADDR0 “bb_B” = register address ADDR1 “$cccccccc_B$” = new register content	$0ddddddddddddddd_B$ (Standard Diagnosis)
Read 8 bit registers	$01aaaabbxxxxxx10_B$ where: “$aaaa_B$” = register address ADDR0 “bb_B” = register address ADDR1 “$xxxxxx_B$” = don´t care	$10aaaabbcccccccc_B$ where: “$aaaa_B$” = register address ADDR0 “bb_B” = register address ADDR1 “$cccccccc_B$” = register content

1) “a” = address bits for ADDR0 field, “b” = address bit for ADDR1 field, “c” = register content, “d” = diagnostic bit

10.6 SPI Registers Overview

10.6.1 Standard Diagnosis

Table 14 Standard Diagnosis

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0	UVRVS	LOPVDD	MODE		TER	0	OLOFF	0	0	0	0	ERR				7800_H

Field	Bits	Type	Description
UVRVS	14	r	**V_S Undervoltage Monitor** 0_B No undervoltage condition on V_S detected (see **Chapter 6.2.1** for more details) 1_B (default) There was at least one V_S Undervoltage condition since last Standard Diagnosis readout
LOPVDD	13	r	**V_{DD} Lower Operating Range Monitor** 0_B V_{DD} is above $V_{DD(LOP)}$ 1_B (default) There was at least one "$V_{DD} = V_{DD(LOP)}$" condition since last Standard Diagnosis readout
MODE	12:11	r	**Operative Mode Monitor** 00_B (reserved) 01_B Limp Home Mode 10_B Active Mode 11_B (default) Idle Mode
TER	10	r	**Transmission Error** 0_B Previous transmission was successful (modulo 16 + n*8 clocks received, where n = 0, 1, 2...) 1_B (default) Previous transmission failed The first frame after a reset is **TER** set to "high" and the **INST** register. The second frame is the Standard Diagnosis with **TER** set to "low" (if there was no fail in the previous transmission).
OLOFF	8	r	**Open Load in OFF Diagnosis** 0_B (default) All channels in OFF state (which have **DIAG_IOL.OUTn** bit set to "1") have $V_{DS} > V_{DS(OL)}$ 1_B At least one channel in OFF state (with **DIAG_IOL.OUTn** bit set to "1") has $V_{DS} < V_{DS(OL)}$ Channels in ON state are not considered
ERRn n = 3 to 0	n:0	r	**Over Load / Over Temperature Diagnosis of channel n** 0_B (default) No failure detected 1_B Over Temperature or Over Load bits 7:4 - reserved (default: 0_B)

10.6.2 Register structure

The register banks the digital part have following structure:

Table 15 Register structure - all registers

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
r = 0 w = 1	r = 1 w = 0	ADDR0				ADDR1		DATA								$XXXX_H$

Table 16 summarizes the available registers with their addresing space and size

Table 16 Register addressing space

Register name	ADDR0	ADDR1	Size	Type	Purpose
OUT n = 3 to 0	0000_B	00_B	n	r/w	**Power output control register** bits OUT.OUTn 0_B (default) Output is OFF 1_B Output is ON bits 7:4 - reserved (read default: 0_B, write ignored)
MAPIN0 n = 3 to 0	0001_B	00_B	n	r/w	**Input Mapping (Input Pin 0)** bits MAPIN0.OUTn 0_B (default) The output is not connected to the input pin 1_B The output is connected to the input pin Note: Channel 2 has the corresponding bit set to “1” by default bits 7:4 - reserved (read default: 0_B, write ignored)
MAPIN1 n = 3 to 0	0001_B	01_B	n	r/w	**Input Mapping (Input Pin 1)** bits MAPIN1.OUTn 0_B (default) The output is not connected to the input pin 1_B The output is connected to the input pin Note: Channel 3 has the corresponding bit set to “1” by default bits 7:4 - reserved (read default: 0_B, write ignored)
INST	0001_B	10_B	8	r	**Input Status Monitor** bit TER 0_B Previous transmission was successful (modulo 16 + n*8 clocks received, where n = 0, 1, 2...) 1_B (default) Previous transmission failed bits INST.RES (6:2) - reserved bits INST.INn (1:0) 0_B (default) The input pin is set to “low” 1_B The input pin is set to “high” First register transmitted after a reset of the logic

Table 16 Register addressing space (cont'd)

Register name	ADDR0	ADDR1	Size	Type	Purpose
DIAG_IOL n = 3 to 0	0010_B	00_B	n	r/w	**Open Load diagnostic current control** bits DIAG_IOL.OUTn 0_B (default) Diagnosis current not enabled 1_B Diagnosis current enabled bits 7:4 - reserved (read default: 0_B, write ignored)
DIAG_OSM n = 3 to 0	0010_B	01_B	n	r	**Output Status Monitor** bits DIAG_OSM.OUTn 0_B (default) $V_{DS} > V_{DS(OL)}$ 1_B $V_{DS} < V_{DS(OL)}$ bits 7:4 - reserved (default: 0_B)
HWCR	0011_B	00_B	8	r/w	**Hardware Configuration Register** bit HWCR.ACT (7) (Active Mode) 0_B (default) Normal operation or device leaves Active Mode 1_B Device enters Active Mode (see **Chapter 6.1** for a description of the possible operative mode transitions) bit HWCR.RST (6) (Reset) 0_B (default) Normal operation 1_B Execute Reset command (self clearing) bits HWCR.PAR (1:0) (channels operating in parallel) 0_B (default) Normal operation 1_B two neighbour channels have Over Load and Over Temperature synchronized (see **Chapter 7.2** for more details) bits 5:2 - reserved (read default: 0_B, write ignored)
HWCR_OCL n = 3 to 0	0011_B	01_B	n	w	**Output Clear Latch** bits HWCR_OCL.OUTn 0_B (default) Normal operation 1_B Clear the error latch for the selected output bits 7:4 - reserved (default: 0_B, write ignored)

10.6.3 Register summary

All registers with addresses not mentioned in **Table 17** have to be considered as "reserved". "Read" operations performed on those registers return the Standard Diagnosis. The column "Default" indicates the content of the register (8 bits) after a reset.

Table 17 Addressable registers

15	14	13-10	9	8	7	6	5	4	3	2	1	0	Default
r = 0 w = 1	r = 1 w = 0	0000	00		(reserved)				**OUT.OUTn**				00_H
r = 0 w = 1	r = 1 w = 0	0001	00		(reserved)				**MAPIN0.OUTn**				04_H

Table 17 Addressable registers

15	14	13-10	9	8	7	6	5	4	3	2	1	0	Default
r = 0 w = 1	r = 1 w = 0	0001	01		(reserved)				**MAPIN1.OUTn**				08_H
0	1	0001	10		**TER**	(reserved)					**INST.INn**		00_H
r = 0 w = 1	r = 1 w = 0	0010	00		(reserved)				**DIAG_IOL.OUTn**				00_H
0	1	0010	01		(reserved)				**DIAG_OSM.OUTn**				00_H
r = 0 w = 1	r = 1 w = 0	0011	00		**HWCR.ACT**	**HWCR.RST**	(reserved)				**HWCR.PAR**		00_H
r = 0 w = 1	r = 1 w = 0	0011	01		(reserved)				**HWCR_OCL.OUTn**				00_H

10.6.4 SPI command quick list

A summary of the most used SPI commands (read and write operations on all registers) is shown in **Table 18**

Table 18 SPI command quick list

Register	“read” command”	“write” command	content written
OUT	4002_H	$80XX_H$	XX_H = xxxxxxxx$_B$
MAPIN0	4402_H	$84XX_H$	XX_H = xxxxxxxx$_B$
MAPIN1	4502_H	$85XX_H$	XX_H = xxxxxxxx$_B$
INST	4602_H	n.a. (read-only)	–
DIAG_IOL	4802_H	$88XX_H$	XX_H = xxxxxxxx$_B$
DIAG_OSM	4902_H	n.a. (read-only)	–
HWCR	$4C02_H$	$8CXX_H$	XX_H = xxxxxxxx$_B$
HWCR_OCL	$4D02_H$	$8DXX_H$	XX_H = xxxxxxxx$_B$

11 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

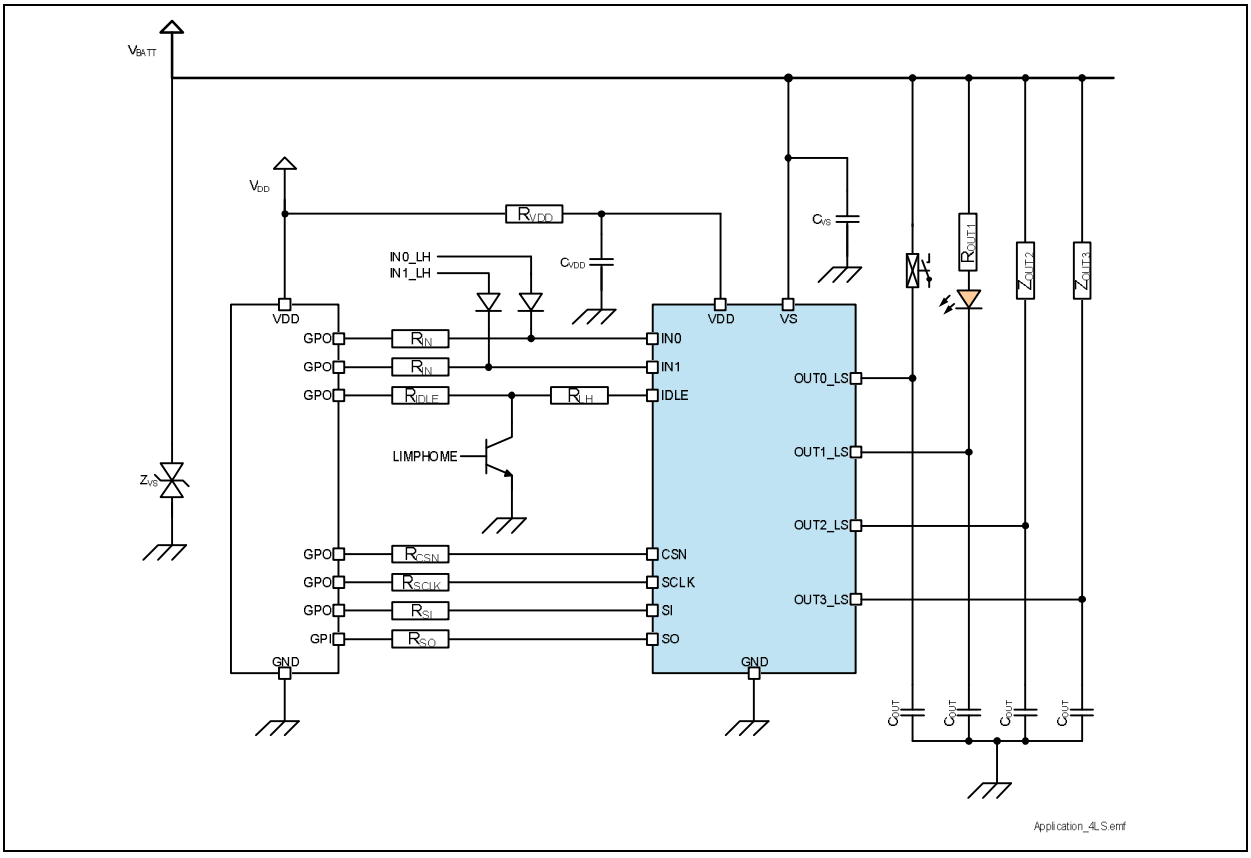


Figure 33 TLE75004-EPD Application Diagram

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

Table 19 Suggested Component values

Reference	Value	Purpose
R_{IN}	4.7 kΩ	Protection of the micro-controller during Over Voltage and Reverse Polarity Guarantee TLE75004-EPD channels OFF during Loss of Ground
R_{IDLE}	4.7 kΩ	Protection of the micro-controller during Over Voltage and Reverse Polarity Guarantee TLE75004-EPD channels OFF during Loss of Ground
R_{CSN}	500 Ω	Protection of the micro-controller during Over Voltage and Reverse Polarity
R_{SCLK}	500 Ω	Protection of the micro-controller during Over Voltage and Reverse Polarity
R_{SI}	500 Ω	Protection of the micro-controller during Over Voltage and Reverse Polarity
R_{SO}	500 Ω	Protection of the micro-controller during Over Voltage and Reverse Polarity
R_{VDD}	100 Ω	Logic supply voltage spikes filtering

Table 19 Suggested Component values (cont'd)

Reference	Value	Purpose
C_{VDD}	100 nF	Logic supply voltage spikes filtering
C_{VS}	68 nF	Analog supply voltage spikes filtering
Z_{VS}	P6SMB30	Protection of device during Over Voltage. Zener diode
C_{OUT}	10 nF	Protection of TLE75004-EPD against ESD and BCI

11.1 Further Application Information

- Please contact us for information regarding the Pin FMEA
- For further information you may contact **http://www.infineon.com/**

12 Package Outlines

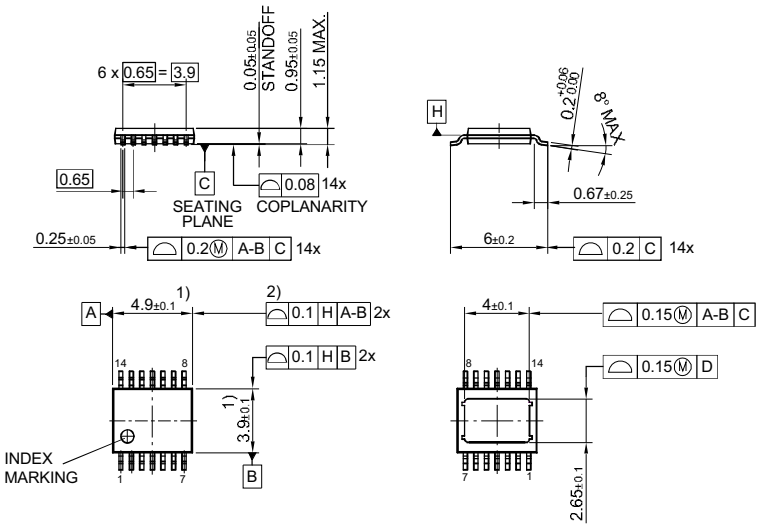


Figure 34 PG-TSDSO-14 Package drawing

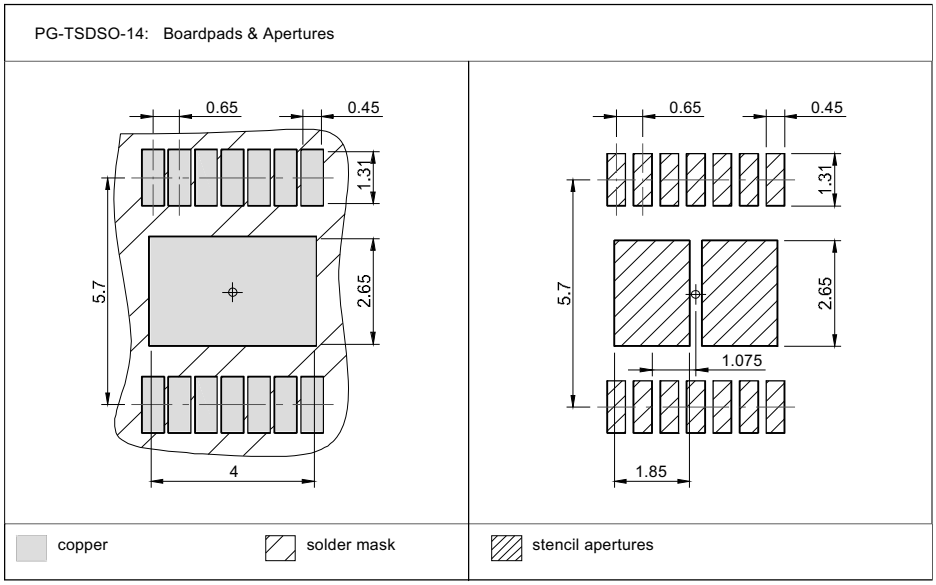


Figure 35 TLE75004-EPD Package pads and stencil

Package Outlines

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

13 Revision History

Page or Item	Changes since previous revision
Rev. 1.10, 2020-09-02	
All	Package name updated
Table 2	Updated ESD susceptibility footnotes for HBM and CDM
	Updated backcover
Rev.1.00, 2017-11-23	
All	Datasheet released
TLE75004-EPD	

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PCN 2021-106-A

Several changes affecting products TLE75x

Affected products sold to FUTURE ELECTRONICS LTD. (4049887)

Sales name	SP number	OPN	Package	Customer part number
TLE75080-ESH	SP001635024	TLE75080ESHXUMA1	PG-TSDSO-24-21	TLE75080ESHXUMA1
TLE75602-ESH	SP001635032	TLE75602ESHXUMA1	PG-TSDSO-24-21	TLE75602ESHXUMA1