



Product Change Notification / SYST-23PDIB871

Date:

28-Jun-2022

Product Category:

32-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ERRATA - SAM E70/S70/V70/V71 Family Silicon Errata and Data Sheet Clarification Revision

Affected CPNs:

[SYST-23PDIB871_Affected_CPN_06282022.pdf](#)

[SYST-23PDIB871_Affected_CPN_06282022.csv](#)

Notification Text:

SYST-23PDIB871

Microchip has released a new Errata for the SAM E70/S70/V70/V71 Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at [SAM E70/S70/V70/V71 Family Silicon Errata and Data Sheet Clarification](#).

Notification Status: Final

Description of Change: Revision L (06/2022) The following silicon errata were added in this revision: • USART: 2.19.3 LIN Bit The following errata were updated with new verbiage: • SDRAMC: 2.14.4 SDRAM Support

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 24 Jun 2022

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Please contact your local [Microchip sales office](#) with questions or concerns regarding this notification.

Terms and Conditions:

If you wish to [receive Microchip PCNs via email](#) please register for our PCN email service at our [PCN home page](#) select register then fill in the required fields. You will find instructions about registering for Microchips PCN email service in the [PCN FAQ](#) section.

If you wish to [change your PCN profile, including opt out](#), please go to the [PCN home page](#) select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.

SYST-23PDIB871 - ERRATA - SAM E70/S70/V70/V71 Family Silicon Errata and Data Sheet Clarification Revisio

Affected Catalog Part Numbers(CPN)

ATSAMS70Q20A-CN
ATSAMS70Q21A-CN
ATSAME70Q21A-CN
ATSAME70Q20A-CN
ATSAME70Q19A-CN
ATSAMS70Q19A-CN
ATSAME70N21A-CN
ATSAMS70N21A-CN
ATSAME70N20A-CN
ATSAME70N19A-CN
ATSAMS70N20A-CN
ATSAMS70N19A-CN
ATSAMS70N21A-CFN
ATSAMS70N20A-CFN
ATSAMS70N19A-CFN
ATSAME70Q20A-CFN
ATSAME70Q21A-CFN
ATSAMS70Q19A-CFN
ATSAME70Q19A-CFN
ATSAMS70Q20A-CFN
ATSAMS70Q21A-CFN
ATSAMS70N20A-AN
ATSAMS70N19A-AN
ATSAMS70N21A-AN
ATSAME70N21A-AN
ATSAME70N20A-AN
ATSAME70N19A-AN
ATSAMS70Q20A-AN
ATSAMS70Q21A-AN
ATSAME70Q20A-AN
ATSAME70Q19A-AN
ATSAMS70Q19A-AN
ATSAME70Q21A-AN
ATSAMS70J20A-MN
ATSAMS70J21A-MN
ATSAMS70J19A-MN
ATSAME70J21A-AN
ATSAMS70J21A-AN
ATSAME70J20A-AN
ATSAME70J19A-AN
ATSAMS70J19A-AN
ATSAMS70J20A-AN

ATSAMS70Q20A-CNT
ATSAMS70Q21A-CNT
ATSAME70Q21A-CNT
ATSAME70Q20A-CNT
ATSAME70Q19A-CNT
ATSAMS70Q19A-CNT
ATSAME70N21A-CNT
ATSAMS70N21A-CNT
ATSAME70N19A-CNT
ATSAMS70N20A-CNT
ATSAMS70N19A-CNT
ATSAME70N20A-CNT
ATSAMV70N20A-CBT
ATSAMS70N21A-CFNT
ATSAMS70N19A-CFNT
ATSAMS70N20A-CFNT
ATSAMS70Q21A-CFNT
ATSAMS70Q20A-CFNT
ATSAMS70Q19A-CFNT
ATSAME70Q21A-CFNT
ATSAME70Q20A-CFNT
ATSAME70Q19A-CFNT
ATSAMS70N20A-ANT
ATSAMS70N19A-ANT
ATSAMS70N21A-ANT
ATSAME70N21A-ANT
ATSAME70N20A-ANT
ATSAME70N19A-ANT
ATSAMS70Q20A-ANT
ATSAMS70Q21A-ANT
ATSAME70Q21A-ANT
ATSAME70Q20A-ANT
ATSAME70Q19A-ANT
ATSAMS70Q19A-ANT
ATSAMS70J21A-MNT
ATSAMS70J20A-MNT
ATSAMS70J19A-MNT
ATSAME70J21A-ANT
ATSAMS70J21A-ANT
ATSAME70J20A-ANT
ATSAMS70J20A-ANT
ATSAME70J19A-ANT
ATSAMS70J19A-ANT
ATSAMV71Q21B-AAB
ATSAMV70Q19B-AAB
ATSAMV70Q20B-AAB
ATSAMV71Q19B-AAB

ATSAMV71Q20B-AAB
ATSAMV70Q20B-AABV10
ATSAMV71Q20B-AABV17
ATSAMV71Q21B-AABV19
ATSAME70Q21B-CN
ATSAME70Q20B-CN
ATSAMS70Q20B-CN
ATSAMS70Q21B-CN
ATSAMV71Q21B-CB
ATSAMV70Q19B-CB
ATSAMV70Q20B-CB
ATSAMV71Q20B-CB
ATSAMV71Q19B-CB
ATSAMV70Q20B-CBVAO
ATSAMV71Q20B-CBVAO
ATSAME70N19B-CN
ATSAME70N20B-CN
ATSAMV71N21B-CB
ATSAMV70N20B-CB
ATSAMV71N20B-CB
ATSAMV71N19B-CB
ATSAMV70N19B-CB
ATSAME70N21B-CN
ATSAMS70N20B-CN
ATSAMS70N21B-CN
ATSAMV71N21B-CBV06
ATSAMV71N21B-CBV11
ATSAMV70N20B-CBVAO
ATSAMS70N20B-CFN
ATSAMS70N21B-CFN
ATSAME70Q21B-CFN
ATSAME70Q20B-CFN
ATSAMS70Q21B-CFN
ATSAMS70Q20B-CFN
ATSAME70N20B-AN
ATSAMV71N20B-AAB
ATSAMV71N19B-AAB
ATSAMV70N19B-AAB
ATSAMV71N21B-AAB
ATSAMV70N20B-AAB
ATSAME70N21B-AN
ATSAMS70N20B-AN
ATSAMS70N21B-AN
ATSAMV71N20B-AABV14
ATSAMV70N20B-AABVAO
ATSAME70Q21B-AN
ATSAMV71Q21B-AABT

ATSAMV70Q19B-AABT
ATSAMV70Q20B-AABT
ATSAMV71Q19B-AABT
ATSAMV71Q20B-AABT
ATSAME70Q20B-AN
ATSAMS70Q20B-AN
ATSAMS70Q21B-AN
ATSAMS70J21B-MN
ATSAMS70J20B-MN
ATSAME70J20B-AN
ATSAMV71J21B-AAB
ATSAMV70J20B-AAB
ATSAME70J21B-AN
ATSAMV71J21B-AABT
ATSAMS70J20B-AN
ATSAMV70J19B-AAB
ATSAMV71J20B-AAB
ATSAMS70J21B-AN
ATSAMV71J19B-AAB
ATSAMV70Q19B-AABTV07
ATSAMV70Q20B-AABTV10
ATSAMV71Q21B-AABTV13
ATSAMV71Q20B-AABTV17
ATSAMV71Q21B-AABTV19
ATSAMV71J21B-AABTV16
ATSAMV71J21B-AABTV18
ATSAMV71J21B-AABTVAO
ATSAME70Q20B-CNT
ATSAMS70Q20B-CNT
ATSAME70Q21B-CNT
ATSAMS70Q21B-CNT
ATSAMV70Q19B-CBT
ATSAMV71Q20B-CBT
ATSAMV71Q19B-CBT
ATSAMV70Q20B-CBT
ATSAMV71Q21B-CBT
ATSAMV70Q19B-CBTV01
ATSAMV71Q21B-CBTV05
ATSAMV70Q20B-CBTV23
ATSAMV70Q20B-CBTVAO
ATSAMV70Q19B-CBTVAO
ATSAME70N19B-CNT
ATSAME70N20B-CNT
ATSAMV71N21B-CBT
ATSAMV70N20B-CBT
ATSAMV71N20B-CBT
ATSAMV70N19B-CBT

ATSAMV71N19B-CBT
ATSAMS70N20B-CNT
ATSAME70N21B-CNT
ATSAMS70N21B-CNT
ATSAMV71N21B-CBTV02
ATSAMV71N20B-CBTV03
ATSAMV70N20B-CBTV08
ATSAMV71N21B-CBTV09
ATSAMV70N20B-CBTV12
ATSAMV71N21B-CBTV15
ATSAMV70N20B-CBTVAO
ATSAMS70N20B-CFNT
ATSAMS70N21B-CFNT
ATSAME70Q20B-CFNT
ATSAMS70Q20B-CFNT
ATSAME70Q21B-CFNT
ATSAMS70Q21B-CFNT
ATSAME70N20B-ANT
ATSAMV71N20B-AABT
ATSAMV71N19B-AABT
ATSAMV70N19B-AABT
ATSAMV71N21B-AABT
ATSAMV70N20B-AABT
ATSAMS70N20B-ANT
ATSAME70N21B-ANT
ATSAMS70N21B-ANT
ATSAMV71N19B-AABTV04
ATSAMV71N21B-AABTV20
ATSAMV70N20B-AABTV22
ATSAMV71N20B-AABTVAO
ATSAMV70N20B-AABTVAO
ATSAME70Q20B-ANT
ATSAMS70Q20B-ANT
ATSAME70Q21B-ANT
ATSAMS70Q21B-ANT
ATSAMS70J21B-MNT
ATSAMS70J20B-MNT
ATSAME70J20B-ANT
ATSAMV70J19B-AABT
ATSAMS70J20B-ANT
ATSAME70J21B-ANT
ATSAMV70J20B-AABT
ATSAMV71J20B-AABT
ATSAMS70J21B-ANT
ATSAMV71J19B-AABT
ATSAMS70Q19B-CN
ATSAME70Q19B-CN

ATSAMV70Q19B-CBV02
ATSAMS70N19B-CN
ATSAMS70N19B-CFN
ATSAME70Q19B-CFN
ATSAMS70Q19B-CFN
ATSAME70N19B-AN
ATSAMS70N19B-AN
ATSAME70Q19B-AN
ATSAMS70Q19B-AN
ATSAMS70J19B-MN
ATSAME70J19B-AN
ATSAMS70J19B-AN
ATSAMS70Q19B-CNT
ATSAME70Q19B-CNT
ATSAMV70Q19B-CBTV02
ATSAMV70Q19B-CBTV03
ATSAMS70N19B-CNT
ATSAMS70N19B-CFNT
ATSAME70Q19B-CFNT
ATSAMS70Q19B-CFNT
ATSAME70N19B-ANT
ATSAMS70N19B-ANT
ATSAMV71N19B-AABTV01
ATSAME70Q19B-ANT
ATSAMS70Q19B-ANT
ATSAME70J19B-ANT
ATSAMS70J19B-ANT



SAM E70/S70/V70/V71 Family

SAM E70/S70/V70/V71 Family Silicon Errata and Data Sheet Clarification

SAM E70/S70/V70/V71 Family

The SAM E70/S70/V70/V71 family of devices that you have received conform functionally to the current Device Data Sheet (DS60001527G), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the following tables. The silicon issues are summarized in [Silicon Issue Summary](#).

The errata described in this document will be addressed in future revisions of the SAM E70/S70/V70/V71 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Data Sheet clarifications and corrections (if applicable) are located in [Data Sheet Clarifications](#), following the discussion of silicon issues.

Table 1. SAM E70 Family Silicon Device Identification

Devices	Device Identification		Revision (CHIPID_CIDR.VERSION[4:0])	
	CHIPID_CIDR[31:0]	CHIPID_EXID[31:0]	A	B
SAME70Q19	0xA10D_0A0x	0x00000002	0x0	0x1
SAME70Q20	0xA102_0C0x	0x00000002		
SAME70Q21	0xA102_0E0x	0x00000002		
SAME70N19	0xA10D_0A0x	0x00000001		
SAME70N20	0xA102_0C0x	0x00000001		
SAME70N21	0xA102_0E0x	0x00000001		
SAME70J19	0xA10D_0A0x	0x00000000		
SAME70J20	0xA102_0C0x	0x00000000		
SAME70J21	0xA102_0E0x	0x00000000		

Table 2. SAM S70 Family Silicon Device Identification

Devices	Device Identification		Revision (CHIPID_CIDR.VERSION[4:0])	
	CHIPID_CIDR[31:0]	CHIPID_EXID[31:0]	A	B
SAMS70Q19	0xA11D_0A0x	0x00000002	0x0	0x1
SAMS70Q20	0xA112_0C0x	0x00000002		
SAMS70Q21	0xA112_0E0x	0x00000002		
SAMS70N19	0xA11D_0A0x	0x00000001		
SAMS70N20	0xA112_0C0x	0x00000001		
SAMS70N21	0xA112_0E0x	0x00000001		
SAMS70J19	0xA11D_0A0x	0x00000000		
SAMS70J20	0xA112_0C0x	0x00000000		
SAMS70J21	0xA112_0E0x	0x00000000		

Table 3. SAM V70 Family Silicon Device Identification

Devices	Device Identification		Revision (CHIPID_CIDR.VERSION[4:0])	
	CHIPID_CIDR[31:0]	CHIPID_EXID[31:0]	A	B
SAMV70Q19	0xA13D_0A0x	0x00000002	0x0	0x1
SAMV70Q20	0xA132_0C0x	0x00000002		
SAMV70N19	0xA13D_0A0x	0x00000001		
SAMV70N20	0xA132_0C0x	0x00000001		
SAMV70J19	0xA13D_0A0x	0x00000000		
SAMV70J20	0xA132_0C0x	0x00000000		

Table 4. SAM V71 Family Silicon Device Identification

Devices	Device Identification		Revision (CHIPID_CIDR.VERSION[4:0])	
	CHIPID_CIDR[31:0]	CHIPID_EXID[31:0]	A	B
SAMV71Q19	0xA12D_0A0x	0x00000002	0x0	0x1
SAMV71Q20	0xA122_0C0x	0x00000002		
SAMV71Q21	0xA122_0E0x	0x00000002		
SAMV71N19	0xA12D_0A0x	0x00000001		
SAMV71N20	0xA122_0C0x	0x00000001		
SAMV71N21	0xA122_0E0x	0x00000001		
SAMV71J19	0xA12D_0A0x	0x00000000		
SAMV71J20	0xA122_0C0x	0x00000000		
SAMV71J21	0xA122_0E0x	0x00000000		

Note:

1. Refer to the “Chip Identifier (CHIPID)” section in the current Device Data Sheet (DS60001527G) for detailed information on Chip Identification and Revision IDs for your specific device.

Table of Contents

SAM E70/S70/V70/V71 Family.....	1
1. Silicon Errata Summary.....	5
2. SAM E70/S70/V70/V71 Errata Issues	8
2.1. Analog Front-End Controller (AFEC).....	8
2.2. Arm® Cortex®-M7.....	9
2.3. Boundary Scan Mode.....	9
2.4. Device.....	9
2.5. Extended DMA Controller (XDMAC).....	10
2.6. Fast Flash Programming Interface (FFPI).....	11
2.7. Ethernet MAC (GMAC).....	11
2.8. Inter-IC Sound Controller (I2SC).....	12
2.9. Controller Area Network (MCAN).....	12
2.10. Parallel Input/Output (PIO).....	15
2.11. Power Management Controller (PMC).....	15
2.12. Quad Serial Peripheral Interface (QSPI).....	16
2.13. Real-Time Clock (RTC).....	16
2.14. SDRAM Controller (SDRAMC).....	17
2.15. Static Memory Controller (SMC).....	17
2.16. Serial Synchronous Controller (SSC).....	17
2.17. Supply Controller (SUPC).....	18
2.18. TWI High-Speed (TWIHS).....	19
2.19. Universal Synchronous Asynchronous Receiver Transmitter (USART).....	19
2.20. USB High-Speed (USBHS).....	20
2.21. Digital-to-Analog Converter Controller (DACC).....	21
2.22. Reset Controller (RSTC).....	21
2.23. Image Sensor Interface (ISI).....	22
3. Data Sheet Clarifications.....	23
3.1. Controller Area Network (MCAN).....	23
4. Appendix A: Revision History.....	24
The Microchip Web Site.....	26
Customer Change Notification Service.....	26
Customer Support.....	26
Microchip Devices Code Protection Feature.....	26
Legal Notice.....	27
Trademarks.....	27
Quality Management System Certified by DNV.....	27
Worldwide Sales and Service.....	28

SAM E70/S70/V70/V71 Family

Silicon Errata Summary

1. Silicon Errata Summary

Table 1-1. Silicon Errata Summary

Module	Feature	Errata Number	Summary	Affected Silicon Revisions	
				A	B
AFEC	Write Protection	2.1.1	The AFEC Channel Selection (AFEC_CSELR) register is not write-protected.	X	X
AFEC	Performance	2.1.2	The AFEC is sensitive to noise. Too much noise may lead to reduced AFEC performance, especially INL, DNL and SNR.	X	X
AFEC	AOFF bit	2.1.3	Changing the Analog Offset (AOFF) bit in the AFEC Channel Offset Compensation (AFEC_COOCR) register during conversions is not safe.	X	X
ARM Cortex-M7	ARM® Cortex®-M7	2.2.1	All issues related to the ARM r0p1 (for MRLA) and r1p1 (and MRLB) cores are described on the ARM site.	X	X
Boundary Scan Mode	Internal Regulator	2.3.1	The internal regulator is OFF in Boundary Scan mode.	X	
Device	AHB Peripheral (AHBP)	2.4.1	Peripheral accesses done through the AHBP with a Core/Bus ratio of 1/3 and 1/4 may lead to unpredictable results.	X	X
Device	AHB Client (AHBS) Port Latency Access	2.4.2	DMA accesses done through the AHBS to the TCM with a Core/Bus ratio of 1/2, 1/3, and 1/4 may lead to latency due to one Wait state added to the access from the bus to AHBS.	X	X
Device	Reserved	2.4.3	Reserved		
Device	GMAC Registers Corruption on HSMCI, PMC, XDMAC and USBHS Registers	2.4.4	Values for HSMCI, PMC, XDMAC and USBHS registers with same offset than some specific GMAC registers, are not read out correctly.	X	X
XDMAC	TCM Accesses	2.5.1	If TCM accesses are generated through the AHBS port of the core, only 32-bit accesses are supported.	X	
XDMAC	Byte and Half-Word Accesses	2.5.2	If XDMAC is used to transfer 8-bit or 16-bit data in Fixed Source Address mode or Fixed Destination Address mode, source and destination addresses are incremented by 8-bit or 16-bit.	X	X
XDMAC	Request Overflow Error	2.5.3	When a DMA memory-to-memory transfer is performed, if the hardware request line selected by the field PERID bit in the XDMAC_CCx register toggles when the copy is enabled, the Request Overflow Error Interrupt Status (ROIS) bit in the XDMAC_CISx register is set incorrectly.	X	X
FFPI	Flash Programming	2.6.1	The FFPI programs only 1 MB of Flash memory.	X	
GMAC	Priority Queues	2.7.1	Only three priority queues are available.	X	
I2SC	Module Availability	2.8.1	The Inter-IC Sound Controller (I2SC) is not available.	X	
I2SC	Corrupted First Sent Data	2.8.2	Immediately after the I2SC module is reset, the first data sent by the controller on the Serial Data Output (I2SC_DO) line is corrupted.		X
MCAN	Non-ISO Operation	2.9.1	The default frame format does not match the default format specified in the current device data sheet.	X	
MCAN	MCANN_CCCR Register	2.9.2	The MCAN CC Control register content does not match the content of the current device data sheet.	X	
MCAN	Transmitter Delay Compensation Value (TDCV) Bits	2.9.3	The Transmitter Delay Compensation Value (TDCV) bit field does not match the content in the current device data sheet.	X	
MCAN	MCAN_PSR Register	2.9.4	The content of the MCAN Protocol Status register differs from the content in the current device data sheet.	X	
MCAN	MCAN_IR Register	2.9.5	The content of the MCAN Interrupt register differs from the content in the current device data sheet.	X	
MCAN	MCAN_IE Register	2.9.6	The content in the MCAN Interrupt Enable register does not match the content in the current device data sheet.	X	
MCAN	MCAN_ILS Register	2.9.7	The content in the MCAN Interrupt Line Support Register does not match the content in the current device data sheet.	X	

SAM E70/S70/V70/V71 Family

Silicon Errata Summary

.....continued

Module	Feature	Errata Number	Summary	Affected Silicon Revisions	
				A	B
MCAN	MCAN Data Bit Timing and Prescaler Register	2.9.8	The MCAN Data Bit Timing and Prescaler register (MCAN_DBTP) is named MCAN Fast Bit Timing and Prescaler register (MCAN_FBTP).	X	
MCAN	MCAN Nominal Bit Timing and Prescaler Register	2.9.9	The MCAN Nominal Bit Timing and Prescaler register (MCAN_NBTP) is named MCAN Bit Timing and Prescaler register (MCAN_BTP).	X	
MCAN	MCAN Transmitter Delay Compensation Register	2.9.10	The MCAN Transmitter Delay Compensation Register (MCAN_TDCR) does not exist.	X	
MCAN	Timestamping Function	2.9.11	TC Counter 0 is not connected to PCK6 and PCK7; therefore, the timestamping functionality does not exist.	X	
PIO	PIO Line Configuration for AFEC and DACC Analog Inputs	2.10.1	Analog inputs, AFE_ADx or DACx, may not properly enable when internal pull-up or pull-down resistors are enabled.	X	X
PMC	Wait Mode Exit Fail from Flash	2.11.1	The delay to exit from Wait mode is too short to respect the Flash wake-up time from Standby mode and Deep Power-Down mode. This delay may lead to bad opcode fetching.	X	X
PMC	Reserved	2.11.2	Reserved		
QSPI	Module Hangs with Long DLYCS	2.12.1	The QSPI module hangs if a command is written to any QSPI register during the delay defined in the DLYCS bit. There is no status bit to flag the end of the delay.	X	X
QSPI	Reserved	2.12.2	Reserved		
RTC	RTC_CALR Reset Value	2.13.1	The reset value of the RTC_CALR register is 0x01E11220.	X	
SDRAMC	Reserved	2.14.1	Reserved		
SDRAMC	Reserved	2.14.2	Reserved		
SDRAMC	Reserved	2.14.3	Reserved		
SDRAMC	SDRAM	2.14.4	The SDRAM Controller is not functional and should not be used. Support for this for all versions has been removed.	X	X
SMC	SMC_WPSR Register Write Protection	2.15.1	When the write protection feature is enabled and a write attempt into a protected register is performed, the Write Protection Violation Source (WPVSR) bit field in the SMC_WPSR register does not report the right violation source.	X	X
SSC	Inverted Left/Right Channels	2.16.1	When the SSC is in Client mode, the Transmit Frame Synchronization (TF) signal is derived from the codec and not controlled by the SSC.	X	
SSC	Unexpected TD Output Delay	2.16.2	An unexpected delay on Transmit Data (TD) output may occur when the SSC is configured under certain conditions.	X	X
SUPC	Write-Protection	2.17.1	The SUPC_WUIR register is not write-protected.	X	X
SUPC	Programmable Clock Controller	2.17.2	Programmable Clock Outputs, PCK0–PCK2, selected from the clock generator outputs to drive the device PCK pins are not supported and should not be used.	X	X
TWIHS	I ² C Hold Timing Incompatibility	2.18.1	The TWIHS module is not compatible with I ² C hold timing.	X	
TWIHS	Clear Command	2.18.2	A bus reset using the CLEAR bit of the TWIHS Control register does not work correctly during a bus busy state.	X	
USART	Flow Control with DMA	2.19.1	The RTS signal is not connected to the DMA. Therefore, when DMA is used, Flow Control is not supported.	X	X
USART	Bad Frame Detection	2.19.2	If a bad frame is received (i.e., incorrect baud rate) with the last data bit being sampled at 1, frame error detection does not occur.	X	X
USART	LIN Bit Error	2.19.3	When transmitting, after a bit error occurs, the next header is not sent correctly after clearing the US_CSR.LINBE flag by writing a 1 to the RSTSTA bit of the Control Register.	X	X
USBHS	USBHS Host	2.20.1	The USB Host does not function in Low-Speed mode.	X	
USBHS	64-pin LQFP Package	2.20.2	The USBHS module does not function in 64-pin LQFP package devices.	X	X
USBHS	No DMA for Endpoint 7	2.20.3	The DMA feature is not available for Pipe/Endpoint 7.	X	X

SAM E70/S70/V70/V71 Family

Silicon Errata Summary

.....continued

Module	Feature	Errata Number	Summary	Affected Silicon Revisions	
				A	B
USBHS	High-Speed Detach/Attach	2.20.4	Detaching the USB Device by setting the USBHS_DEVCTRL_DETACH bit when a Single Ended Zero(SE0) condition is present on the USB Data lines will cause the USBHS module to enter an unknown state.	X	X
DACC	Interpolation Mode	2.21.1	Interpolation Mode is not functional	X	X
RSTC	Watchdog Reset	2.22.1	Infinite Watchdog Reset loop.	X	X
ISI	Grayscale Little Endian	2.23.1	Grayscale Little Endian feature (ISI_CFG1.GRAYLE) is not supported.	X	

2. SAM E70/S70/V70/V71 Errata Issues

The following errata issues apply to the SAM E70/S70/V70/V71 silicon family devices.

2.1 Analog Front-End Controller (AFEC)

2.1.1 Write Protection

The AFEC Channel Selection (AFEC_CSELR) register is not write-protected.

Workaround

None.

Affected Silicon Revisions

A	B						
X	X						

2.1.2 Performance

The AFEC is sensitive to noise. Too much noise may lead to reduced AFEC performance, especially INL, DNL and SNR. The following situations will generate the noise:

- Using a 64-pin QFP package option (it does not have the VREFN pin)
- Device activity (that is, clock tree)
- External components (that is, missing on-board supply decoupling capacitors)

Workaround

Adapt the environment to the expected level of performances.

Affected Silicon Revisions

A	B						
X	X						

2.1.3 AOFF bit

Changing the Analog Offset (AOFF) bit in the AFEC Channel Offset Compensation (AFEC_COCCR) register during conversions is not safe.

The recommended value of the AOFF bit is 512 (the default value is zero). Different values are possible for each channel. The AOFF bit is read and updated during the AFE start-up sequence and at the end of each conversion. If during AFE idle time (no conversion is on-going) the user updates the AOFF bit for the next channel to be converted, the next conversion will be incorrect.

Workaround

The value of the AOFF bit can be updated only if the AFEC module is restarted, or if two conversions are run; the second one will have the correct AOFF bit setting.

Affected Silicon Revisions

A	B						
X	X						

2.2 Arm® Cortex®-M7

2.2.1 Arm Cortex-M7

All issues related to the Arm r0p1 (for MRLA) and r1p1 (and MRLB) cores are described on the Arm website.

Workaround

Refer to the following Arm documentation:

- For Arm Cortex-M7 r0p1 core (MRLA device): <https://silver.arm.com/download/download.tm?pv=2004343>
- For Arm Cortex-M7 r1p1 core (MRLB device): <https://silver.arm.com/download/download.tm?pv=3257391&p=1929427>
- Arm Embedded Trace Macrocell CoreSight ETM-M7 (TM975) Software Developers Errata Notice: <https://silver.arm.com/download/download.tm?pv=1998309>

Affected Silicon Revisions

A	B						
X	X						

2.3 Boundary Scan Mode

2.3.1 Internal Regulator

The internal regulator is OFF in Boundary Scan mode.

Workaround

The user must provide external VDDCORE (1.2V Typ.) to perform Boundary Scan mode.

Affected Silicon Revisions

A	B						
X							

2.4 Device

2.4.1 AHB Peripheral (AHBP) Port Frequency Ratio

Peripheral accesses done through the AHBP with a Core/Bus ratio of 1/3 and 1/4 may lead to unpredictable results.

Workaround

The user must use a Core/Bus frequency ratio of 1 or 1/2.

Affected Silicon Revisions

A	B						
X	X						

2.4.2 AHB Client (AHBS) Port Latency Access

DMA accesses done through the AHBS to the TCM with a Core/Bus ratio of 1/2, 1/3, and 1/4 may lead to latency due to one Wait state added to the access from the bus to AHBS.

Workaround

The user must use only the Core/Bus frequency ratio of 1 to guarantee the length of the access.

Affected Silicon Revisions

A	B						
X	X						

2.4.3 Reserved

2.4.4 GMAC Registers Corruption on HSMCI, PMC, XDMAC and USBHS Registers

Whenever there is any non-zero value in the following registers, values for registers with same offset in other peripherals (HSMCI, PMC, XDMAC, and USBHS) are not read out correctly:

- 0x0500-0x055C (GMAC Screening Type 1/2 Registers) - GMAC_ST1RPQx or GMAC_ST2RPQx
- 0x06E0-0x06EC (GMAC Screening Type 2 Ether Type Registers) - GMAC_ST2ERx
- 0x0700-0x07BC (GMAC Screening Type 2 Compare Registers) - GMAC_ST2CW0x and GMAC_ST2CW1x

Workaround

While reading the affected registers from other peripherals, the user needs to ensure that the GMAC register with the same offset address have a value of "0x00000000".

Affected Silicon Revisions

A	B						
X	X						

2.5 Extended DMA Controller (XDMAC)

2.5.1 TCM Accesses

If TCM accesses are generated through the AHBS port of the core, only 32-bit accesses are supported. Accesses that are not 32-bit aligned may overwrite bytes at the beginning and at the end of 32-bit words.

Workaround

The user application must use 32-bit aligned buffers and buffers with a size of a multiple of 4 bytes when transferring data to or from the TCM through the AHBS port of the core.

Affected Silicon Revisions

A	B						
X							

2.5.2 Byte and Half-Word Accesses

If XDMAC is used to transfer 8-bit or 16-bit data in Fixed Source Address mode or Fixed Destination Address mode, source and destination addresses are incremented by 8-bit or 16-bit.

Workaround

The user can resolve this issue by setting the source and destination addressing mode to use microblock and data striding with microblock stride set to 0 and data stride set to -1.

Affected Silicon Revisions

A	B						
X	X						

2.5.3 Request Overflow Error

When a DMA memory-to-memory transfer is performed, if the hardware request line selected by the field PERID bit in the XDMAC_CCx register toggles when the copy is enabled, the Request Overflow Error Interrupt Status (ROIS) bit in the XDMAC_CISx register is set incorrectly. The memory transfer proceeds normally and the data area is correctly transferred.

Workaround

Configure the PERID bit to an unused peripheral ID.

Affected Silicon Revisions

A	B						
X	X						

2.6 Fast Flash Programming Interface (FFPI)

2.6.1 Flash Programming

The FFPI programs only 1 MB of Flash memory.

Workaround

None.

Affected Silicon Revisions

A	B						
X							

2.7 Ethernet MAC (GMAC)

2.7.1 Priority Queues

Only three priority queues are available with the following sizes:

Queue Number	Queue Size
2 (highest priority)	4 KB
1	2 KB
0 (lowest priority)	2 KB

Workaround

None.

Affected Silicon Revisions

A	B						
X							

2.8 Inter-IC Sound Controller (I2SC)

2.8.1 Module Availability

The Inter-IC Sound Controller (I2SC) is not available.

Workaround

None.

Affected Silicon Revisions

A	B						
X							

2.8.2 Corrupted First Sent Data

Immediately after the I2SC module is reset, the first data sent by the controller on the Serial Data Output (I2SC_DO) line is corrupted. Any data that follows is not affected.

Workaround

None.

Affected Silicon Revisions

A	B						
	X						

2.9 Controller Area Network (MCAN)

2.9.1 Non-ISO Operation

The default frame format does not match the default format specified in the current device data sheet.

Workaround

Set the MCAN_CCCR.NISO bit to '1'.

Affected Silicon Revisions

A	B						
X							

2.9.2 MCAN_CCCR Register

The MCAN CC Control register content does not match the content of the current device data sheet.

- The NISO bit is missing
- The EFBI bit is named as FDBS
- The PXHD bit is named as FDO

- The BRSE and FDOE bits are named as CME[1:0]
- The CMR[1:0] bits are present

Workaround

None.

Affected Silicon Revisions

A	B						
X							

2.9.3 Transmitter Delay Compensation Value (TDCV) Bits

The Transmitter Delay Compensation Value (TDCV) bit field does not match the content in the current device data sheet.

The TDCV bits are located in the MCAN_TEST register.

In the current device data sheet, the TDCV bits are located in the MCAN_PSR register.

Workaround

None.

Affected Silicon Revisions

A	B						
X							

2.9.4 MCAN_PSR Register

The content of the MCAN Protocol Status register differs from the content in the current device data sheet.

- The PXE bit is not available
- The RFDF bit is named as REDL
- The DLEC[2:0] bits are named as FLEC[2:0]

Workaround

None.

Affected Silicon Revisions

A	B						
X							

2.9.5 MCAN_IR Register

The content of the MCAN Interrupt register differs from the content in the current device data sheet.

- The STE and FOE bits are present
- The ARA bit is replaced by the ACKE bit
- The PED bit is replaced by the BE bit
- The PEA bit is replaced by the CRCE bit

Workaround

None.

Affected Silicon Revisions

A	B						
X							

2.9.6 MCAN_IE Register

The content in the MCAN Interrupt Enable register does not match the content in the current device data sheet.

- The STEE and FOEE bits are present
- The ARAE bit is replaced by the ACKEE bit
- The PEDE bit is replaced by the BEE bit
- The PEAE bit is replaced by the CRCEE bit

Workaround

None.

Affected Silicon Revisions

A	B						
X							

2.9.7 MCAN_ILS Register

The content in the MCAN Interrupt Line Support Register does not match the content in the current device data sheet.

- The STEL and FOEL bits are present
- The ARAL bit is replaced by the ACKEL bit
- The PEDL bit is replaced by the BEL bit
- The PEAL bit is replaced by the CRCEL bit

Workaround

None.

Affected Silicon Revisions

A	B						
X							

2.9.8 MCAN Data Bit Timing and Prescaler Register

The MCAN Data Bit Timing and Prescaler (MCAN_DBTP) register is named MCAN Fast Bit Timing and Prescaler (MCAN_FBTP) register. The MCAN_DBTP and MCAN_FBTP registers do not share the same bit fields.

Workaround

Ensure that the name MCAN_FBTP and the MCAN_FBTP settings are used.

Affected Silicon Revisions

A	B						
X							

2.9.9 MCAN Nominal Bit Timing and Prescaler Register

The MCAN Nominal Bit Timing and Prescaler (MCAN_NBTP) register is named as the MCAN Bit Timing and Prescaler (MCAN_BTP) register.

Workaround

Ensure that the name MCAN_BTP is used.

Affected Silicon Revisions

A	B						
X							

2.9.10 MCAN Transmitter Delay Compensation Register

The MCAN Transmitter Delay Compensation Register (MCAN_TDCR) does not exist.

Workaround

The transmit delay compensation offset is configured in the TDCO field of the MCAN_FBTP register.

Affected Silicon Revisions

A	B						
X							

2.9.11 Timestamping Function

TC Counter 0 is not connected to PCK6 and PCK7; therefore, the timestamping functionality does not exist.

Workaround

None.

Affected Silicon Revisions

A	B						
X							

2.10 Parallel Input/Output (PIO)

2.10.1 PIO Line Configuration for AFEC and DACC Analog Inputs

Analog inputs, AFE_ADx or DACx, may not enable when internal pull-up or pull-down resistors are enabled.

Workaround

Disable the internal pull-up or pull-down resistors by writing a '1' to the PIO_PUDR or PIO_PPDDR for the port pins where analog inputs are needed.

Affected Silicon Revisions

A	B						
X	X						

2.11 Power Management Controller (PMC)

2.11.1 Wait Mode Exit Fail from Flash

The delay to exit from Wait mode is too short to respect the Flash wake-up time from Stand-by mode and Deep Power-Down mode. This delay may lead to bad opcode fetching.

Workaround 1

Use the Flash in Idle mode (FLPM = 2).

Workaround 2

If Flash in Stand-by mode (FLPM = 0) or in Deep Power-Down mode (FLPM = 1) is used, run the wake-up routine from SRAM. This option provides a slight improvement in power consumption.

Affected Silicon Revisions

A	B						
X	X						

2.11.2 Reserved

2.12 Quad Serial Peripheral Interface (QSPI)

2.12.1 Module Hangs with Long DLYCS

The QSPI module hangs if a command is written to any QSPI register during the delay defined in the DLYCS bit. There is no status bit to flag the end of the delay.

Workaround

The DLYCS bit defines a minimum period over which the Chip Select is deasserted, which is required by some memories. This delay is generally less than 60 ns and comprises internal execution time, arbitration, and latencies. Therefore, the DLYCS bit must be configured to be slightly higher than the value specified for the client device. The software must wait for at least this same period of time before a command can be written to the QSPI module.

Affected Silicon Revisions

A	B						
X	X						

2.12.2 Reserved

2.13 Real-Time Clock (RTC)

2.13.1 RTC_CALR Reset Value

The reset value of the RTC_CALR register is 0x01E11220.

Workaround

None.

Affected Silicon Revisions

A	B						
X							

2.14 SDRAM Controller (SDRAMC)

2.14.1 Reserved

2.14.2 Reserved

2.14.3 Reserved

2.14.4 SDRAM Support

The SDRAM Controller is not functional and should not be used. Support for this for all versions has been removed.

Workaround

None.

Affected Silicon Revisions

A	B						
X	X						

2.15 Static Memory Controller (SMC)

2.15.1 SMC_WPSR Register Write Protection

When the write protection feature is enabled and a write attempt into a protected register is performed, the Write Protection Violation Source (WPVSRC) bit field in the SMC_WPSR register does not report the right violation source. As a consequence, the value in the WPVSRC bit field is incorrect. This issue does not affect the write protection feature itself, which is fully functional.

Workaround

None.

Affected Silicon Revisions

A	B						
X	X						

2.16 Serial Synchronous Controller (SSC)

2.16.1 Inverted Left/Right Channels

When the SSC is in Client mode, the Transmit Frame Synchronization (TF) signal is derived from the codec and not controlled by the SSC. The SSC transmits the data when detecting the falling edge on the TF signal after the SSC transmission is enabled. In some cases of overflow, a left/right channel inversion may occur. When this occurs, the SSC must be reinitialized.

Workaround

Using the SSC in Host mode will ensure that TF is controlled by the SSC and no error occurs. If the SSC must be used in TF Client mode, the SSC must be started by writing TXEN and RXEN synchronously with the TXSYN flag rising in the SSC_SR.

Affected Silicon Revisions

A	B						
X							

2.16.2 Unexpected TD Output Delay

An unexpected delay on Transmit Data (TD) output may occur when the SSC is configured with the following conditions:

- The START bit in the RCMR register = Start on falling edge/Start on Rising edge/Start on any edge
- The FSOS bit in the RFMR register = None (input)
- The START bit in the TCMR register = Receive Start

Under these conditions, an unexpected delay of two or three system clock cycles is added to the TD output.

Workaround

None.

Affected Silicon Revisions

A	B						
X	X						

2.17 Supply Controller (SUPC)

2.17.1 Write-Protection

The SUPC_WUIR register is not write-protected.

Workaround

None.

Affected Silicon Revisions

A	B						
X	X						

2.17.2 Programmable Clock Controller

Programmable Clock Outputs, PCK0 and PCK2, selected from the clock generator outputs to drive the device PCK pins are not supported and should not be used.

Workaround

Use PCK1.

Table 2-1. Affected Silicon Revisions

A	B						
X	X						

2.18 TWI High-Speed (TWIHS)

2.18.1 I²C Hold Timing Incompatibility

The TWIHS module is not compatible with I²C hold timing. The divider to program the hold time is too short to achieve the expected hold time at high frequency. The achieved time is 227 ns maximum at 150 MHz, instead of the required 300 ns.

Workaround

None.

Affected Silicon Revisions

A	B						
X							

2.18.2 Clear Command

A bus reset using the CLEAR bit of the TWIHS Control register does not work correctly during a bus busy state.

Workaround

Reconfigure the TWCK line in GPIO output and generate nine clock pulses through software to unlock the I²C device. After that the TWCK line can be reconfigured as a peripheral line.

Affected Silicon Revisions

A	B						
X							

2.19 Universal Synchronous Asynchronous Receiver Transmitter (USART)

2.19.1 Flow Control with DMA

The CTS and RTS signals are not connected to DMA. Therefore, when DMA is used, Flow Control is not supported.

Workaround

None.

Affected Silicon Revisions

A	B						
X	X						

2.19.2 Bad Frame Detection

If a bad frame is received (that is, incorrect baud rate) with the last data bit being sampled at 1, frame error detection does not occur.

Workaround

There is no general workaround. When performing baud rate detection with receive part, the transmit frame must be sent with a parity bit set to '0'.

Affected Silicon Revisions

A	B						
X	X						

2.19.3 LIN Bit Error

When transmitting, after a bit error occurs (US_CSR.LINBE = 1), the next header is not sent correctly after clearing the US_CSR.LINBE flag by writing a '1' to the RSTSTA bit of the Control register (US_CSR.RSTSTA = 1).

Workaround

After a bit error occurs (US_CSR.LINBE = 1), reset the transmitter (US_CR.RSTTX = 1) and re-enable it (US_CR.TXEN = 1).

Affected Silicon Revisions

A	B						
X	X						

2.20 USB High-Speed (USBHS)

2.20.1 USBHS Host Does Not Function in Low-Speed Mode

The USB Host does not function in Low-Speed mode.

Workaround

None.

Affected Silicon Revisions

A	B						
X							

2.20.2 64-pin LQFP Package

The USBHS module does not function in 64-pin LQFP package devices.

Workaround

None.

Affected Silicon Revisions

A	B						
X	X						

2.20.3 No DMA for Endpoint 7

The DMA feature is not available for Pipe/Endpoint 7.

Workaround

None.

Affected Silicon Revisions

A	B						
X	X						

2.20.4 USBHS Detach Can Fail While SE0 Condition Exists

Detaching the USB device by setting the USBHS_DEVCTRL_DETACH bit when a Single-Ended Zero (SE0) condition is present on the USB data lines will cause the USBHS module to enter an unknown state. This issue occurs only in the high-speed operation. Attempting to reattach the device by clearing the USBHS_DEVCTRL_DETACH bit will not work.

Workaround

When operating in High-Speed mode, ensure that the device detach (USBHS_DEVCTRL_DETACH = 1) is followed by a USB module disable (USBHS_CTRL.USBE = 0). To attach the device, enable the USB module ((USBHS_CTRL.USBE = 1) and then clear the detach bit (USBHS_DEVCTRL_DETACH = 0).

Affected Silicon Revisions

A	B						
X	X						

2.21 Digital-to-Analog Converter Controller (DACC)

2.21.1 Interpolation Mode

The Interpolation mode that allows Oversampling Ratio (OSR) of 2x, 4x, 8x, 16x, or 32x is not functional.

Workaround

None.

Affected Silicon Revisions

A	B						
X	X						

2.22 Reset Controller (RSTC)

2.22.1 Watchdog Reset

With External Reset Length set to 0 (MR.ERSTL= 0) in the Reset Controller Mode register, a Watchdog Reset may cause an Infinite Reset loop.

Workaround

To ensure a correct Watchdog Reset of the system, the ERSTL field in the Reset Controller Mode register must be set to a non-zero value (MR.ERSTL >= 1).

Affected Silicon Revisions

A	B						
X	X						

2.23 Image Sensor Interface (ISI)

2.23.1 Greyscale Little Endian

Greyscale Little Endian feature (ISI_CFG1.GRAYLE) is not supported.

Workaround:

None.

Affected Silicon Revisions

A	B						
X							

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest revision of the device data sheet (DS60001527G):

Note: Corrections in tables, registers, and text are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 Controller Area Network (MCAN)

The MCAN_CREL register reset value documented in the data sheet is applicable to devices with silicon revision B. The MCAN_CREL register reset value for devices with silicon revision A is 0x30130506.

4. Appendix A: Revision History

Revision L (06/2022)

The following silicon errata were added in this revision:

- [USART: 2.19.3 LIN Bit Reference](#)

The following errata were updated with new verbiage:

- [SDRAMC: 2.14.4 SDRAM Support](#)

Revision K (03/2022)

The following silicon errata is added in this revision:

- [DEVICE: 2.4.4 GMAC Registers Corruption on HSMCI, PMC, XDMAC and USBHS Registers](#)

The following Silicon Errata were deprecated, and are now marked as *Reserved*:

- [PMC: 12.2](#)
- [QSPI: 13.2](#)

Revision J (08/2021)

The following silicon errata were added in this revision:

- [SDRAMC: 15.4 SDRAM](#)

The following errata were removed:

- [Device 5.3](#)
- [SDRAMC 15.1](#)
- [SDRAMC 15.2](#)
- [SDRAMC 15.3](#)

Revision H (05/2021)

The SPI and I²C standards use the terminology "Master" and "Slave". The equivalent Microchip terminology, "Host" and "Client" is used in this document. This terminology has been updated throughout this document for this revision.

Added a new silicon issue:

- [24.1 ISI Greyscale Little Endian](#)

Revision G (12/2020)

Added a new Silicon Issue:

- [23.1 RSTC Watchdog Reset](#)

Revision F (02/2020)

Added a new Silicon issue:

- [21.4 USBHS High Speed Detach/Attach](#)

Revision E (09/2019)

The following silicon issues were updated with new verbiage:

- [10.8 MCAN Data Bit Timing and Prescaler Register](#)
- [11.1 PIO Line Configuration for AFEC and DACC Analog Inputs](#)

Revision D (5/2019)

Updated the [Silicon Issue Summary](#) table to be more readable.

The following Silicon Issues were updated:

- [Boundary Scan Mode: Internal Regulator](#)
- [XDMAC: TCM Accesses](#)

- [FFPI: Flash Programming](#)
- [PMC: Wait Mode Exit Fail from Flash](#)
- [SDRAMC: SDRAM Controller Scrambling Use Limitation](#)
- [SMC: SMC_WPSR Register Write Protection](#)
- [TWIHS: I²C Hold Timing Incompatibility](#)
- [TWIHS: Clear Command](#)

The following Silicon Issues were added:

- [DEVICE: System Performance](#)
- [SDRAMC:Operational Voltage](#)

Revision C (11/2018)

The following Silicon Issues were added:

- [18.2 Programmable Clock Controller](#)
- [22.1 Interpolation Mode](#)

The following Data Sheet Clarifications were added:

- [Controller Area Network \(MCAN\)](#)
- [Quad Serial Peripheral Interface \(QSPI\)](#)

Revision B (8/2018)

This revision was updated for Revision B silicon.

The following Silicon Issue was added:

- [13.2 WDRBT](#)

Revision A (11/2017)

Initial release of this document.

The Microchip Web Site

Microchip provides online support via our web site at www.microchip.com/. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Customer Change Notification Service

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com/. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: www.microchip.com/support

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Legal Notice

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks

The Microchip name and logo, the Microchip logo, AnyRate, AVR, AVR logo, AVR Freaks, BeaconThings, BitCloud, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, Heldo, JukeBlox, KeeLoq, KeeLoq logo, Kleer, LANCheck, LINK MD, maXStylus, maXTouch, MediaLB, megaAVR, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, Prochip Designer, QTouch, RightTouch, SAM-BA, SpyNIC, SST, SST Logo, SuperFlash, tinyAVR, UNI/O, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, EtherSynch, Hyper Speed Control, HyperLight Load, IntelliMOS, mTouch, Precision Edge, and Quiet-Wire are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BodyCom, chipKIT, chipKIT logo, CodeGuard, CryptoAuthentication, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, Inter-Chip Connectivity, JitterBlocker, KleerNet, KleerNet logo, Mindi, MiWi, motorBench, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PureSilicon, QMatrix, RightTouch logo, REAL ICE, Ripple Blocker, SAM-ICE, Serial Quad I/O, SMART-I.S., SQI, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2017, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

ISBN: 978-1-6683-0694-9

Quality Management System Certified by DNV

ISO/TS 16949

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC[®] MCUs and dsPIC[®] DSCs, KEELOQ[®] code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
<p>Corporate Office 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: http://www.microchip.com/support Web Address: www.microchip.com</p> <p>Atlanta Duluth, GA Tel: 678-957-9614 Fax: 678-957-1455</p> <p>Austin, TX Tel: 512-257-3370</p> <p>Boston Westborough, MA Tel: 774-760-0087 Fax: 774-760-0088</p> <p>Chicago Itasca, IL Tel: 630-285-0071 Fax: 630-285-0075</p> <p>Dallas Addison, TX Tel: 972-818-7423 Fax: 972-818-2924</p> <p>Detroit Novi, MI Tel: 248-848-4000</p> <p>Houston, TX Tel: 281-894-5983</p> <p>Indianapolis Noblesville, IN Tel: 317-773-8323 Fax: 317-773-5453 Tel: 317-536-2380</p> <p>Los Angeles Mission Viejo, CA Tel: 949-462-9523 Fax: 949-462-9608 Tel: 951-273-7800</p> <p>Raleigh, NC Tel: 919-844-7510</p> <p>New York, NY Tel: 631-435-6000</p> <p>San Jose, CA Tel: 408-735-9110 Tel: 408-436-4270</p> <p>Canada - Toronto Tel: 905-695-1980 Fax: 905-695-2078</p>	<p>Asia Pacific Office Suites 3707-14, 37th Floor Tower 6, The Gateway Harbour City, Kowloon Hong Kong Tel: 852-2943-5100 Fax: 852-2401-3431</p> <p>Australia - Sydney Tel: 61-2-9868-6733 Fax: 61-2-9868-6755</p> <p>China - Beijing Tel: 86-10-8569-7000 Fax: 86-10-8528-2104</p> <p>China - Chengdu Tel: 86-28-8665-5511 Fax: 86-28-8665-7889</p> <p>China - Chongqing Tel: 86-23-8980-9588 Fax: 86-23-8980-9500</p> <p>China - Dongguan Tel: 86-769-8702-9880</p> <p>China - Guangzhou Tel: 86-20-8755-8029</p> <p>China - Hangzhou Tel: 86-571-8792-8115 Fax: 86-571-8792-8116</p> <p>China - Hong Kong SAR Tel: 852-2943-5100 Fax: 852-2401-3431</p> <p>China - Nanjing Tel: 86-25-8473-2460 Fax: 86-25-8473-2470</p> <p>China - Qingdao Tel: 86-532-8502-7355 Fax: 86-532-8502-7205</p> <p>China - Shanghai Tel: 86-21-3326-8000 Fax: 86-21-3326-8021</p> <p>China - Shenyang Tel: 86-24-2334-2829 Fax: 86-24-2334-2393</p> <p>China - Shenzhen Tel: 86-755-8864-2200 Fax: 86-755-8203-1760</p> <p>China - Wuhan Tel: 86-27-5980-5300 Fax: 86-27-5980-5118</p> <p>China - Xian Tel: 86-29-8833-7252 Fax: 86-29-8833-7256</p>	<p>China - Xiamen Tel: 86-592-2388138 Fax: 86-592-2388130</p> <p>China - Zhuhai Tel: 86-756-3210040 Fax: 86-756-3210049</p> <p>India - Bangalore Tel: 91-80-3090-4444 Fax: 91-80-3090-4123</p> <p>India - New Delhi Tel: 91-11-4160-8631 Fax: 91-11-4160-8632</p> <p>India - Pune Tel: 91-20-3019-1500</p> <p>Japan - Osaka Tel: 81-6-6152-7160 Fax: 81-6-6152-9310</p> <p>Japan - Tokyo Tel: 81-3-6880-3770 Fax: 81-3-6880-3771</p> <p>Korea - Daegu Tel: 82-53-744-4301 Fax: 82-53-744-4302</p> <p>Korea - Seoul Tel: 82-2-554-7200 Fax: 82-2-558-5932 or 82-2-558-5934</p> <p>Malaysia - Kuala Lumpur Tel: 60-3-6201-9857 Fax: 60-3-6201-9859</p> <p>Malaysia - Penang Tel: 60-4-227-8870 Fax: 60-4-227-4068</p> <p>Philippines - Manila Tel: 63-2-634-9065 Fax: 63-2-634-9069</p> <p>Singapore Tel: 65-6334-8870 Fax: 65-6334-8850</p> <p>Taiwan - Hsin Chu Tel: 886-3-5778-366 Fax: 886-3-5770-955</p> <p>Taiwan - Kaohsiung Tel: 886-7-213-7830</p> <p>Taiwan - Taipei Tel: 886-2-2508-8600 Fax: 886-2-2508-0102</p> <p>Thailand - Bangkok Tel: 66-2-694-1351 Fax: 66-2-694-1350</p>	<p>Austria - Wels Tel: 43-7242-2244-39 Fax: 43-7242-2244-393</p> <p>Denmark - Copenhagen Tel: 45-4450-2828 Fax: 45-4485-2829</p> <p>Finland - Espoo Tel: 358-9-4520-820</p> <p>France - Paris Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79</p> <p>France - Saint Cloud Tel: 33-1-30-60-70-00</p> <p>Germany - Garching Tel: 49-8931-9700</p> <p>Germany - Haan Tel: 49-2129-3766400</p> <p>Germany - Heilbronn Tel: 49-7131-67-3636</p> <p>Germany - Karlsruhe Tel: 49-721-625370</p> <p>Germany - Munich Tel: 49-89-627-144-0 Fax: 49-89-627-144-44</p> <p>Germany - Rosenheim Tel: 49-8031-354-560</p> <p>Israel - Ra'anana Tel: 972-9-744-7705</p> <p>Italy - Milan Tel: 39-0331-742611 Fax: 39-0331-466781</p> <p>Italy - Padova Tel: 39-049-7625286</p> <p>Netherlands - Druen Tel: 31-416-690399 Fax: 31-416-690340</p> <p>Norway - Trondheim Tel: 47-7289-7561</p> <p>Poland - Warsaw Tel: 48-22-3325737</p> <p>Romania - Bucharest Tel: 40-21-407-87-50</p> <p>Spain - Madrid Tel: 34-91-708-08-90 Fax: 34-91-708-08-91</p> <p>Sweden - Gothenberg Tel: 46-31-704-60-40</p> <p>Sweden - Stockholm Tel: 46-8-5090-4654</p> <p>UK - Wokingham Tel: 44-118-921-5800 Fax: 44-118-921-5820</p>