Product Change Notification / SYST-16CFWZ879

Date:

17-May-2022

Product Category:

Wireless IC, Wireless Modules

PCN Type:

Document Change

Notification Subject:

ERRATA - PIC32MZ-W1 MCU and WFI32E01 Module Errata Revision

Affected CPNs:

SYST-16CFWZ879_Affected_CPN_05172022.pdf
SYST-16CFWZ879_Affected_CPN_05172022.csv

Notification Text:

SYST-16CFWZ879

Microchip has released a new Product Documents for the PIC32MZ-W1 MCU and WFI32E01 Module Errata of devices. If you are using one of these devices please read the document located at PIC32MZ-W1 MCU and WFI32E01 Module Errata.

Notification Status: Final

Description of Change: Added new silicon errata issue Wi-Fi and its summary in Table 2.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 17 May 2022

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

PIC32MZ-W1 MCU and WFI32E01 Module Errata

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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PIC32MZ1025W104 MCU and WFI32E01 Module with Wi-Fi® and Hardware-Based Security Accelerator Errata

The PIC32MZ-W1 Family of devices that you have received conform functionally to the current Device Data Sheet (DS70005425), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The silicon revision level can be identified using the current version of MPLAB® X IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB X IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB X IDE project.
3. Configure the MPLAB X IDE project for the appropriate device and hardware debugger.
4. Select *Window* > *Dashboard*, then click the **Refresh Debug Tool Status** icon ( ).
5. The part number and the Device and Revision ID values appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, visit support.microchip.com or contact your local Microchip sales office.

The Device and Revision ID values for the PIC32MZ1025W104 silicon are shown in the table below.

TABLE 1: SILICON DEVICE AND REVISION DETAILS

Part Number	Device ID	Revision ID for Silicon Revision	
		A1	B0
PIC32MZ1025W104	0x80C03053	0x01	NA
PIC32MZ1025W104	0x0A403053	NA	0x02

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Issue	Issue Summary	Affected Revisions	
				A1	B0
CAN	Interrupt	1.	The CAN Wake Interrupt Flag bit, WAKIF, is set even when the CAN module is disabled.	X	X
CAN	CAN	2.	The CAN FIFO abort operation during transmission does not set the TXABAT bit in FIFOCON register.	X	X
I^2C	I^2C Client	3.	The 7-bit address that matches the 10-bit upper address value (111_10xx_xxx) is not accepted regardless of the STRICT bit setting.	X	X
ICSP	TDO	4.	The TDO pin becomes an output and toggles while programming on any ICSP™ PGECx/PGEDx pair.	X	X
SPI	Block Transmission	5.	The SRMT bit incorrectly indicates the end of transmission for the last PBCLK.	X	X
Timer1	Asynchronous Counter	6.	Timer1 in Asynchronous External Counter mode does not reflect the first count from an external T1CLK input.	X	X
Timer1	TMR1 Register	7.	The TMR1 register of Timer1 in Asynchronous mode remains at the initial set value for five external clock pulses after wake-up from Sleep mode.	X	X
Timer1	Asynchronous Mode	8.	Timer1 counts beyond the period value in Asynchronous mode when the period is 0x01.	X	X
UART	TX/RX Interrupt	9.	A UART Transmit Interrupt (UTXISEL[1:0] bits (UxSTA[15:14]) = ‘0b00) is generated and asserted while the transmit buffer contains at least one empty space and the UART Receiver Interrupt Flag bit (URXISEL[1:0] bits (UxSTA[7:6]) = ‘0b00) is asserted while the receive buffer is not empty and non-functional.	X	X
UART	TX Interrupt	10.	A UART Transmit Interrupt (UTXISEL[1:0] bits = ‘0b01) is generated, but does not remain asserted when all of the characters have been transmitted.	X	X
UART	TX Interrupt	11.	A UART Transmit Interrupt (UTXISEL[1:0] bits = ‘0b10) is generated but does not remain asserted while the transmit buffer is empty.	X	X
UART	RX Interrupt	12.	The UART Receive Interrupt flag (URXISEL[1:0] bits = ‘0b01) is asserted only when the receive buffer equals one-half full and not when the receive buffer is greater than one-half full.	X	X
UART	RX Interrupt	13.	The UART Receive Interrupt Flag bit (URXISEL[1:0] bits = ‘0b10) is asserted only when the receive buffer equals three-quarters full and not when the receive buffer is greater than three-quarters full.	X	X

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Issue	Issue Summary	Affected Revisions	
				A1	B0
Watchdog Timer (WDT)	WDT	14.	WDT does not reset the device if WDT writes are performed outside of the WDT window.	X	X
Watchdog Timer (WDT)	WDT	15.	WDT does not reset the CPU within the expected time period across the voltage and temperature ranges.	X	—
Wi-Fi	Data Transmission	16.	Degraded TX EVM is observed during low Wi-Fi traffic with a long idle duration between packet transmission.	X	—
USB	Compliance	17.	SE0 output of the USB peripheral may not meet compliance requirements.	X	X
Power	Low power mode	18.	Excess leakage current observed in some devices under certain voltage and temperature ranges when the USB controller is disabled and not connected.	—	X
Wi-Fi	Wi-Fi	19.	Potential issue whereby the DMA interface module can latch the sub-MSDU length for an A-MSDU from the header as a frame is received but before the FCS is validated, resulting in the possibility of subsequent valid frames being dropped.	X	—

SILICON ERRATA ISSUES

1. Module: CAN

Clear the WAKIF (CxINT[14]) bit prior to enabling the CAN peripheral.

Work around

During the CAN initialization and before enabling the CAN peripheral, clear the WAKIF bit in the user code and this work around is implemented in Harmony.

Affected Silicon Revisions

A1	B0						
X	X						

2. Module: CAN

The CAN FIFO aborts the operation during transmission without setting the TXABAT bit in the FIFOCON register.

Work around

None.

Affected Silicon Revisions

A1	B0						
X	X						

3. Module: I^2C

The 7-bit address that matches the 10-bit upper address value (111_10xx_xxx) is not accepted regardless of the STRICT bit setting.

Work around

None.

Affected Silicon Revisions

A1	B0						
X	X						

4. Module: ICSP

The TDO pin becomes an output and toggles while programming on any ICSP™ PGECx/ PGEDx pair.

Work around

None.

Affected Silicon Revisions

A1	B0						
X	X						

5. Module: SPI

Just before the last block of a transmission is shifted out to the SPI pins, the SRMT bit may incorrectly indicate that the transmission is done. However, this does not affect the Transmit Buffer Empty Interrupt (STXISEL = 0).

Work around

Use the interrupt indication bit to determine the end of transmission.

Affected Silicon Revisions

A1	B0						
X	X						

6. Module: Timer1

In Asynchronous External Counter mode, (i.e., TCS bit (T1CON[1] = 1), TSYNC bit (T1CON[2] = 0) and TECS[1:0] (T1CON[9:8] = '0b01')), the Timer1 register (TMR1) does not reflect the first count from an external T1CLK input.

Work around

Always add 1 to the Timer1 count value to reflect the first count from an external T1CLK input.

Affected Silicon Revisions

A1	B0						
X	X						

7. Module: Timer1

In Asynchronous External Counter mode, (i.e., TCS bit (T1CON[1] = 1), TSYNC bit (T1CON[2] = 0), and TECS[1:0] (T1CON[9:8] = '0b01')), the Timer1 register (TMR1) remains at the initial set value for five external clock pulses after wake-up from Sleep mode.

Work around

None.

Affected Silicon Revisions

A1	B0						
X	X						

8. Module: Timer1

Timer1 counts beyond the period value in Asynchronous mode when the period is 0x01.

Work around

Set the Timer1 period, PR1, to a value greater than 1.

Affected Silicon Revisions

A1	B0						
X	X						

9. Module: UART

A UART Transmit Interrupt (UTXISEL[1:0] bits (UxSTA[15:14]) = ‘0b00) is generated and asserted while the transmit buffer contains at least one empty space and the UART Receiver Interrupt Flag bit (URXISEL[1:0] bits (UxSTA[7:6]) = ‘0b00) is asserted while the receive buffer is not empty and non-functional.

Work around

None.

Affected Silicon Revisions

A1	B0						
X	X						

10. Module: UART

A UART Transmit Interrupt (UTXISEL[1:0] bits = ‘0b01) is generated but does not remain asserted even when all of the characters have been transmitted. Once the IFSx bit is cleared by the user, it does not remain asserted even while all characters have been transmitted. This behavior compounded with finite interrupt latency can create a race condition amongst subsequent TX interrupts.

Work around

To avoid the race condition, clear the UARTx IFSx flag before writing a new value to the TX Buffer, UxTXREG, in the ISR.

Affected Silicon Revisions

A1	B0						
X	X						

11. Module: UART

The UART Transmit UTXISEL[1:0] bits = ‘0b10 Interrupt is generated but does not remain asserted while the transmit buffer is empty. Once the IFS bit is cleared by the user, it does not remain asserted even while the transmit buffer is empty. This behavior compounded with finite interrupt latency can create a race condition amongst subsequent TX interrupts.

Work around

To avoid the race condition, clear the UARTx IFS flag before writing a new value to the TX Buffer, UxTXREG, in the ISR.

Affected Silicon Revisions

A1	B0						
X	X						

12. Module: UART

The UART Receive Interrupt Flag (URXISEL[1:0] bits = ‘0b01) is asserted only when the receive buffer equals one-half full and not when the receive buffer is greater than one-half full.

Work around

Before exiting the UART RX ISR, ensure all the contents of the RX Buffer have been read, by reading the contents of the RX Buffer in the ISR until the URXDA bit (UxSTA[0]) is cleared and this work around is implemented in Harmony.

Affected Silicon Revisions

A1	B0						
X	X						

13. Module: UART

The UART Receive Interrupt Flag bit (URXISEL[1:0] bits = ‘0b10) is asserted only when the receive buffer equals three-quarters full and not when the receive buffer is greater than three-quarters full.

Work around

Before exiting the UART RX ISR, ensure the entire contents of the RX Buffer have been read by reading the contents of the RX Buffer in the ISR until the URXDA bit (UxSTA[10]) is cleared and this work around is implemented in Harmony.

Affected Silicon Revisions

A1	B0						
X	X						

14. Module: Watchdog Timer (WDT)

The WDT does not reset the device if the WDT writes are performed outside of the WDT window.

Work around

None.

Affected Silicon Revisions

A1	B0						
X	X						

15. Module: Watchdog Timer (WDT)

When LPRC is used as a WDT source prescalar, the WDT does not cause a CPU Reset within the time period expected by the WDTPS configurations. The following table shows the WDT and prescaler values, with their corresponding expected reset period and mean values.

TABLE 3: WDTPS CONFIGURATION

PS Value	Input Clock	Expected Time Period	Mean Value
0xA	LRPC	1s	1.026s
0xB	LPRC	2s	2.025s
0xA	LRPC	1s	1.439s
0xB	LPRC	2s	2.357s

Work around

None.

Affected Silicon Revisions

A1	B0						
X	—						

16. Module: Wi-Fi

Degraded TX EVM is observed during low Wi-Fi traffic with a long idle duration between packet transmission due to rapid transient surges in current consumption. The magnitude of EVM degradation varies from device to device. The range of degradation can cause EVM specification failure for MCS6 and MCS7 data rates. Operations like low-frequency ping will show this issue. There is no impact on throughput performance.

Work around

None.

Affected Silicon Revisions

A1	B0						
X	—						

17. Module: USB

The SE0 output state of the USB peripheral while operating in host or device mode may not meet the USB 2.0 electrical standards and, hence, may cause the USB peripheral to fail the USB Eye pattern test.

Work around

None.

Affected Silicon Revisions

A1	B0						
X	X						

18. Module: Power

Excess leakage current observed in some devices under certain voltage and temperature ranges when the USB controller is disabled and not connected.

Work around

To achieve optimal power-down current in deep sleep and extreme deep sleep states, the USB D+ and D- signals must not be left floating. The signals can be tied to GROUND if the USB peripheral is not used.

If the USB peripheral is used, the user can mitigate this issue by connecting two GPIO pins available on the WFI32 device to the D+ and D- USB pins. These GPIO pins must be in the high impedance state during normal USB operation. When the USB peripheral is disabled or the WFI32 device enters the deep sleep state, program these GPIO pins as outputs driving 0V. Configure the GPIO pins as open drain input and disable internal pull-up/pull-down to change to the high impedance state. It is recommended that a 0Ω resistor be added between the GPIO pins and the D+/D- lines to prevent design changes with the future versions of the silicon.

Affected Silicon Revisions

A1	B0						
—	X						

19. Module: Wi-Fi

Potential issue whereby the DMA interface module can latch the sub-MSDU length for an A-MSDU from the header as a frame is received but before the FCS is validated. Because of this, an incorrect length could be latched for a corrupted received frame (A-MSDU or not). Once latched, this length is updated only on the reception of a valid A-MSDU.

This can cause the receiver to lock up. This issue is fixed in the B0 silicon revision by adding logic to clear the latched sub-MSDU length field.

Work around

None.

Affected Silicon Revisions

A1	B0						
X	—						

DATA SHEET CLARIFICATIONS

The following clarifications and additional information are applicable to the latest version of the device data sheet (DS70005425C):

1. The low power mode information updated in Section *35.0 “POWER MANAGEMENT UNIT (PMU)”, Section 36.0 “POWER-SAVING FEATURES”* and *Section 41.0 “ELECTRICAL SPECIFICATIONS*” are relevant for B0 silicon version and later.

APPENDIX A: DOCUMENT REVISION HISTORY

TABLE 4: REVISION HISTORY

Revision	Date	Section	Description
F	05/2022	Document	Added new silicon errata issue Wi-Fi and its summary in Table 2.
E	01/2022	Document	• Updated Workaround of Power errata. • Added **Section "Data Sheet Clarifications"**.
D	11/2021	Document	Added Power errata and its details.
C	10/2021	Document	• Updated the Errata with B0 release information. • Design/implementation-related limitations are now available in the data sheet. • Updated with the new terminologies. For more details, see the following note. • Added USB errata and its details.
B	01/2021	Document	Added new silicon errata issue Wi-Fi and its summary in Table 2.
A	09/2020	Document	Initial release

Note: *Microchip is aware that some terminologies used in the technical documents and existing software codes of this product are outdated and unsuitable. This document may use these new terminologies, which may or may not reflect on the source codes, software GUIs, and the documents referenced within this document. The following table shows the relevant terminology changes made in this document.*

TABLE 5: TERMINOLOGY RELATED CHANGES

Old Terminology	New Terminology	Description
I^2C Slave	I^2C Client	Table 2 is updated with new terminology.

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SYST-16CFWZ879 - ERRATA - PIC32MZ-W1 MCU and WFI32E01 Module Errata Revision

Affected Catalog Part Numbers(CPN)

PIC32MZ1025W104132-I/NX
WFI32E01PE-IA1
WFI32E01UE-IA1
WFI32E01PC-IA1
WFI32E01PCI
WFI32E01UC-IA1
WFI32E01UCI
WFI32E01PC-I
WFI32E01UC-I
WFI32E01PE-I
WFI32E01UE-I