Product Change Notice

(PCN Tracking Number: EE-QR-220409-20)

Version: 1

Customer:	All Customers
Renesas Product Type:	RH850/F1, R1, E1 and C1 series, refer to Product List
Description of Change:	Addition of wafer type for Naka products

Wafer Process	Current wafer specifications	Wafer specifications after change
Naka	EPI Wafer	EPI Wafer Non-EPI Wafer

Reason for Change:	In order to realize stable supply, Renesas will implement specification addition of non-EPI wafers for Naka products in addition to EPI wafers which are current wafer specifications in Naka.
Identification:	Identifiable by T/C code on marking and label for each product.
Schedules:	Requested approval 15. Jul. 2022 Change implementation from Jul. 2022 onwards sequentially
Anticipated Impact:	Fit: No change Form: No change Function: No change Quality & Reliability: No change
Doc. No.:	EEQC-PCN-CR-22-0090
Internal Reference:	AMBD-2022-0351, AMBD-2022-0428

In case of any question, please contact:

INITIATOR	TITLE	E-mail	PHONE No.
Farhad Banihashemi	Staff Engineer	Farhad.Banihashemi@renesas.com	+49-211-6503-1844

Düsseldorf, 21.04.2022

Customer Response:

(please fill in and return by e-mail, fax or mail)

☐ acknowledge
☐ acceptable
☐ inacceptable (pls. comment)
☐ not applicable

Company: _____

Name & Position: _____

Phone / Fax No.: _____

Note: Acknowledgement must be received by Renesas within 30 days or Renesas will consider the change as approved. If timely acknowledgement is provided by Customer, then Customer shall have 90 days from the date of receipt of this PCN in which to make any objections to the PCN. If Customer fails to make objections to this PCN within 90 days of the receipt of the PCN then Renesas will consider the PCN changes as approved. If customer cannot accept the PCN, they must provide Renesas with a last time buy demand and purchase order.

Comments:

_____ (Signature)

Details of Change:

Renesas has been faced with serious supply shortage of Si-wafers due to the demand increase for semiconductors in these years.
In order to avoid delivery shortage and to realize stable supply of Renesas' RH850 series we plan to add non-EPI wafers for the Si-wafer specifications of Naka products in addition to current EPI wafers.

Please refer to below summary for changed items:

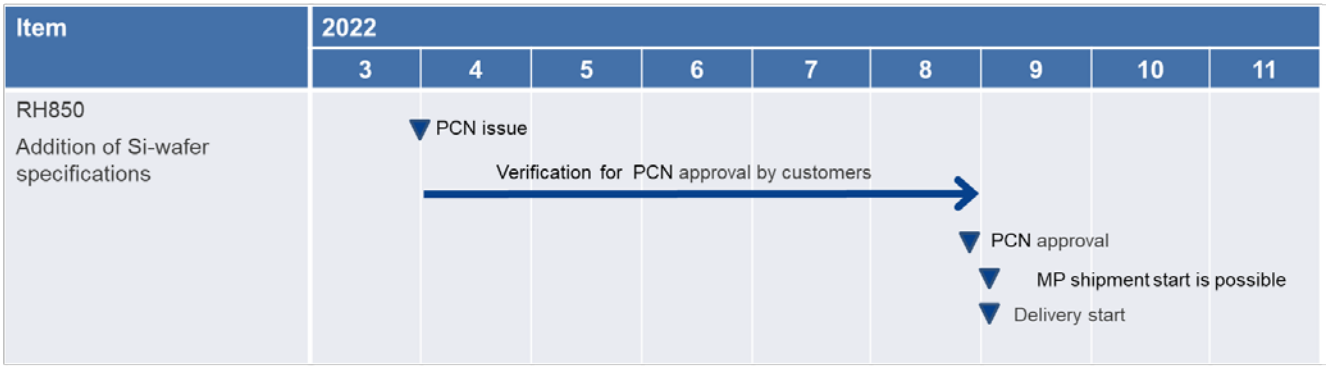
Wafer Process Site: Renesas Semiconductor Manufacturing Co., Ltd. Naka Factory

	Items	Current products	Changed products	Changes
1	Si-Wafer specifications	EPI Wafer	EPI Wafer non-EPI Wafer	w/

4 M1E change items	Conventional products	Change products	4M1E change items	Remarks
Man	Certified workers	←	**No**	
Machine	Machine A	←	**No**	
Material	EPI Wafer	EPI Wafer non-EPI Wafer	**YES**	Addition of Si-wafer specifications
Method	Process method A	←	**No**	
Environment	Process A	←	**No**	

Item	Judgement
Product names	No change
Marking	No change
Label	No change
Product identification	Controlled through Trace Code (T/C) described on Marking (Mark) and Label

Schedule of Change:



Evaluation of the Change

All potential risk items about addition of Si-wafer specifications were verified based on DRBFM. As a result, no problem has been confirmed.

Change Items	Impact due to changes	Concern items	Counter measures	Verification Methods	Judgment (Reference Section)
Addition of Si-wafer specifications	Impact on characteristics	Yield drop	Wafer-Test result confirmation	There is no yield difference between before and after change.	OK
			Final-Test result confirmation	There is no yield difference between before and after change.	OK
		Deterioration in characteristics	Wafer-Test result confirmation	There is no yield difference between before and after change. There is no anomalous defect occurrence.	OK
			Final-Test result confirmation	There is no yield difference between before and after change. There is no anomalous defect occurrence.	OK
			ED (Electrical Distribution) confirmation	There is no significant difference between before and after change.	OK
			Electrical characteristics	There is no significant difference in electrical characteristics between before and after change.	OK
	Impact on reliability	Deterioration in reliability	ESD characteristics	There is no significant difference between before and after change.	OK
			TEG reliability verification	Confirmation of process reliability.	OK

Evaluation Results:

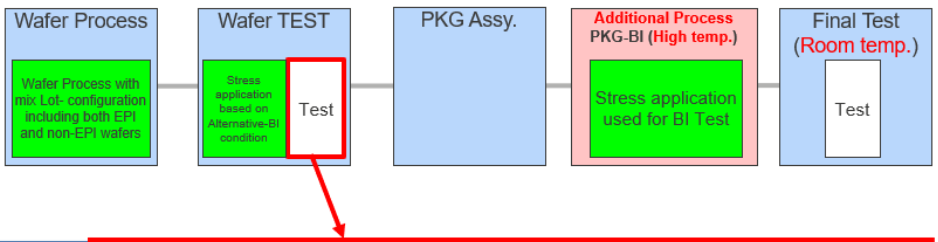
To evaluate the additional wafer type the wafer process for RH850/F1L at Naka was performed with the identical lot which includes both non-EPI wafers and EPI wafers at the normal production flow.

Regarding representative products, we chose the RH850/F1L series whose test yield has been monitored at Naka. Packaged samples of the non-EPI wafers and EPI wafers were assembled at the mass-production flow of RSC.

Regarding stress-application Process, we performed PKG-BI Process in addition to Wafer Test under mass-production flows.

The conditions of used Wafer-Test programs, Final-Test programs, Tester and Test boards were the same as mass-production.

Wafer Test Results:



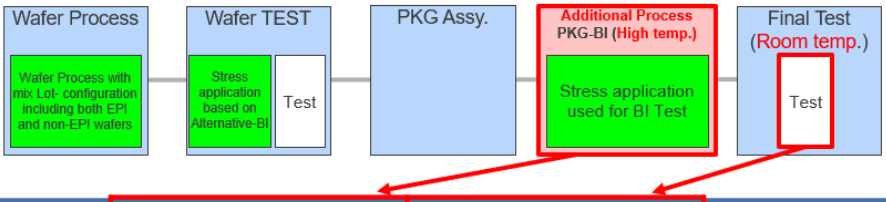
Criteria : There is no significant difference between before and after change.

Products	WT1	WT2	WT3	WT4
non-EPI (After change) *1	1.00	1.00	1.00	1.00
EPI (Mass-production results before change) *1	1.00	1.00	1.00	1.00

*1 Relative values at EPI yield results (Mass-production results before change) = 1

We confirmed that there was no change in yield due to the change of Si-wafer specifications.

Final Test Results:



Criteria : There is no significant difference between before and after change.

Products	S.S	PKG-BI		Final Test		Yield (%)
		PASS	Fail	PASS	Fail	
non-EPI (After change)	2963	2963	0	2963	0	100
EPI (Before change)	2955	2955	0	2955	0	100

We confirmed that there was no yield drop due to change of wafer specifications and there was no significant difference between before and after change. We confirmed that initial defect samples of non-EPI wafers were sufficiently able to be rejected at the same stress condition as Epi wafers in Wafer Test.

Electrical Distribution Results:

We confirmed the electrical distribution results at 4 temperatures (-40°C, +25°C, +105°C, +125°C) and confirmed no significant difference between non-EPI and EPI products. Cpk for all parameters is > 1.67.

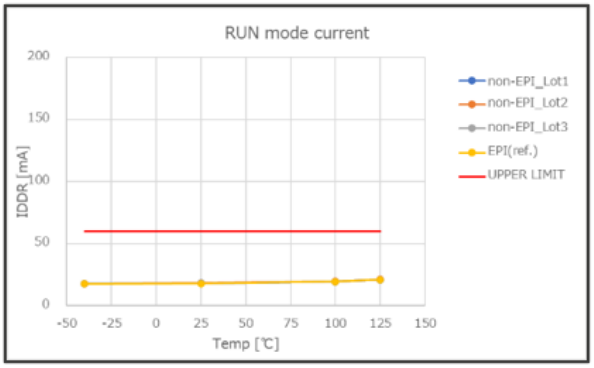
[DC parameter Ta= 25℃]
REGVCC=EVCC=VPOC to 5.5V, BVCC=VPOC to REGVCC, A0VREF=3.0V to 5.5V, A1VREF=3.0V to 5.5V, AW0VSS=IS0VSS=EVSS=BVSS=A0VSS=A1VSS=0V

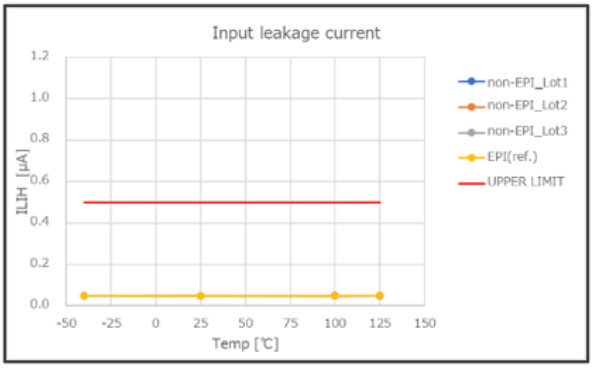
Parameter	Symbol			UNIT	UPPER LIMIT	LOWER LIMIT	non-EPI_Lot1,30pcs AVERAGE	SIGMA	Cpk	non-EPI_Lot2,30pcs AVERAGE	SIGMA	Cpk	non-EPI_Lot3,30pcs AVERAGE	SIGMA	Cpk	EPI(ref.),30pcs AVERAGE	SIGMA	Cpk
High level input voltage	VIH	CMOS		V	1.95	-	1.47	0.004	41.28	1.46	0.003	59.98	1.47	0.004	38.21	1.46	0.003	49.04
		SHMT1 (except FLMD0 pin)		V	1.95	-	1.79	0.005	10.03	1.79	0.009	5.97	1.79	0.006	8.50	1.79	0.006	8.55
		SHMT1 (FLMD0 pin)		V	1.98	-	1.84	0.011	4.21	1.83	0.011	4.56	1.84	0.009	5.42	1.84	0.008	6.18
		SHMT2		V	2.25	-	1.92	0.010	10.62	1.92	0.010	11.17	1.93	0.010	10.69	1.92	0.012	9.22
		SHMT4		V	2.40	-	2.09	0.006	16.75	2.09	0.007	15.62	2.09	0.007	15.11	2.09	0.007	14.43
		TTL		V	2.20	-	1.18	0.005	66.57	1.18	0.006	58.80	1.19	0.005	67.78	1.19	0.006	57.72
		IP0_0 pin		V	2.10	-	1.27	0.005	57.41	1.27	0.004	64.32	1.28	0.007	38.16	1.28	0.006	42.97
Low level input voltage	VIL	CMOS		V	-	1.05	1.45	0.005	28.23	1.45	0.003	47.24	1.45	0.006	23.84	1.45	0.003	45.56
		SHMT1		V	-	1.05	1.17	0.005	8.70	1.17	0.007	5.72	1.17	0.006	6.47	1.17	0.005	7.83
		SHMT2		V	-	0.75	1.03	0.007	13.96	1.03	0.007	13.91	1.03	0.007	13.22	1.03	0.006	15.88
		SHMT4		V	-	1.50	1.76	0.004	29.31	1.75	0.006	15.42	1.76	0.006	13.52	1.76	0.004	23.63
		TTL		V	-	0.80	1.18	0.005	27.93	1.17	0.006	21.46	1.18	0.006	20.46	1.17	0.005	24.02
		IP0_0 pin		V	-	0.90	1.28	0.005	28.40	1.27	0.004	34.68	1.28	0.007	19.20	1.28	0.006	20.11
High level output voltage	VOH	Fast mode	IOH=-5mA (6pin)	V	-	2.00	2.91	0.002	179.07	2.91	0.002	134.57	2.91	0.002	134.29	2.91	0.001	192.05
			IOH=-3mA (10pin)	V	-	2.00	2.89	0.001	211.69	2.89	0.001	211.78	2.89	0.001	211.52	2.89	0.001	296.64
			IOH=-1mA (16pin)	V	-	2.50	2.94	0.001	148.13	2.95	0.001	148.36	2.94	0.001	123.44	2.94	0.001	185.17
			IOH=-0.1mA (16pin)	V	-	2.50	2.99	0.001	205.75	2.99	0.001	274.48	2.99	0.001	225.30	2.99	0.001	329.33
		Slow mode	IOH=-1mA (16pin)	V	-	2.50	2.89	0.001	126.91	2.89	0.002	84.87	2.89	0.002	84.61	2.89	0.001	127.07
			IOH=-0.1mA (16pin)	V	-	2.50	2.99	0.001	325.33	2.99	0.001	325.24	2.99	0.001	325.33	2.99	0.001	325.33
Low level output voltage	VOL	Fast mode	IOL= 5mA (6pin)	V	0.40	-	0.13	0.002	59.88	0.13	0.003	36.04	0.13	0.002	52.59	0.13	0.001	81.92
			IOL= 3mA (10pin)	V	0.40	-	0.08	0.001	89.81	0.08	0.002	63.45	0.08	0.001	89.46	0.08	0.001	216.00
			IOL= 1mA (16pin)	V	0.40	-	0.04	0.000	303.39	0.04	0.001	151.81	0.04	0.001	173.40	0.04	0.001	202.33
		Slow mode	IOL= 1mA (16pin)	V	0.40	-	0.08	0.001	152.51	0.08	0.001	106.98	0.08	0.001	118.42	0.08	0.001	106.91
Internal pull-up resistance	RU	except FLMD0 pin		kΩ	100	20	28.18	0.26	10.36	27.94	0.36	7.34	28.31	0.32	8.86	27.97	0.22	12.29
		FLMD0 pin		kΩ	36	4	14.58	0.11	31.05	14.46	0.16	21.68	14.67	0.13	27.53	14.49	0.10	33.56
Internal pull-down resistance	RD	except FLMD0 pin		kΩ	100	20	30.08	0.21	15.66	30.10	0.29	11.74	30.35	0.21	16.08	30.04	0.15	22.36
		FLMD0 pin		kΩ	36	-4	15.91	0.13	30.71	15.83	0.15	26.25	16.02	0.12	34.12	15.88	0.12	34.27
Input leakage current	ILIH	VI=REGVCC	IP0_0 pin	μA	0.50	-	0.049	0.002	93.92	0.049	0.002	100.30	0.049	0.001	107.32	0.049	0.001	136.55
		VI=EVCC	RESET,FLMD0,IP0,P0,P1,P2,P8,P9,P20 pin	μA	0.50	-	0.000	0.001	277.67	0.000	0.001	277.67	0.000	0.001	333.24	0.000	0.001	333.24
		VI=BVCC	P10, P11, P12, P18 pin	μA	0.50	-	0.000	0.001	333.24	0.000	0.000	416.61	0.000	0.001	237.97	0.000	0.001	333.24
		VI=A0VREF	AP0	μA	0.50	-	0.000	0.001	208.19	0.000	0.001	237.97	0.000	0.001	208.17	0.000	0.001	208.19
		VI=A1VREF	AP1	μA	0.50	-	0.000	0.010	16.67	0.000	0.001	237.97	0.000	0.001	277.74	0.000	0.010	16.67
	ILIL	VI=0	IP0_0 pin	μA	-	-0.50	-0.034	0.001	155.49	-0.033	0.002	103.87	-0.033	0.002	103.78	-0.033	0.001	141.39
		VI=0	RESET,FLMD0,IP0,P0,P1,P2,P8,P9,P20 pin	μA	-	-0.50	0.000	0.010	16.67	0.000	0.000	416.72	0.000	0.000	416.61	0.000	0.010	16.67
		VI=0	P10, P11, P12, P18 pin	μA	-	-0.50	0.000	0.001	333.33	0.000	0.000	416.72	0.000	0.000	416.61	0.000	0.000	416.72
		VI=0	AP0	μA	-	-0.50	0.001	0.001	166.96	0.000	0.001	208.50	0.001	0.001	166.93	0.001	0.001	166.91
		VI=0	AP1	μA		-0.50	0.000	0.001	333.42	0.000	0.001	333.33	0.000	0.000	416.72	0.000	0.010	16.67
RUN mode current	IDDR	fCPUCLK=80MHz@PLL	All peripheral is running	mA	80	-	18.23	0.19	73.29	18.38	0.28	49.08	18.22	0.21	66.92	18.02	0.16	85.53
HALT mode current	IDDH	fCPUCLK=80MHz@PLL	All peripheral is running	mA	56	-	15.76	0.14	98.86	15.92	0.22	61.09	15.78	0.15	92.08	15.62	0.10	138.76
STOP mode current	IDDS	fCPUCLK is stopping	All peripheral is stopping	mA	21	-	0.36	0.01	928.62	0.37	0.01	991.26	0.36	0.01	1064.01	0.36	0.01	1134.77
DeepSTOP mode current	IDDDS	fCPUCLK is power off	All peripheral is stopping.Isolated area Power Off	μA	1270	-	36.97	1.01	440.89	38.12	1.48	300.09	36.60	1.07	415.29	37.07	1.14	388.80
Cyclic RUN mode current	IDDCR	fCPUCLK=HS IntOSC		mA	40	-	2.32	0.03	440.71	2.35	0.04	318.49	2.33	0.03	461.64	2.30	0.02	584.45
Cyclic STOP mode current	IDDCS	fCPUCLK is stopping		mA	32	-	0.79	0.02	688.93	0.81	0.02	658.05	0.79	0.01	737.72	0.79	0.01	800.19

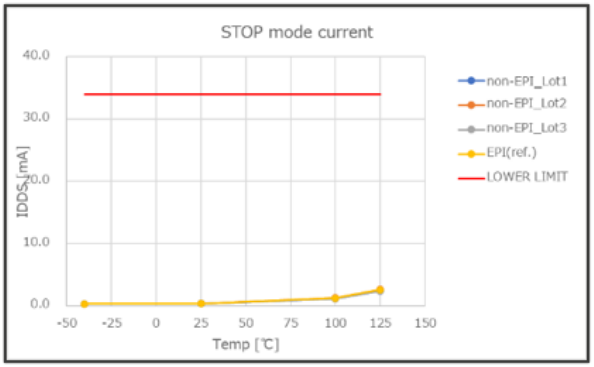
Example of electrical distribution at +25°C

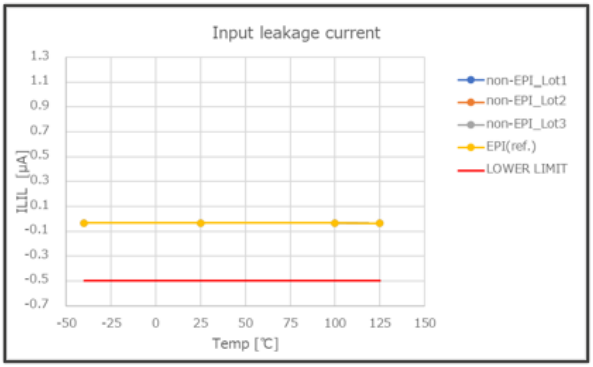
Electrical Characteristics:

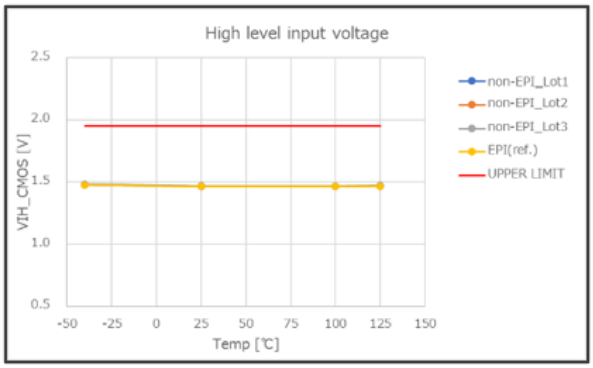
We confirmed that there was no significant difference in electrical characteristics between EPI and non-EPI products.

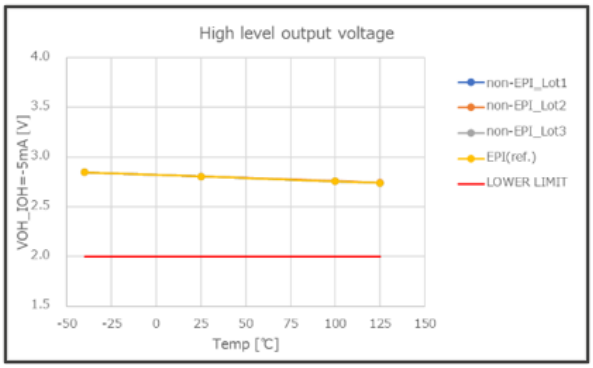


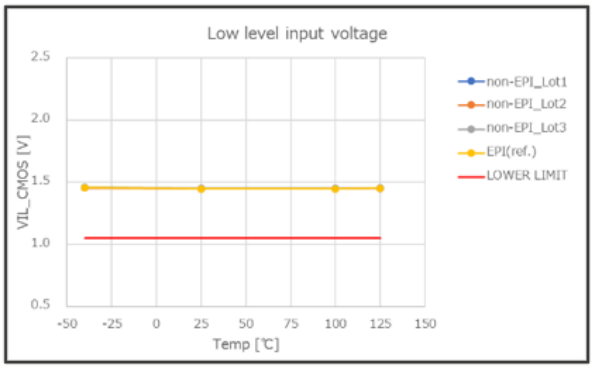


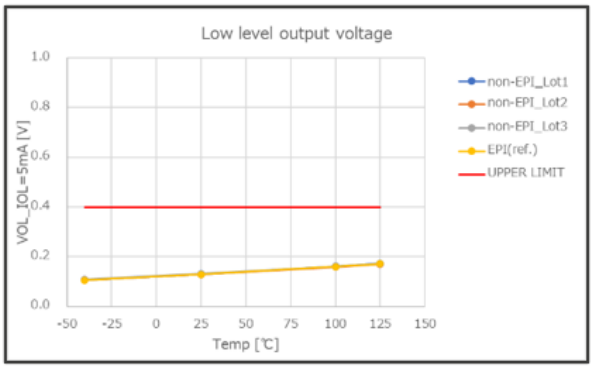












◆Products：RH850/F1L-2M　◆PKG：176pin QFP　◆ASSY：RSC

Reliability Evaluation Results:

ESD and LATCH-UP results:

The following table shows ESD/LATCH-UP Test results for EPI/non-EPI wafers. The results of ESD and LATCH-UP Test between wafer specifications were equivalent and there were no problems.

Test type	Target specification	Number of sample	EPI wfr. of N3	non-EPI wfr. of N3
HBM	AEC-Q100 +/- 2000V	3pcs	OK	OK
CDM	AEC-Q100 +/- 500V (All pin)	3pcs	OK	OK
Latch-up	AEC-Q100 +/- 100mA	6pcs	OK	OK

Reliability impact confirmation:

We completed TEG evaluation about extracted concern items based on addition of Si-wafer specifications.
We confirmed that non-Epi products were equivalent to Epi products in all items through TEG evaluation.

Change items	Change points	Concern items	Confirmation items	Confirmation results (EPI <-> non-EPI difference)
Impact on reliability due to addition of Si-Wafer specifications (EPI -> non-EPI)	Increase in crystal defects, impurities and precipitates in crystals and deterioration in gettering capability due to decrease in BMD*1 density	Change in reliability (Breakdown-voltage characteristics) of Gate-Oxide films	TDDB	We confirmed that there was no significant difference.
			TZDB	We confirmed that there was no significant difference.
		Changes in reliability (Retention characteristics) of Tunnel-Oxide films	HCI	We confirmed that there was no significant difference.
			NBTI	We confirmed that there was no significant difference.
			SILC/TDDB	We confirmed that there was no significant difference.

*1 Bulk Micro Defects: Crystal defects due to Oxygen precipitation

Product List

R7F7010023AFP#AA4	R7F7010184AFP#KA4
R7F7010023AFP#BA4	R7F7010214AFP#KA4
R7F7010023AFP#KA4	R7F7010223AFP#AA4
R7F7010033AFP#AA2	R7F7010233AFP#AA4
R7F7010033AFP#BA2	R7F7010233AFP#BA4
R7F7010033AFP-C#AA2	R7F7010233AFP#KA4
R7F7010073AFP#AA4	R7F7010234AFP#AA4
R7F7010073AFP#BA4	R7F7010243AFP#AA2
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R7F7010114AFP#AA4	R7F7010254AFP#AA2
R7F7010114AFP#KA4	R7F7010283AFP#KA4
R7F7010124AFP#KA4	R7F7010304AFP#AA4
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