Product Change Notification / SYST-29CDIS884

Date:

02-May-2022

Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ERRATA - PIC18(L)F27/47/57K42 Family Silicon Errata and Data Sheet Clarification

Affected CPNs:

SYST-29CDIS884_Affected_CPN_05022022.pdf
SYST-29CDIS884_Affected_CPN_05022022.csv

Notification Text:

SYST-29CDIS884

Microchip has released a new Product Documents for the PIC18(L)F27/47/57K42 Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at PIC18(L)F27/47/57K42 Family Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change: - Added Module 3.3 Double Sample Conversions, 12 Central Processing Unit (CPU), and 12.1 FSR Shadow Registers..

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 2 May 2022

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

PIC18(L)F27/47/57K42 Family Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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SYST-29CDIS884 - ERRATA - PIC18(L)F27/47/57K42 Family Silicon Errata and Data Sheet Clarification

Affected Catalog Part Numbers(CPN)

PIC18F27Q10-E/SP
PIC18F27Q10-E/ML
PIC18F27Q10-E/SS
PIC18F27Q10-E/SO
PIC18F47Q10-E/MP
PIC18F47Q10-E/P
PIC18F27Q10-E/STX
PIC18F47Q10-E/PT
PIC18F27Q10-I/SP
PIC18F27Q10-I/ML
PIC18F27Q10-I/SS
PIC18F27Q10-I/SO
PIC18F47Q10-I/MP
PIC18F47Q10-I/P
PIC18F27Q10-I/STX
PIC18F47Q10-I/PTC01
PIC18F47Q10-I/PT
PIC18F27Q10T-I/ML
PIC18F27Q10T-I/SS
PIC18F27Q10T-I/SO
PIC18F47Q10T-I/MP
PIC18F27Q10T-I/STX
PIC18F47Q10T-I/PTC01
PIC18F47Q10T-I/PT
PIC18F27Q43-E/SP
PIC18F27Q43-E/ML
PIC18F27Q43-E/SS
PIC18F27Q43-E/SO
PIC18F47Q43-E/MP
PIC18F47Q43-E/P
PIC18F27Q43-E/STX
PIC18F47Q43-E/ML
PIC18F47Q43-E/PT
PIC18F27Q43-I/SP
PIC18F27Q43-I/ML
PIC18F27Q43-I/SS
PIC18F27Q43-I/SO
PIC18F47Q43-I/MP
PIC18F47Q43-I/P
PIC18F27Q43-I/STX
PIC18F47Q43-I/ML
PIC18F47Q43-I/PT

PIC18F27Q43T-I/ML
PIC18F27Q43T-I/SS
PIC18F27Q43T-I/SO
PIC18F47Q43T-I/MP
PIC18F27Q43T-I/STX
PIC18F47Q43T-I/ML
PIC18F47Q43T-I/PT
PIC18F27Q83-E/5N
PIC18F27Q84-E/5N
PIC18F27Q83-E/SP
PIC18F27Q84-E/SP
PIC18F27Q83-E/SS
PIC18F27Q84-E/SS
PIC18F27Q83-E/SO
PIC18F27Q84-E/SO
PIC18F47Q83-E/NHX
PIC18F47Q84-E/NHX
PIC18F47Q83-E/P
PIC18F47Q84-E/P
PIC18F47Q83-E/PT
PIC18F47Q84-E/PT
PIC18F27Q83-I/5N
PIC18F27Q84-I/5N
PIC18F27Q83-I/SP
PIC18F27Q84-I/SP
PIC18F27Q83-I/SS
PIC18F27Q84-I/SS
PIC18F27Q83-I/SO
PIC18F27Q84-I/SO
PIC18F47Q83-I/NHX
PIC18F47Q84-I/NHX
PIC18F47Q83-I/P
PIC18F47Q84-I/P
PIC18F47Q83-I/PT
PIC18F47Q84-I/PT
PIC18F27Q83T-I/5N
PIC18F27Q84T-I/5N
PIC18F27Q83T-I/SS
PIC18F27Q84T-I/SS
PIC18F27Q83T-I/SO
PIC18F27Q84T-I/SO
PIC18F47Q83T-I/NHX
PIC18F47Q84T-I/NHX
PIC18F47Q83T-I/PT
PIC18F47Q84T-I/PT
PIC18F27Q84T-E/5N
PIC18F27K40-E/SP

PIC18LF27K40-E/SP
PIC18F27K40-E/ML
PIC18LF27K40-E/ML
PIC18F27K40-E/SS
PIC18LF27K40-E/SS
PIC18F27K40-E/SO
PIC18LF27K40-E/SO
PIC18F47K40-E/P
PIC18LF47K40-E/P
PIC18F47K40-E/MV
PIC18LF47K40-E/MV
PIC18F47K40-E/ML
PIC18LF47K40-E/ML
PIC18F47K40-E/PT
PIC18LF47K40-E/PT
PIC18F27K40-I/SP
PIC18LF27K40-I/SP
PIC18F27K40-I/ML
PIC18LF27K40-I/ML
PIC18F27K40-I/SS
PIC18LF27K40-I/SS
PIC18F27K40-I/SO
PIC18LF27K40-I/SO
PIC18F47K40-I/P
PIC18LF47K40-I/P
PIC18F47K40-I/MV
PIC18LF47K40-I/MV
PIC18F47K40-I/ML
PIC18LF47K40-I/ML
PIC18F47K40-I/PT
PIC18LF47K40-I/PT
PIC18F27K40T-I/ML
PIC18LF27K40T-I/ML
PIC18F27K40T-I/MLV02
PIC18F27K40T-I/MLVAO
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PIC18LF27K40T-I/SS
PIC18F27K40T-I/SSV01
PIC18F27K40T-I/SO
PIC18LF27K40T-I/SO
PIC18F47K40T-I/MV
PIC18LF47K40T-I/MV
PIC18F47K40T-I/ML
PIC18LF47K40T-I/ML
PIC18F47K40T-I/PT
PIC18LF47K40T-I/PT
PIC18F47K40T-E/ML

PIC18LF47K40T-E/PTVAO
PIC18F27K42-E/SP
PIC18LF27K42-E/SP
PIC18F27K42-E/ML
PIC18LF27K42-E/ML
PIC18F27K42-E/MLVAO
PIC18F27K42-E/MX
PIC18LF27K42-E/MX
PIC18F27K42-E/SS
PIC18LF27K42-E/SS
PIC18F27K42-E/SO
PIC18LF27K42-E/SO
PIC18F57K42-E/MV
PIC18LF57K42-E/MV
PIC18F47K42-E/P
PIC18LF47K42-E/P
PIC18F47K42-E/MV
PIC18LF47K42-E/MV
PIC18F47K42-E/ML
PIC18LF47K42-E/ML
PIC18F47K42-E/PT
PIC18LF47K42-E/PT
PIC18F57K42-E/PT
PIC18LF57K42-E/PT
PIC18F27K42-I/SP
PIC18LF27K42-I/SP
PIC18F27K42-I/ML
PIC18LF27K42-I/ML
PIC18F27K42-I/MX
PIC18LF27K42-I/MX
PIC18F27K42-I/SS
PIC18LF27K42-I/SS
PIC18F27K42-I/SO
PIC18LF27K42-I/SO
PIC18F57K42-I/MV
PIC18LF57K42-I/MV
PIC18F47K42-I/P
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PIC18F47K42-I/MV
PIC18LF47K42-I/MV
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PIC18LF27K42T-I/SO
PIC18F57K42T-I/MV
PIC18LF57K42T-I/MV
PIC18F47K42T-I/MV
PIC18LF47K42T-I/MV
PIC18F47K42T-I/ML
PIC18LF47K42T-I/ML
PIC18F47K42T-I/PT
PIC18LF47K42T-I/PT
PIC18F57K42T-I/PT
PIC18LF57K42T-I/PT
PIC18F27K42T-E/ML
PIC18LF27K42T-E/ML
PIC18F27K42T-E/MLV01
PIC18F27K42T-E/MLVAO
PIC18LF27J53-I/SP
PIC18F27J53-I/SP
PIC18LF27J53-I/ML
PIC18F27J53-I/ML
PIC18LF27J53-I/SS
PIC18F27J53-I/SS
PIC18F27J53-I/SO
PIC18LF47J53-I/ML
PIC18F47J53-I/ML
PIC18LF47J53-I/PT
PIC18F47J53-I/PT
PIC18F27J53T-I/ML
PIC18F27J53T-I/SS
PIC18F47J53T-I/ML
PIC18F47J53T-I/PT
PIC18LF27J13-I/SP
PIC18F27J13-I/SP
PIC18LF27J13-I/ML
PIC18F27J13-I/ML
PIC18LF27J13-I/SS
PIC18F27J13-I/SS
PIC18LF27J13-I/SO
PIC18F27J13-I/SO
PIC18LF47J13-I/ML
PIC18F47J13-I/ML
PIC18LF47J13-I/PT

PIC18F47J13-I/PT
PIC18F27J13T-I/ML020
PIC18F27J13T-I/ML021
PIC18F27J13T-I/ML022
PIC18F27J13T-I/ML023
PIC18F27J13T-I/ML024
PIC18F27J13T-I/ML025
PIC18F27J13T-I/ML
PIC18F27J13T-I/MLV01
PIC18F27J13T-I/MLV02
PIC18F27J13T-I/SS
PIC18F47J13T-I/PT

PIC18(L)F27/47/57K42 Family Silicon Errata and Data Sheet Clarification

The PIC18(L)F27/47/57K42 family devices that you have received conform functionally to the current Device Data Sheet (DS40001919**F**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18(L)F27/47/57K42 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A3**).

Data Sheet clarifications and corrections start on page 9, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, contact your local Microchip sales office for assistance.

The DEVREV/REVID values for the various PIC18(L)F27/47/57K42 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID<13:0>(1), (2)	Revision ID for Silicon Revision	
		A1	A3
PIC18F27K42	6C40h	A001	A003
PIC18F47K42	6BE0h	A001	A003
PIC18F57K42	6B80h	A001	A003
PIC18LF27K42	6D80h	A001	A003
PIC18LF47K42	6D20h	A001	A003
PIC18LF57K42	6CC0h	A001	A003

Note 1: The Revision ID is located in addresses 3FFFFCh-3FFFFDh and Device ID is located in addresses 3FFFFEh-3FFFFFh.

2: Refer to the *"PIC18(L)F27/47/57K42 Memory Programming Specification"* (DS40001886) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item No.	Issue Summary	Affected Revisions(1)	
				A1	A3
Electrical Specifications	SMBus 3.0	1.1	SMBus 3.0 logic levels.	X	X
	Min VDD specification for A1 rev	1.2	Device may not work properly at certain voltage levels and temperatures.	X	
	Min VDD specification for LF devices for A3 rev	1.3	LF device may not work properly at certain voltage levels and temperatures.	X	X
	Fixed Voltage Reference (FVR) accuracy	1.4	FVR output tolerance may be higher than specified at temperatures below -20°C.	X	X
Direct Memory Access (DMA)	DMA reads from data EEPROM	2.1	DMA reads from data EEPROM does not operate.	X	
	DMA in Doze mode	2.2	DMA transfers may not work when CPU is in Doze mode.	X	
Analog-to-Digital Converter with Computation (ADC2)	ADC Conversion in FOSC mode	3.1	ADC does not complete conversion successfully in FOSC mode.	X	
	Burst Average mode Double Sampling	3.2	The ADC^2 does not trigger the second conversion when operated in non-continuous double-sampling Burst Average mode.	X	
	Double Sample Conversions	3.3	An unexpected acquisition time is added between the first and second conversions.	X	X
Universal Asynchronous Receiver Transmitter (UART)	BRGS Select	4.1	BRGS Select feature not functional in DALI mode.		X
	Stop bit interrupt flag	4.2	Stop bit interrupt flag functionality not available.	X	
	Auto-baud	4.3	The first character after auto-baud may be corrupted.	X	X
I2C	I^{2}C receive buffer	5.1	Received data is transferred into the I2CxRXB buffer on an incorrect clock edge.	X	X
	I^{2}C Start/Stop Flags	5.2	I^{2}C Start and/or Stop flags maybe set when I^{2}C is enabled.	X	X
Nonvolatile Memory (NVM) Control	WRERR bit functionality	6.1	The WRERR bit cannot be cleared in hardware after being set once.	X	
Windowed Watchdog Timer (WWDT)	WWDT operation in Doze mode	7.1	Window violation occurs when WWDT operated in Doze mode.	X	
Power-Saving Operation Modes	Low-Power Sleep mode	8.1	Low-power Sleep mode does not operate at 3.1V < VDD < 3.3V.	X	
Program Flash Memory (PFM)	Endurance of PFM	9.1	Endurance of PFM is lower than specified.	X	X
Instruction Set	MOVFF/MOVSF instruction	10.1	MOVFF/MOVSF may corrupt destination.	X	X
In-Circuit Debugging (ICD)	Software breakpoints	11.1	Software breakpoints are not available.	X	X
Central Processing Unit (CPU)	FSR Shadow Registers	12.1	FSR Shadow Registers are not writable.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A3**).

1. Module: Electrical Specifications

1.1 SMBus 3.0

The SMBus 3.0 V_{IL} specification (Parameter D305) is temperature and V_{DD} dependent. Refer to the table below.

Temperature	V_{DD}	D305 SMBus 3.0 V_{IL} Specification
-40°C	1.8V	0.6V
-40°C	5.5V	0.8V
25°C	1.8V	0.6V
25°C	5.5V	0.8V
85°C	1.8V	0.6V
85°C	5.5V	0.7V
125°C	1.8V	0.5V
125°C	5.5V	0.7V

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

1.2 Min V_{DD} Specification for A1 Rev

V_{DDMIN} for A1 rev has changed for temperatures below +25°C as shown below in **bold**.

PIC18LF27/47/57K42			Standard Operating Conditions (unless otherwise stated)				
PIC18F27/47/57K42							
Param. No.	Sym.	Characteristic	Min.	Typ.†	Max.	Units	Conditions
Supply Voltage							
D002	V_{DD}		**2.5** 1.8 2.5 2.7	— — — —	3.6 3.6 3.6 3.6	V V V V	$F_{OSC} \leq$ 16 MHz **(-40°C to <+25°C)** $F_{OSC} \leq$ 16 MHz **(≥+25°C to +125°C)** $F_{OSC} >$ 16 MHz and $F_{OSC} \leq$ 32 MHz $F_{OSC} >$ 32 MHz
D002	V_{DD}		**2.5** 2.3 2.5 2.7	— — — —	5.5 5.5 5.5 5.5	V V V V	$F_{OSC} \leq$ 16 MHz **(-40°C to <+25°C)** $F_{OSC} \leq$ 16 MHz **(≥+25°C to +125°C)** $F_{OSC} >$ 16 MHz and $F_{OSC} \leq$ 32 MHz $F_{OSC} >$ 32 MHz

Work around

None.

Affected Silicon Revisions

A1	A3						
X							

1.3 Min VDD Specification for LF Devices for A3 Rev

VDDMIN for A3 rev of LF devices has changed for temperatures below +25°C as shown below in **bold**.

PIC18LF27/47/57K42			Standard Operating Conditions (unless otherwise stated)				
PIC18F27/47/57K42							
Param. No.	Sym.	Characteristic	Min.	Typ.†	Max.	Units	Conditions
Supply Voltage							
D002	VDD		**2.3**	—	3.6	V	FOSC ≤ 16 MHz **(-40°C to <+25°C)**
			1.8	—	3.6	V	FOSC ≤ 16 MHz **(≥+25°C to +125°C)**
			2.5	—	3.6	V	FOSC > 16 MHz and FOSC ≤ 32 MHz
			2.7	—	3.6	V	FOSC > 32 MHz
D002	VDD		2.3	—	5.5	V	FOSC ≤ 16 MHz
			2.5	—	5.5	V	FOSC > 16 MHz and FOSC ≤ 32 MHz
			2.7	—	5.5	V	FOSC > 32 MHz

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

1.4 Fixed Voltage Reference (FVR) Accuracy

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This will apply to all three gain amplifier settings (1X, 2X, 4X). The affected parameter numbers found in the data sheet are: FVR01 (1X gain setting), FVR02 (2X gain setting), and FVR03 (4X gain setting).

Work around

At temperatures above -20°C, the stated tolerances in the data sheet remain in effect. Operate the FVR only at temperatures above -20°C.

Affected Silicon Revisions

A1	A3						
X	X						

2. Module: Direct Memory Access (DMA)

2.1 DMA Reads from Data EEPROM

The DMA modules do not operate when configured to access the data EEPROM (i.e., SMR[1:0] = 1x). The destination gets written to 0x00.

Work around

None. NVMCON reads work as described.

Affected Silicon Revisions

A1	A3						
X							

2.2 DMA in Doze Mode

When the CPU is operated in Doze mode, DMA transfers may not work as expected.

Work around

None.

Affected Silicon Revisions

A1	A3						
X							

3. Module: Analog-to-Digital Converter with Computation (ADC^2)

3.1 ADC Conversion in Fosc Mode

The ADCON0.GO bit remains set and the conversion does not complete successfully when configured to operate in FOSC mode (ADCON0.CS = 0) with FOSC > 40 MHz.

Work around

Use ADCRC as the ADC clock source (ADCON0.CS = 1).

Affected Silicon Revisions

A1	A3						
X							

3.2 Burst Average Mode Double Sampling

When the ADC^2 is operated in Burst Average mode (MD = 0b011 in the ADCON2 register) while enabling non-continuous operation and double-sampling (CONT = 0 in the ADCON0 register and DSEN = 1 in the ADCON1 register), the value in the ADCNT register does not increment beyond 0b1 toward the value in the ADRPT register.

Work around

When operating the ADC^2 in Burst Average mode with double-sampling, enable continuous operation of the module (CONT = 1 in the ADCON0 register) and set the Stop-On-Interrupt bit (SOI in the ADCON3 register). After the interrupt occurs, perform appropriate threshold calculations in the software and retrigger ADC^2 as necessary.

If the CPU is in Low-Power Sleep mode, alternatively the ADC^2 in non-continuous Burst Average mode can be operated with single ADC conversion (DSEN = 0 in the ADCON1 register) compromising noise immunity for lower power consumption by preventing the device from waking up to perform threshold calculations in the software.

Affected Silicon Revisions

A1	A3						
X							

3.3 Double Sample Conversions

When enabling a Double Sample Conversion (DSEN = 1), with no Precharge time (ADPRE = 0) and no Acquisition time (ADACQ = 0), the maximum number of cycles of acquisition time is inserted prior to the second conversion.

The first conversion will be performed as expected with no Precharge time and no Acquisition time. It is only between the first and second conversions where a maximum number of cycles of Acquisition time is performed unexpectedly.

Work around

Method 1: Disable double conversion (DSEN = 0) and perform two single conversions back to back.

Method 2: If adding acquisition time is acceptable, then select no Precharge time, along with the desired Acquisition time.

Affected Silicon Revisions

A1	A3						
X	X						

4. Module: Universal Asynchronous Receiver Transmitter (UART)

4.1 Baud Rate Generator Speed Select

The Baud Rate Generator Speed Select feature (the BRGS bit in the UxCON0 register) in DALI mode is not functional. The Baud Rate Generator always operates at normal speed with 16 baud clocks per bit in DALI mode.

Work around

None.

Affected Silicon Revisions

A1	A3						
	X						

4.2 Stop Bit Interrupt Flag

Stop bit interrupt flag functionality is not available in the CERIF bit in revision A1.

Work around

Use Timer2 with HLT and connect the UART RX port to the timer Reset trigger. Set the time-out period to the desired Stop bit time (for DALI mode, this is equivalent to two Stop bits at 1200 baud = 1.66 ms). When the Stop bit is received, the timer times out notifying end of data.

Affected Silicon Revisions

A1	A3						
X							

4.3 Auto-Baud

When the UART is configured as follows, then the first character received after auto-baud may be corrupted:

- The UBRG registers are cleared.
- The BRGS bit is set (Fast Baud Rate mode).
- The Stop bits are configured for two Stop bits (STP = 0b1x).

Work around

a) In asynchronous modes other than LIN: The transmitter may delay the first character by at least one character period after sending auto-baud.

b) In all asynchronous modes including LIN: Clear the BRGS bit to select the normal baud rate mode.

Affected Silicon Revisions

A1	A3						
X	X						

5. Module: I²C

5.1 I²C Receive Buffer

When receiving data into the receive buffer I2CxRXB, the byte is transferred into the buffer on the 9th rising clock edge rather than the expected 8th falling edge. This causes both the Receive Buffer Full (RXBF) status bit and the Receive Buffer Interrupt Flag (I2CxRXIF) to also be set on the 9th rising clock edge. The Data Write Interrupt (WRIF) and Address Interrupt Flag (ADRIF) will still be set on the 8th falling clock edge. If user software is configured to interrupt (or poll) when either the WRIF bit or the ADRIF bit is set, hardware will read an empty receive buffer, set the Receive Read Error (RXRE) status flag, and a NACK will be issued.

Work around

Do not use WRIF or ADRIF to determine when the receive buffer has received data. Instead, interrupt/poll using the I2CxRXIF interrupt bit or poll the RXBF bit. These bits are correctly set once the address/data byte has been transferred into I2CxRXB.

Affected Silicon Revisions

A1	A3						
X	X						

5.2 I²C Start and/or Stop Flags May be Set When I²C is Enabled

When I²C is enabled, erroneous Start and/or Stop conditions may be detected. This can generate erroneous I²C interrupts if enabled.

Work around

Use the following procedure to correctly detect the Start and Stop conditions:

1. Disable Start and Stop conditions interrupt functions.
2. Enable I²C module.
3. Wait 250 ns + 6 instruction cycles (Fosc/4).
4. Clear the Start and Stop conditions interrupt flags.
5. Enable Start and Stop conditions interrupt functions if used.

```
I2CxPIEbits.SCIE = 0;
I2CxPIEbits.PCIE = 0;
I2CxCON0bits.EN = 1;
Delay();
I2CxPIRbits.SCIF = 0;
I2CxPIRbits.PCIF = 0;
I2CxPIEbits.SCIE = 1;
I2CxPIEbits.PCIE = 1;
```

Affected Silicon Revisions

A1	A3						
X	X						

6. Module: Nonvolatile Memory (NVM) Control

6.1 WRERR Bit Functionality

When a Reset is issued while an NVM high-voltage operation is in progress, the WRERR bit in the NVMCON1 register is set as expected. After clearing the WRERR bit, if a Reset reoccurs, the WRERR bit is set again regardless of whether an NVM operation is in progress or not.

Work around

None.

Affected Silicon Revisions

A1	A3						
X							

7. Module: Windowed Watchdog Timer (WWDT)

7.1 WWDT Operation in Doze Mode

When the CLRWDT instruction is issued in Doze mode, a window violation error occurs in WWDT even though the window is open and armed.

Work around

Do not operate the WWDT in Doze mode.

Affected Silicon Revisions

A1	A3						
X							

8. Module: Power-Saving Operation Modes

8.1 Low-Power Sleep Mode in F Devices

The F device resets when waking up from Sleep while in Low-Power mode (VREGPM = 1 in the VREGCON register) at 3.1V < VDD < 3.3V.

Work around

a) If wake-up from Sleep is needed at 3.1V < VDD < 3.3V, operate the F device in Normal Power mode (VREGPM = 0).

b) If wake-up from Sleep is needed at 3.1V < VDD < 3.3V, enable the Fixed Voltage Reference (EN = 1 in the FVRCON register). This increases the current in Sleep mode by typically 7 µA.

Affected Silicon Revisions

A1	A3						
X							

9. Module: Program Flash Memory (PFM)

9.1 Endurance of PFM

The Flash memory cell endurance specification (Parameter MEM30) is 1K cycles.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

10. Module: Instruction Set

10.1 MOVFF/MOVSF Instruction

When the BSR points to the last bank of the SFR region (BSR = 0x3F) and the low byte of the source or destination address of a MOVFF/MOVSF instruction equals the low byte of an indirect addressing operation register address (INDFx, POSTINCx, POSTDECx, PREINCx, PLUSWx), the operation will not be completed as expected. Either, one or more of the destination, FSR value, or location pointed to by the FSR will be corrupted, or the move will simply not occur.

Work around

Ensure that the BSR does not point to the last bank of the SFR region (BSR = 0x3F) when the MOVFF/MOVSF instruction is being executed.

Affected Silicon Revisions

A1	A3						
X	X						

11. Module: In-Circuit Debugging (ICD)

11.1 Software Breakpoints

When debugging code, software breakpoints will not be available.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

12. Module: Central Processing Unit (CPU)

12.1 FSR Shadow Registers

Writing to the FSR Shadow Registers does not result in accurate values being stored in the registers. Consequently, reading the FSR Shadow Registers after they have been written will return inaccurate data.

Work around

Writes to the FSR shadow registers can be performed safely using the following steps:

1. Save regular FSR2 value into RAM
2. Write the regular FSR2 with the targeted value minus the computed offset (IR[6:0] + 1, see below)
3. Write the shadow FSRxL (data doesn't matter), this will clock the shadow FSR with the FSR computed offset value.
4. Decrement FSR2 value by 1 since FSRxH increments the address by 1 (IR[6:0])
5. Write FSRxH
6. Restore the regular FSR2 from the stored RAM value.

The FSR shadow should have the value desired and the regular FSR should have the original value.

Affected Silicon Revisions

A1	A3						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001919**F**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev F Document (04/2022)

Added Module 3.3 Double Sample Conversions, 12 Central Processing Unit (CPU), and 12.1 FSR Shadow Registers..

Rev E Document (09/2021)

Added Module 5.2 I^2C Start/Stop Flags.

Rev D Document (02/2021)

Added Module 11.1 Software Breakpoints. Minor corrections.

Rev C Document (06/2019)

Added Modules 1.4 Fixed Voltage Reference (FVR) Accuracy and 5.1 I^2C Receive Buffer.

Rev B Document (03/2019)

Added silicon rev A3. Added Modules 1.3: Min V_{DD} Specification for LF Devices for A3 Rev, 2.2: DMA in Doze mode, 4: UART, 5: NVM Control, 6: WWDT, 7: Power-Saving Operation Modes, 8: PFM, and 9: Instruction Set.

Updated Module 1.2: Min VDD Specification for A1 Rev. Updated Table 2.

Data Sheet Clarifications: Removed Module 1.

Rev A Document (01/2018)

Initial release of this document.

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