Product Change Notification / SYST-27OHRV327

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Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ERRATA - PIC18(L)F24/25K42 Silicon Errata and Data Sheet Clarification

Affected CPNs:

SYST-27OHRV327_Affected_CPN_04282022.pdf
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Notification Text:

SYST-27OHRV327

Microchip has released a new Product Documents for the PIC18(L)F24/25K42 Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at PIC18(L)F24/25K42 Silicon Errata and Data Sheet Clarification.

Notification Status: Final
Description of Change: 1. Added Modules 2.5 Double Sample Conversions; 13 Central Processing Unit (CPU); and 13.1 FSR Shadow Registers.

Impacts to Data Sheet: None
Reason for Change: To Improve Productivity
Change Implementation Status: Complete
Date Document Changes Effective: 28 April 2022
NOTE: Please be advised that this is a change to the document only the product has not been changed.
Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

PIC18(L)F24/25K42 Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

PIC18F24K42-E/5NV03
PIC18F24K42-E/SP
PIC18F25K42-E/SP
PIC18LF24K42-E/SP
PIC18LF25K42-E/SP
PIC18F24K42-E/ML
PIC18F25K42-E/ML
PIC18LF24K42-E/ML
PIC18LF25K42-E/ML
PIC18F24K42-E/MLV02
PIC18F24K42-E/SS
PIC18F25K42-E/SS
PIC18LF24K42-E/SS
PIC18LF25K42-E/SS
PIC18F24K42-E/SSV01
PIC18F25K42-E/SSVAO
PIC18F24K42-E/SSVAO
PIC18F24K42-E/SO
PIC18F25K42-E/SO
PIC18LF24K42-E/SO
PIC18LF25K42-E/SO
PIC18F24K42-E/MV
PIC18F25K42-E/MV
PIC18LF24K42-E/MV
PIC18LF25K42-E/MV
PIC18F24K42-I/SP
PIC18F25K42-I/SP
PIC18LF24K42-I/SP
PIC18LF25K42-I/SP
PIC18F24K42-I/ML
PIC18F25K42-I/ML
PIC18LF24K42-I/ML
PIC18LF25K42-I/ML
PIC18F24K42-I/SS
PIC18F25K42-I/SS
PIC18LF24K42-I/SS
PIC18LF25K42-I/SS
PIC18F24K42-I/SO
PIC18F25K42-I/SO
PIC18LF24K42-I/SO
PIC18LF25K42-I/SO
PIC18F24K42-I/MV
PIC18F25K42-I/MV
PIC18LF24K42-I/MV
PIC18LF25K42-I/MV
PIC18F24K42T-I/ML

PIC18F25K42T-I/ML
PIC18LF24K42T-I/ML
PIC18LF25K42T-I/ML
PIC18F24K42T-I/SS
PIC18F25K42T-I/SS
PIC18LF24K42T-I/SS
PIC18LF25K42T-I/SS
PIC18F24K42T-I/SO
PIC18F25K42T-I/SO
PIC18LF24K42T-I/SO
PIC18LF25K42T-I/SO
PIC18F24K42T-I/MV
PIC18F25K42T-I/MV
PIC18LF24K42T-I/MV
PIC18LF25K42T-I/MV
PIC18F24K42T-E/5NV03
PIC18F24K42T-E/SS020
PIC18F24K42T-E/SS
PIC18F25K42T-E/SSVAO
PIC18F24K42T-E/SSVAO
PIC18F24K42T-E/MV

PIC18(L)F24/25K42

PIC18(L)F24/25K42 Silicon Errata and Data Sheet Clarification

The PIC18(L)F24/25K42 devices that you have received conform functionally to the current Device Data Sheet (DS40001869**E**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18(L)F24/25K42 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A4**).

Data Sheet clarifications and corrections start on page 13, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18(L)F24/25K42 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID<13:0>(1), (2)	Revision ID for Silicon Revision		
		A1	A2	A4
PIC18F24K42	6CA0h	A001	A002	A004
PIC18LF24K42	6DE0h	A001	A002	A004
PIC18F25K42	6C80h	A001	A002	A004
PIC18LF25K42	6DC0h	A001	A002	A004

Note 1: The Revision ID is located in addresses 3FFFFCh-3FFFFDh and the Device ID is located in addresses 3FFFFEh-3FFFFFh.

2: Refer to the *"PIC18(L)F24/25K42 Memory Programming Specification"* (DS40001836) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item No.	Issue Summary	Affected Revisions(1)		
				A1	A2	A4
Direct Memory Access (DMA)	Hard stop	1.1	Stopping DMA transfers by clearing EN (DMAxCON0 register).	X		
	DMA in Doze mode	1.2	DMA transfers may not work when CPU is in Doze mode.	X	X	X
Analog-to-Digital Converter with Computation (ADC2)	ADC RC oscillator	2.1	ADC RC oscillator not functional.	X		
	ADC conversion	2.2	The 12-bit ADC shorts briefly at the beginning of the ADC conversion stage.	X		
	Burst Average mode Double Sampling	2.3	The ADC^2 does not trigger the second conversion when operated in non-continuous double-sampling Burst Average mode.	X	X	X
	ADC conversion in FOSC mode	2.4	ADC does not complete conversion successfully in FOSC mode.	X	X	
	Double Sample Conversions	2.5	An unexpected acquisition time is added between the first and second conversions.	X	X	X
Universal Asynchronous Receiver Transmitter (UART)	Flow control PPS	3.1	Flow control affected by PPS.	X	X	X
	Flow control transmit driver	3.2	Flow control transmit driver enable (TXDE) is low true.	X		
	DALI mode auto-baud	3.3	DALI mode always auto-bauds on the Start bit.	X		
	BRGS select	3.4	BRGS select feature not functional in DALI mode.		X	X
	Stop bit interrupt flag	3.5	Stop bit interrupt flag functionality not available.	X		
	DMX mode make after break	3.6	Make after Break period is less than required by the DMX specification.	X		
	RXIDL Status bit	3.7	RXIDL remains clear after auto-baud overflow.	X		
	TXMTIF interrupt flag	3.8	TXMTIF flag is delayed by two instruction cycles.	X		
	Auto-baud	3.9	The first character after auto-baud may be corrupted.	X	X	X
I2C	Multi-Host mode transmission	4.1	Multi-Host mode transmission.	X		
	10-bit Host mode reception	4.2	Automatic restart in 10-bit Host reception.	X	X	X
	NACKIF interrupt flag	4.3	Operation of the NACKIF flag.	X		
	Auto-count	4.4	Auto-count feature in Host Reception mode.	X	X(2)	X(2)
	TXIF interrupt flag	4.5	The TXIF flag is set for 7/10 bit reads when ADBDIS = 1.	X	X(2)	X(2)
	I^{2}C receive buffer	4.6	Received data is transferred into the I2CxRXB buffer on an incorrect clock edge.	X	X	X
	I^{2}C Start/Stop Flags	4.7	I^{2}C Start and/or Stop flags may be set when I^{2}C is enabled.	X	X	X
Program Flash Memory	Endurance of PFM cell for LF devices	5.1	Endurance of the PFM cell is lower than specified.	X	X	X

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item No.	Issue Summary	Affected Revisions(1)		
				A1	A2	A4
Signal Measurement Timer (SMT)	MFINTOSC clock sources into SMT	6.1	MFINTOSC clock sources into the SMT are not functional.	X	X	X
Electrical Specifications	SMBus 2.0	7.1	SMBus 2.0 logic levels.	X		
	SMBus 3.0	7.2	SMBus 3.0 logic levels.	X	X	X
	Min V_{DD} specification	7.3	Device may not work properly at certain voltage levels and temperatures.	X	X	X
	Fixed Voltage Reference (FVR) accuracy	7.4	FVR output tolerance may be higher than specified at temperatures below -20°C.	X	X	X
Nonvolatile Memory (NVM) Control	The WRERR bit functionality	8.1	The WRERR bit cannot be cleared in hardware after being set once.	X	X	X
Windowed Watchdog Timer (WWDT)	WWDT operation in Doze mode	9.1	Window violation occurs when WWDT operated in Doze mode.	X	X	X
Power-Saving Operation Modes	Low-Power Sleep mode	10.1	Low-Power Sleep mode does not operate at 3.1V < V_{DD} < 3.3V.	X	X	
Instruction Set	MOVFF/MOVSF instruction	11.1	MOVFF/MOVSF may corrupt destination.	X	X	X
In-Circuit Debugging (ICD)	Software breakpoints	12.1	Software breakpoints are not available.	X	X	X
Central Processing Unit (CPU)	FSR Shadow Registers	13.1	FSR Shadow Registers are not writable.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

2: I^2C issues exist only in 10-bit Addressing mode. Fixed in 7-bit Addressing mode.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

1. Module: Direct Memory Access (DMA)

1.1 Hard Stop

When a DMA transaction is stopped in the middle of the transfer (the XIP bit is set) by clearing the Enable bit (hard stop), the destination address can be written to with 0x00. This only happens if the very next cycle (after clearing enable) can provide the DMA access to the SRAM bus.

Work around

Clearing the DGO bit before hard stop will prevent the destination being written to with 0x00.

Affected Silicon Revisions

A1	A2	A4					
X							

1.2 DMA in Doze Mode

When the CPU is operated in Doze mode, DMA transfers may not work as expected.

Work around

None.

Affected Silicon Revisions

A1	A2	A4					
X	X	X					

2. Module: Analog-to-Digital Converter with Computation (ADC^2)

2.1 ADC RC Oscillator

Incorrect ADC operation when using clock supplied from dedicated FRC oscillator (i.e., the CS bit is set in the ADCON0 register).

Work around

Use ADC clock supplied by FOSC for ADC operation.

Affected Silicon Revisions

A1	A2	A4					
X							

2.2 ADC Conversion

At the very beginning of the ADC conversion, the input signal may briefly be pulled to ground, which in turn may take some charge out of the internal Sample-and-Hold capacitor. The problem is more pronounced on inputs with an impedance greater than 1 kOhm.

This issue will be seen when sampling the following internal channel inputs: FVR, DAC, and Temperature Indicator and when sampling external sources on an analog pin, including the CVD.

Work around

a) When sampling the internal channel inputs, FVR, DAC, and Temperature Indicator, increase the minimum TAD time to 4 μs to increase accuracy.

b) When sampling an external source through an analog pin, keep the input impedance below 1 kOhm.

c) When using the ADC in CVD mode, there is no work around.

Affected Silicon Revisions

A1	A2	A4					
X							

2.3 Burst Average Mode Double Sampling

When the ADC^2 is operated in Burst Average mode (MD = 0b011 in the ADCON2 register) while enabling non-continuous operation and double-sampling (CONT = 0 in the ADCON0 register and DSEN = 1 in the ADCON1 register), the value in the ADCNT register does not increment beyond 0b1 toward the value in the ADRPT register.

Work around

When operating the ADC^2 in Burst Average mode with double-sampling, enable continuous operation of the module (CONT = 1 in the ADCON0 register) and set the Stop-On-Interrupt bit (SOI in the ADCON3 register). After the interrupt occurs, perform appropriate threshold calculations in the software and retrigger ADC^2 as necessary.

If the CPU is in Low-Power Sleep mode, alternatively the ADC^2 in non-continuous Burst Average mode can be operated with single ADC conversion (DSEN = 0 in the ADCON1 register) compromising noise immunity for lower power consumption by preventing the device from waking up to perform threshold calculations in the software.

Affected Silicon Revisions

A1	A2	A4					
X	X	X					

2.4 ADC Conversion in Fosc Mode

The ADCON0.GO bit remains set and the conversion does not complete successfully when configured to operate in Fosc mode (ADCON0.CS = 0) with Fosc > 40 MHz.

Work around

Use ADCRC as the ADC clock source (ADCON0.CS = 1).

Affected Silicon Revisions

A1	A2	A4					
X	X						

2.5 Double Sample Conversions

When enabling a Double Sample Conversion (DSEN = 1), with no Precharge time (ADPRE = 0) and no Acquisition time (ADACQ = 0), the maximum number of cycles of acquisition time is inserted prior to the second conversion.

The first conversion will be performed as expected with no Precharge time and no Acquisition time. It is only between the first and second conversions where a maximum number of cycles of Acquisition time is performed unexpectedly.

Work around

Method 1: Disable double conversion (DSEN = 0) and perform two single conversions back to back.

Method 2: If adding acquisition time is acceptable, then select no Precharge time, along with the desired Acquisition time.

Affected Silicon Revisions

A1	A2	A4					
X	X	X					

3. Module: Universal Asynchronous Receiver Transmitter (UART)

3.1 Flow Control PPS

Unimplemented PPS input selections for UART1 and UART2 may interfere with hardware flow control when that feature is enabled.

Work around

Set SFRs 0x3AE7 and 0x3AEA to 0x18.

Affected Silicon Revisions

A1	A2	A4					
X	X	X					

3.2 Flow Control Transmit Driver

The TXDE output is active-low, whereas the DE input of RS-485 transceivers need an active-high signal to enable the transmit drivers.

Work around

Use PPS to route TXDE to a pin and then use a CLC module to input and invert the signal on that pin, and use PPS to output that CLC to another pin.

Affected Silicon Revisions

A1	A2	A4					
X							

3.3 DALI Mode Auto-Baud

The auto-baud feature is always enabled in DALI mode in revision A1, regardless of the value of the ABDEN control bit. This will adversely affect data reception when the mid-bit transition of the Manchester data is offset by more than 14%.

Work around

None in revision A1. The auto-baud feature is disabled in DALI mode in revision A2.

Affected Silicon Revisions

A1	A2	A4					
X							

3.4 Baud Rate Generator Speed Select

The Baud Rate Generator Speed Select feature (the BRGS bit in the UxCON0 register) in DALI mode is not functional. The Baud Rate Generator always operates at normal speed with 16 baud clocks per bit in DALI mode.

Work around

When using UART in DALI mode, operate the Baud Rate Generator in normal speed (BRGS = 0) only and use the following formula to calculate the UxBRGH:L register value:

$$UxBRGH:L = \frac{FOSC}{16 \times Desired\ Baud\ Rate} - 1$$

Example: To obtain the desired baud rate of 1200 at FOSC = 64 MHz,

$$UxBRGH:L = \frac{64,000,000}{16 \times 1200} - 1 = 3332$$

Affected Silicon Revisions

A1	A2	A4					
	X	X					

3.5 Stop Bit Interrupt Flag

Stop bit interrupt flag functionality is not available in the CERIF bit in revision A1.

Work around

Use Timer2 with HLT and connect the UART RX port to the timer Reset trigger. Set the time-out period to the desired Stop bit time (for DALI mode, this is equivalent to two Stop bits at 1200 baud = 1.66 ms). When the Stop bit is received, the timer times out notifying end of data.

Affected Silicon Revisions

A1	A2	A4					
X							

3.6 DMX Mode Make After Break

In DMX Console mode, the MAB period is 8 µs. The specification requires a minimum of 12 µs.

Work around

The UART uses only the BREAK time to determine the start of a new frame. Therefore, the short MAB period does not affect DMX operation when using this UART as equipment and no work around is required. However, equipment using other devices for reception may be affected, in which case 8-bit Asynchronous mode must be used with software control of all of the DMX console operations.

Affected Silicon Revisions

A1	A2	A4					
X							

3.7 RXIDL Status Bit

The RXIDL bit properly stays low until the 5th rising edge after auto-baud starts. If auto-baud overflows and is subsequently cleared by software, then RXIDL improperly remains low until the 5th rising edge.

Work around

If RXIDL is low after an auto-baud overflow, then cycle the RXEN or ON bit to restore normal operation.

Affected Silicon Revisions

A1	A2	A4					
X							

3.8 TXMTIF Interrupt Flag

The TXMTIF flag goes low two instruction cycles after the TXB register is written. The bit cannot be polled or interrupt enabled immediately after writing the TXB register.

Work around

Allow at least two instruction cycles after writing TXB before enabling the TXMTIF interrupt or starting to poll the TXMTIF flag.

Affected Silicon Revisions

A1	A2	A4					
X							

3.9 Auto-Baud

When the UART is configured as follows, then the first character received after auto-baud may be corrupted:

- The UBRG registers are cleared.
- The BRGS bit is set (Fast Baud Rate mode).
- The Stop bits are configured for two Stop bits (STP = `0b1x`).

Work around

a) In asynchronous modes other than LIN: The transmitter may delay the first character by at least one character period after sending auto-baud.

b) In all asynchronous modes including LIN: Clear the BRGS bit to select the normal baud rate mode.

Affected Silicon Revisions

A1	A2	A4					
X	X	X					

4. Module: I²C

4.1 Multi-Host Mode Transmission

When the I²C is configured in Multi-Host mode and is operating in Client Transmission mode, writes to the transmit buffer will set the S (Start) bit in the I2CxCON0 register. When the bus becomes free (i.e., BFRE = 1) after client transmission is complete, then the multi-host behaves as a host and initiates a transaction. The host will either send the content of address buffer (ADBDIS = 0) or transmit buffer (ADBDIS = 1).

Work around

Clear the Start bit just before the Stop condition of client transmission occurs; this prevents a false addressing sequence on the I²C Bus.

Affected Silicon Revisions

A1	A2	A4					
X							

4.2 10-Bit Host Mode Reception

When ADBDIS = 1, user software writes to the transmit buffer with the client address. After the addressing sequence is complete, the user software writes the read address to the transmit buffer, while the host is paused for restart (i.e., MDR = 1 & I2CCNT = 0 & MMA = 1). However, a restart does not occur when the transmit buffer is written to.

Work around

The user has to load the transmit buffer and additionally set the S (Start) bit to initiate the restart sequence.

Affected Silicon Revisions

A1	A2	A4					
X	X	X					

4.3 NACKIF Interrupt Flag

The NACKIF flag is set on the client even if the host transmits a non-matching client address.

Work around

Enable NACKIE only when SMA = 1 to avoid unwanted interrupts.

Affected Silicon Revisions

A1	A2	A4					
X							

4.4 Auto-Count

When the ACNT bit in the I2CxCON2 register is set before the host transmits the high address byte, then the MDR bit is set after the 8th SCL pulse, preventing the completion of the addressing sequence.

Work around

Set the ACNT bit after the addressing sequence is complete and when the host is paused for restart (i.e., MDR = 1 & I2CCNT = 0 & MMA = 1).

Affected Silicon Revisions for 7-bit Addressing Mode

A1	A2	A4					
X							

Affected Silicon Revisions for 10-bit Addressing Mode

A1	A2	A4					
X	X	X					

4.5 TXIF Interrupt Flag

When ADBDIS = 1, the address is sent through the transmit buffer. Even if it is a read address, the TXIF flag is set as the data was moved out of the transmit buffer.

Work around

For I²C host read, ignore the TXIF flag if ADBDIS = 1.

Affected Silicon Revisions for 7-bit Addressing Mode

A1	A2	A4					
X							

Affected Silicon Revisions for 10-bit Addressing Mode

A1	A2	A4					
X	X	X					

4.6 I²C Receive Buffer

When receiving data into the receive buffer I2CxRXB, the byte is transferred into the buffer on the 9th rising clock edge rather than the expected 8th falling edge. This causes both the Receive Buffer Full (RXBF) status bit and the Receive Buffer Interrupt Flag (I2CxRXIF) to also be set on the 9th rising clock edge. The Data Write Interrupt (WRIF) and Address Interrupt Flag (ADRIF) will still be set on the 8th falling clock edge. If user software is configured to interrupt (or poll) when either the WRIF bit or the ADRIF bit is set, hardware will read an empty receive buffer, set the Receive Read Error (RXRE) status flag, and a NACK will be issued.

Work around

Do not use WRIF or ADRIF to determine when the receive buffer has received data. Instead, interrupt/poll using the I2CxRXIF interrupt bit or poll the RXBF bit. These bits are correctly set once the address/data byte has been transferred into I2CxRXB.

Affected Silicon Revisions

A1	A2	A4					
X	X	X					

4.7 I²C Start and/or Stop Flags May be Set When I²C is Enabled

When I²C is enabled, erroneous Start and/or Stop conditions may be detected. This can generate erroneous I²C interrupts if enabled.

Work around

Use the following procedure to correctly detect the Start and Stop conditions:

1. Disable Start and Stop conditions interrupt functions.
2. Enable I²C module.
3. Wait 250 ns + 6 instruction cycles (Fosc/4).
4. Clear the Start and Stop conditions interrupt flags.
5. Enable Start and Stop conditions interrupt functions if used.

```
I2CxPIEbits.SCIE = 0;
I2CxPIEbits.PCIE = 0;
I2CxCON0bits.EN = 1;
Delay();
I2CxPIRbits.SCIF = 0;
I2CxPIRbits.PCIF = 0;
I2CxPIEbits.SCIE = 1;
I2CxPIEbits.PCIE = 1;
```

Affected Silicon Revisions

A1	A2	A4					
X	X	X					

5. Module: Program Flash Memory

5.1 Endurance of PFM Cell for LF Devices

The Flash memory cell endurance specification (Parameter MEM30) for PIC18LF24/25K42 devices is 1K cycles.

Work around

None.

Affected Silicon Revisions

A1	A2	A4					
X	X	X					

6. Module: Signal Measurement Timer (SMT)

6.1 MFINTOSC Clock Sources into SMT

The Signal Measurement Timer does not operate when the MFINTOSC is selected as the clock source (i.e., CSEL = 0b100 and 0b101). The MFINTOSC does not start up automatically.

Work around

User software needs to manually enable the MFINTOSC by setting the MFOEN bit in the OSCCEN register. The MFINTOSC will remain enabled as long as the MFOEN bit is set.

Affected Silicon Revisions

A1	A2	A4					
X	X	X					

7. Module: Electrical Specifications

7.1 SMBus 2.0

The SMBus 2.0 V_{IL} specification (Parameter D304) at 125°C is 0.7V.

Work around

None.

Affected Silicon Revisions

A1	A2	A4					
X							

7.2 SMBus 3.0

The SMBus 3.0 V_{IL} specification (Parameter D305) is temperature and V_{DD} dependent. Refer to the table below.

Temperature	V_{DD}	D305 SMBus 3.0 V_{IL} Specification
-40°C	1.8V	0.6V
-40°C	5.5V	0.8V
25°C	1.8V	0.6V
25°C	5.5V	0.8V
85°C	1.8V	0.6V
85°C	5.5V	0.7V
125°C	1.8V	0.5V
125°C	5.5V	0.7V

Work around

None.

Affected Silicon Revisions

A1	A2	A4					
X	X	X					

7.3 Min VDD Specification for LF Devices

VDDMIN for LF devices has changed for temperatures below +25ºC as shown below in **bold**.

PIC18LF24/25K42			Standard Operating Conditions (unless otherwise stated)				
PIC18F24/25K42							
Param. No.	Sym.	Characteristic	Min.	Typ.†	Max.	Units	Conditions
Supply Voltage							
D002	VDD		**2.3** 1.8 2.5 2.7	— — — —	3.6 3.6 3.6 3.6	V V V V	FOSC ≤ 16 MHz **(-40°C to <+25°C)** FOSC ≤ 16 MHz **(≥+25°C to +125°C)** FOSC > 16 MHz and FOSC ≤ 32 MHz FOSC > 32 MHz
D002	VDD		2.3 2.5 2.7	— — —	5.5 5.5 5.5	V V V	FOSC ≤ 16 MHz FOSC > 16 MHz and FOSC ≤ 32 MHz FOSC > 32 MHz

Work around

None.

Affected Silicon Revisions

A1	A2	A4					
X	X	X					

7.4 Fixed Voltage Reference (FVR) Accuracy

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This will apply to all three gain amplifier settings (1X, 2X, 4X). The affected parameter numbers found in the data sheet are: FVR01 (1X gain setting), FVR02 (2X gain setting), and FVR03 (4X gain setting).

Work around

At temperatures above -20°C, the stated tolerances in the data sheet remain in effect. Operate the FVR only at temperatures above -20°C.

Affected Silicon Revisions

A1	A2	A4					
X	X	X					

8. Module: Nonvolatile Memory (NVM) Control

8.1 WRERR Bit Functionality

When a Reset is issued while an NVM high-voltage operation is in progress, the WRERR bit in the NVMCON1 register is set as expected. After clearing the WRERR bit, if a Reset reoccurs, the WRERR bit is set again regardless of whether an NVM operation is in progress or not.

Work around

None.

Affected Silicon Revisions

A1	A2	A4					
X	X	X					

9. Module: Windowed Watchdog Timer (WWDT)

9.1 WWDT Operation in Doze Mode

When the `CLRWDT` instruction is issued in Doze mode, a window violation error occurs in WWDT even though the window is open and armed.

Work around

Do not operate the WWDT in Doze mode.

Affected Silicon Revisions

A1	A2	A4					
X	X	X					

10. Module: Power-Saving Operation Modes

10.1 Low-Power Sleep Mode in F Devices

The F device resets when waking up from Sleep while in Low-Power mode (VREGPM = 1 in the VREGCON register) at 3.1V < VDD < 3.3V.

Work around

a) If wake-up from Sleep is needed at 3.1V < VDD < 3.3V, operate the F device in Normal Power mode (VREGPM = 0).

b) If wake-up from Sleep is needed at 3.1V < VDD < 3.3V, enable the Fixed Voltage Reference (EN = 1 in the FVRCON register). This increases the current in Sleep mode by typically 7 µA.

Affected Silicon Revisions

A1	A2	A4					
X	X						

11. Module: Instruction Set

11.1 MOVFF/MOVSF Instruction

When the BSR points to the last bank of the SFR region (BSR = 0x3F) and the low byte of the source or destination address of a MOVFF/MOVSF instruction equals the low byte of an indirect addressing operation register address (INDFx, POSTINCx, POSTDECx, PREINCx, PLUSWx), the operation will not be completed as expected. Either, one or more of the destination, FSR value, or location pointed to by the FSR will be corrupted, or the move will simply not occur.

Work around

Ensure that the BSR does not point to the last bank of the SFR region (BSR = 0x3F) when the MOVFF/MOVSF instruction is being executed.

Affected Silicon Revisions

A1	A2	A4					
X	X	X					

12. Module: In-Circuit Debugging (ICD)

12.1 Software Breakpoints

When debugging code, software breakpoints will not be available.

Work around

None.

Affected Silicon Revisions

A1	A2	A4					
X	X	X					

13. Module: Central Processing Unit (CPU)

13.1 FSR Shadow Registers

Writing to the FSR Shadow Registers does not result in accurate values being stored in the registers. Consequently, reading the FSR Shadow Registers after they have been written will return inaccurate data.

Work around

Writes to the FSR shadow registers can be performed safely using the following steps:

1. Save regular FSR2 value into RAM
2. Write the regular FSR2 with the targeted value minus the computed offset (IR[6:0] + 1, see below)
3. Write the shadow FSRxL (data doesn't matter), this will clock the shadow FSR with the FSR computed offset value.
4. Decrement FSR2 value by 1 since FSRxH increments the address by 1 (IR[6:0])
5. Write FSRxH
6. Restore the regular FSR2 from the stored RAM value.

The FSR shadow should have the value desired and the regular FSR should have the original value.

Affected Silicon Revisions

A1	A2	A4					
X	X	X					

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001869**E**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Electrical Specifications

Figure 44-5 incorrectly shows the location of parameters OS1, OS2, OS3, OS4, OS5, OS6, OS7, OS8, OS9, OS10, OS20 and OS21. The correct location for the above-mentioned parameters is depicted in the following figure.

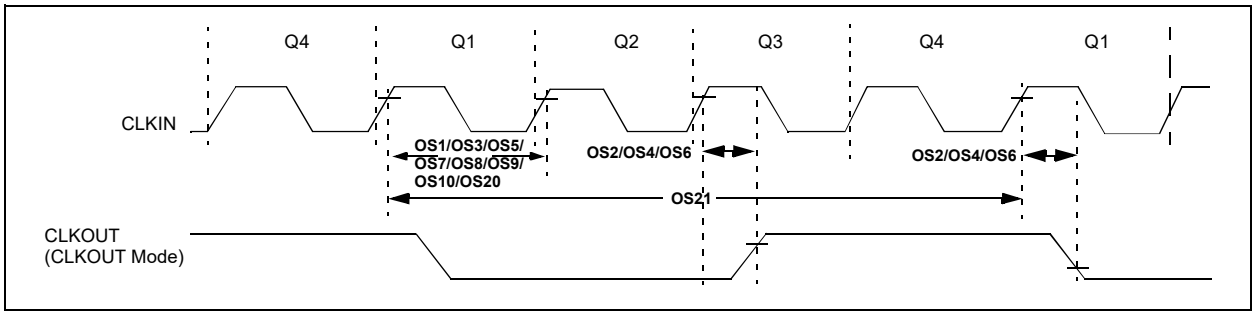

Figure 44-5 Clock Timing

2. Module: Nonvolatile Memory (NVM) Control

Section 13.2 incorrectly states the writing access for User IDs. The corrected Section 13.2 is shown below with changes highlighted in **bold**.

2.1 Device Information Area, Device Configuration Area, User ID, Device ID and Configuration Word Access

When REG[1:0] = `0b01` or `0b11` in the NVMCON1 register, the Device Information Area, the Device Configuration Area, the User IDs, Device ID/ Revision ID and Configuration Words can be accessed. Different access may exist for reads and writes (see Table 13-1).

2.1.1 Reading Access

The user can read from these blocks by setting the REG bits to `0b01` or `0b11`. The user needs to load the address into the TBLPTR registers. Executing a `TBLRD` instruction after that moves the byte pointed to the TABLAT register. The CPU operation is suspended during the read and resumes after. When read access is initiated on an address outside the parameters listed in Table 13-1, the TABLAT register is cleared, reading back '`0`'s.

2.1.2 Writing Access

Only the User IDs and CONFIG words have write access enabled. The user can write to these blocks by setting the REG bits to `0b01` or `0b11`.

The WREN bit in NVMCON1 must be set to enable writes. This prevents accidental writes to the **User IDs/** CONFIG words due to errant (unexpected) code execution. WREN must be kept clear at all times, except when updating the **User IDs/**CONFIG words. WREN is not cleared by hardware. The WR bit will be inhibited from being set unless the WREN bit is set.

2.1.2.1 Writing to CONFIG Words

The user needs to load the TBLPTR and TABLAT registers with the address and data byte respectively before executing the write command. An unlock sequence needs to be followed for writing to the **CONFIG** words (Section 13.1.4, NVM Unlock Sequence). If WRTC = `0` or if TBLPTR points to an invalid address location (see Table 13-1), the WR bit is cleared without any effect and WRERR is set.

A single CONFIG word byte is written at once and the operation includes an implicit erase cycle for that byte (it is not necessary to set FREE). CPU execution is stalled and, at the completion of the write cycle, the WR bit is cleared in hardware and the NVM Interrupt Flag (NVMIF) bit is set. The new CONFIG value takes effect when the CPU resumes operation.

2.1.2.2 Writing to User IDs

The user needs to load the TBLPTR and TABLAT registers with the address and data byte respectively. Writing to the User IDs does not include an implicit erase cycle like the EEPROM/ CONFIG words. Hence, the user needs to clear the memory location pointed by TBLPTR, first by setting the FREE bit and executing the write command. An unlock sequence is required before setting the writing command. A single User ID byte is cleared at once (set to `0xFF`). CPU execution is stalled and, at the completion of the write cycle, the WR bit is cleared in hardware, the NVM Interrupt Flag (NVMIF) bit is set and the CPU resumes operation.

Once the User ID byte is cleared, the user can now write the new value to that location. To do this, the user needs to execute the `TBLWT` instruction followed by executing the write command. An unlock sequence is required before setting the writing command. A single User ID byte is written at once. CPU execution is stalled and, at the completion of the write cycle, the WR bit is cleared in hardware and the NVM Interrupt Flag (NVMIF) bit is set. The new User ID value takes effect when the CPU resumes operation.

During the above operations, if TBLPTR points to an invalid address location (see Table 13-1), the WR bit is cleared without any effect and WRERR is set.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev J Document (04/2022)

Added Modules 2.5 Double Sample Conversions; 13 Central Processing Unit (CPU); and 13.1 FSR Shadow Registers.

Rev H Document (09/2021)

Added Module 4.7 I^2C Start/Stop Flags.

Rev G Document (02/2021)

Added Module 12.1 Software Breakpoints.

Data Sheet Clarifications:

Changed Module DC and AC Characteristics Graphs and Charts to Electrical Specifications. Changed figure 45-20 to 44-5. Added Module Nonvolatile Memory (NVM) Control.

Minor corrections.

Rev F Document (10/2019)

Added Silicon Revision A4. Added Modules 2.4 ADC Conversion; 3.9 Auto-Baud; 4.6 I^2C Receive Buffer; and 11.1 `MOVFF/MOVSF` Instruction.

Data Sheet Clarifications:

DC and AC Characteristics Graphs and Charts: Correction to Figure 45-20 I_{DD}, HFINTOSC Doze Mode, F_{OSC} = 16 MHz, PIC18F24/25K42 Only.

Rev E Document (11/2018)

Remove A2 from Affected Silicon Revisions in ADC Conversion.

Rev D Document (11/2018)

Added Modules 1.2: DMA in Doze Mode; 2.2 ADC Conversion; and 2.3 Burst Average Mode Double Sampling. Added new Modules 8: NVM Control, 9: WWDT, and 10: Power-Saving Operation Modes.

Updated 3.4.

Rev C Document (02/2018)

Added Silicon Revision A2. Added 3.4 Baud Rate Generator Speed Select; 3.5 Stop Bit Interrupt Flag – renumbered sections.

Other minor corrections.

Rev B Document (07/2017)

Added Module 6: SMT and Module 7: Electrical Specifications for LF Devices Only to Silicon Errata Issues. Other minor corrections.

Rev A Document (01/2017)

Initial release of this document.

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