Product Change Notification / SYST-15NFVY812

Date:

28-Mar-2022

Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ERRATA - PIC18F6527/6622/8527/8622 Rev. A1 Silicon Errata Document Revision

Affected CPNs:

SYST-15NFVY812_Affected_CPN_03282022.pdf
SYST-15NFVY812_Affected_CPN_03282022.csv

Notification Text:

SYST-15NFVY812

Microchip has released a new Product Documents for the PIC18F6527/6622/8527/8622 Rev. A1 Silicon Errata of devices. If you are using one of these devices please read the document located at PIC18F6527/6622/8527/8622 Rev. A1 Silicon Errata.

Notification Status: Final

Description of Change: Added Revision ID A1.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 28 Mar 2022

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

PIC18F6527/6622/8527/8622 Rev. A1 Silicon Errata

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

PIC18F6527-I/PT
PIC18F6527T-E/PTV04
PIC18F6527T-I/PT
PIC18F6622-E/PT
PIC18F6622-I/PT
PIC18F6622-I/PTC06
PIC18F6622-I/PTREL
PIC18F6622-I/PTV02
PIC18F6622T-E/PTV03
PIC18F6622T-I/PT
PIC18F6622T-I/PTC06
PIC18F8527-I/PT
PIC18F8527T-I/PT
PIC18F8622-E/PT
PIC18F8622-I/PT
PIC18F8622-I/PTREL
PIC18F8622T-I/PT

PIC18F6527/6622/8527/8622 Rev. A1 Silicon Errata

The PIC18F6527/6622/8527/8622 parts you have received conform functionally to the Device Data Sheet (DS39646**C**), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F6527/6622/8527/8622 devices will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

All of the issues listed here will be addressed in future revisions of the PIC18F6527/6622/8527/8622 silicon.

The following silicon errata apply only to PIC18F6527/6622/8527/8622 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID	
		A0	A1
PIC18F6527	01 0011 010	00000	00001
PIC18F6622	01 0011 100	00000	00001
PIC18F8527	01 0011 011	00000	00001
PIC18F8622	01 0011 101	00000	00001

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

1. Module: A/D

The A/D offset is greater than the specified limit in Table 28-26 of the Device Data Sheet. The updated conditions and limits are shown in **bold** text in Table 1.

Work around

Three work arounds exist.

1. Configure the A/D to use the VREF+ and VREF- pins for the voltage references. This is done by setting the VCFG<1:0> bits (ADCON1<5:4>).
2. Perform a conversion on a known voltage reference voltage and adjust the A/D result in software.
3. Increase system clock speed and adjust A/D settings accordingly. Higher system clock frequencies decrease offset error.

Date Codes that pertain to this issue:

All engineering and production devices.

TABLE 1: A/D CONVERTER CHARACTERISTICS: PIC18F6X27/6X22/8X27/8X22 (INDUSTRIAL, EXTENDED) PIC18LF6X27/6X22/8X27/8X22 (INDUSTRIAL)

Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
A06A	**EOFF**	**Offset Error**	**—**	**—**	**±1.5**	**LSb**	**VREF = VREF+ and VREF-**
A06	**EOFF**	**Offset Error**	—	—	**±3.5**	**LSb**	**VREF = VSS and VDD**

2. Module: EUSART

In Synchronous mode, EUSART baud rates using SPBRGx values of '0' and '1' may not function correctly.

Work around

Use another baud rate configuration to generate the desired baud rate.

3. Module: EUSART

After the last received byte has been read from the EUSART receive buffer, RCREGx, the value is no longer valid for subsequent read operations. The RCREGx register should only be read once for each byte received.

Work around

After each byte is received from the EUSART, store the byte into a user variable. To determine when a byte is available to read from RCREGx, poll the RCIDL (BAUDCONx<6>) bit for a low-to-high transition or use the EUSART Receive Interrupt Flag, RC1IF (PIR1<5>).

4. Module: EUSART

In 9-Bit Asynchronous Full-Duplex Receive mode, received data may be corrupted if the TX9D bit (TXSTAx<0>) is not modified immediately after RCIDL (BAUDCONx<6>) is set.

Work around

Only write to TX9D when a reception is not in progress (RCIDL = 1). No interrupt is associated with RCIDL, therefore, it must be polled in software to determine when TX9D can be updated.

5. Module: ECCP

PIC18F6XXX device's Configuration Word, CONFIG3L, is not unimplemented and will switch the ECCP2 output pin similar to the PIC18F8XXX devices if the Processor mode does not select Microcontroller mode.

Work around

In MPLAB® IDE, program the PIC18F6XXX device as its PIC18F8XXX equivalent and assign the Processor mode bits (PM<1:0>) to '11' for Microcontroller mode.

6. Module: External Memory Bus

For PIC18F8XXX devices, the Stack Pointer may incorrectly increment during a table read operation if the external memory bus wait states are enabled (i.e., Configuration bit, WAIT, is clear (CONFIG3L<7> = 0) and WAIT<1:0> bits (MEMCON<5:4>) are not equal to '11').

Work around

If using the external memory bus and performing TBLRD operations with a non-zero Wait state (CONFIG3L<7> = 0 and WAIT<1:0> (MEMCON<5:4>) are not equal to '11'), disable interrupts by clearing the GIE/GIEH (INTCON<7>) and PEIE/GIEL (INTCON<6>) bits prior to executing any TBLRD operation.

7. Module: MSSP

In SPI mode, the Buffer Full flag (BF bit in the SSPxSTAT register), the Write Collision Detect bit (WCOL bit in SSPxCON1) and the Receive Overflow Indicator bit (SSPOV in SSPxCON1) are not reset upon disabling the SPI module (by clearing the SSPEN bit in the SSPxCON1 register).

For example, if SSPxBUF is full (BF bit is set) and the MSSP module is disabled and re-enabled, the BF bit will remain set. In SPI Client mode, a subsequent write to SSPxBUF will result in a write collision. Also, if a new byte is received, a receive overflow will occur.

Work around

Ensure that if the buffer is full, SSPxBUF is read (thus clearing the BF flag) and WCOL is clear before disabling the MSSP module. If the module is configured in SPI Client mode, ensure that the SSPOV bit is clear before disabling the module.

8. Module: Timer1

In 16-Bit Asynchronous Counter mode or 16-Bit Asynchronous Oscillator mode, the TMR1H and TMR3H buffers do not update when TMRxL is read. This issue only affects reading the TMRxH registers. The timers increment and set the interrupt flags as expected. The Timer registers can also be written as expected.

Work around

Use 8-bit mode by clearing the RD16 (T1CON<7>) bit or use the synchronization option by clearing T1SYNC (T1CON<2>).

9. Module: PORTE

The RE4 pin latch remains at tri-state when the ECCPMX Configuration bit is clear and selects PORTH.

Work around

This issue will be corrected in a future revision of silicon.

10. Module: EUSART

In rare situations, one or more extra zero bytes have been observed in a packet transmitted by the module operating in Asynchronous mode. The actual data is not lost or corrupted; only unwanted (extra) zero bytes are observed in the packet.

This situation has only been observed when the contents of the transmit buffer, TXREGx, are transferred to the TSRx during the transmission of a Stop bit. For this to occur, three things must happen in the same instruction cycle:

- TXREGx is written to;
- the baud rate counter overflows (at the end of the bit period); and
- a Stop bit is being transmitted (shifted out of TSRx).

Work around

If possible, do not use the module's double buffer capability. Instead, load the TXREGx register when the TRMT bit (TXSTAx<1>) is set, indicating the TSRx is empty.

If double-buffering is used and back-to-back transmission is performed, then load TXREGx immediately after TXxIF is set or wait 1-bit time after TXxIF is set. Both solutions prevent writing TXREGx while a Stop bit is transmitted. Note that TXxIF is set at the beginning of the Stop bit transmission.

11. Module: EUSART

When performing back-to-back transmission in 9-bit mode (TX9D bit in the TXSTAx register is set), the second byte may be corrupted if it is written into TXREGx immediately after the TMRT bit is set.

Work around

Execute a software delay, at least one-half the transmission's bit time, after TMRT is set and prior to writing subsequent bytes into TXREGx.

Date Codes that pertain to this issue:

All engineering and production devices.

If transmission is intermittent, then do the following:

- Wait for the TRMT bit to be set before loading TXREGx
- Alternatively, use a free timer resource to time the baud period. Set up the timer to overflow at the end of the Stop bit, then start the timer when you load the TXREGx. Do not load the TXREGx when timer is about to overflow.

Date Codes that pertain to this issue:

All engineering and production devices.

12. Module: EUSART

With the auto-wake-up option enabled by setting the WUE (BAUDCONx<1>) bit, the RCxIF bit will become set on a high-to-low transition on the RXx pin. However, the WUE bit may not clear within 1 TCY of a low-to-high transition on RXx. While the WUE bit is set, reading the receive buffer, RCREGx, will not clear the RCxIF interrupt flag. Therefore, the first opportunity to automatically clear RCxIF by reading RCREGx may take longer than expected.

Note:	RCxIF can only be cleared by reading RCREGx.

Work around

There are two work arounds available:

1. Clear the WUE bit in software, after the wake-up event has occurred, prior to reading the receive buffer, RCREGx.
2. Poll the WUE bit and read RCREGx after the WUE bit is automatically cleared.

Date Codes that pertain to this issue:

All engineering and production devices.

13. Module: MSSP (SPI Mode)

In SPI mode, the SDOx output may change after the inactive clock edge of the bit '0' output. This may affect some SPI components that read data over 300 ns after the inactive edge of SCKx.

Work around

None

Date Codes that pertain to this issue:

All engineering and production devices.

14. Module: MSSP (SPI Mode)

In SPI mode, the Buffer Full Status bit, BF (SSPxSTAT<0>), should not be polled in software to determine when the transfer is complete.

Work around

Copy the SSPxSTAT register into a variable and perform the bit test on the variable. In Example 1, SSPxSTAT is copied into the working register where the bit test is performed (SSP1STAT is shown, but this process is also applicable to SSP2STAT).

EXAMPLE 1:

```
loop_MSB:
    MOVF    SSP1STAT, W
    BTFSS   WREG, BF
    BRA     loop_MSB
```

A second option is to poll the appropriate Master Synchronous Serial Port Interrupt Flag bit, SSPxIF. This bit can be polled and will set when the transfer is complete.

Date Codes that pertain to this issue:

All engineering and production devices.

15. Module: MSSP (SPI Mode)

In SPI Host mode, a write collision may occur if the SSPxBUF register is loaded immediately after a transfer is complete. This may be caused by an inadequate delay between the MSSP Interrupt Flag bit (SSPxIF) or the Buffer Full bit (BF) being set, and SSPxBUF being written to.

This has only been observed when the SPI clock is operating at FOSC/64 or ((Timer2)/2) (SSPxCON1<3:0> = 001x).

Work around

Add a software delay of one SCKx period after detecting the completed transfer, and prior to updating the contents of SSPxBUF.

Also verify that the Write Collision bit (WCOL) is clear after writing SSPxBUF. If WCOL is set, clear the bit in software and rewrite the contents of SSPxBUF.

Date Codes that pertain to this issue:

All engineering and production devices.

16. Module: MSSP (I^2C™ Mode)

In its current implementation, the I^2C Host mode operates as follows:

a) The Baud Rate Generator for I^2C in Host mode is slower than the rates specified in Table 17-3 of the Device Data Sheet.

For this revision of silicon, use the values shown in Table 2 (below) in place of those shown in Table 17-3 of the Device Data Sheet. The differences are shown in **bold** text.

b) Use the following formula in place of the one shown in Register 19-4 (SSPxCON1) of the Device Data Sheet for bit description SSPM3:SSPM0 = 1000.

$$SSPxADD = INT((F_{CY}/F_{SCL}) - (F_{CY}/1.111\ MHz)) - 1$$

Date Codes that pertain to this issue:

All engineering and production devices.

TABLE 2: I^2C™ CLOCK RATE w/BRG

FOSC	FCY	FCY * 2	BRG Value	FSCL (2 Rollovers of BRG)
40 MHz	10 MHz	20 MHz	**0Eh**	400 kHz(1)
40 MHz	10 MHz	20 MHz	**15h**	312.5 kHz
40 MHz	10 MHz	20 MHz	**59h**	100 kHz
16 MHz	4 MHz	8 MHz	**05h**	400 kHz(1)
16 MHz	4 MHz	8 MHz	**08h**	308 kHz
16 MHz	4 MHz	8 MHz	**23h**	100 kHz
4 MHz	1 MHz	2 MHz	**01h**	333 kHz(1)
4 MHz	1 MHz	2 MHz	**08h**	100 kHz
4 MHz	1 MHz	2 MHz	00h	1 MHz(1)

Note 1: The I^2C™ interface does not conform to the 400 kHz I^2C specification (which applies to rates greater than 100 kHz) in all details, but may be used with care where higher rates are required by the application.

17. Module: MSSP (I^2C Mode)

It has been observed that, following a Power-on Reset, I^2C mode may not initialize properly by just configuring the SCLx and SDAx pins as either inputs or outputs. This has only been seen in a few unique system environments.

A test of a statistically significant sample of pre-production systems, across the voltage and current range of the application's power supply, should indicate if a system is susceptible to this issue.

Work around

Before configuring the module for I^2C operation:

1. Configure the SCLx and SDAx pins as outputs by clearing their corresponding TRIS bits.
2. Force SCLx and SDAx low by clearing the corresponding LAT bits.
3. While keeping the LAT bits clear, configure SCLx and SDAx as inputs by setting their TRIS bits.

Once this is done, use the SSPxCON1 and SSPxCON2 registers to configure the proper I^2C mode as before.

Date Codes that pertain to this issue:

All engineering and production devices.

18. Module: MSSP (I^2C Mode)

In I^2C Host mode, the RCEN bit is set by software to begin data reception, and cleared by the peripheral after a byte is received. After a byte is received, the device may take up to 80 TCY to clear RCEN and 800 TCY during emulation.

Work around

Single byte receptions are typically not affected, since the delay between byte receptions typically is long enough for the RCEN bit to clear. For multiple byte receptions, the software must wait until the bit is cleared by the peripheral before the next byte can be received.

Date Codes that pertain to this issue:

All engineering and production devices.

19. Module: ECCP (PWM Mode)

When the PWM auto-shutdown feature is configured for automatic restart by setting the PxRSEN bit (ECCPxDEL<7>), the pulse may terminate immediately in a shutdown event. In addition, the pulse may restart within the period if the shutdown condition expires. This may result in the generation of short pulses on the PWM output(s).

Work around

Configure the auto-shutdown for software restart by clearing the PxRSEN bit. The PWM can be re-enabled by clearing the ECCPxASE bit (ECCPxAS<7>) after the shutdown condition expires.

Date Codes that pertain to this issue:

All engineering and production devices.

20. Module: ECCP (PWM Mode)

When configured for half-bridge operation with dead band (CCPxCON<7:6> = 10), the PWM output may be corrupted for certain values of the PWM duty cycle. This can occur when these additional criteria are also met:

- a non-zero, dead-band delay is specified (PxDC6:PxDC0 > 0); and
- the duty cycle has a value of 0 through 3, or 4n + 3 ($n \geq 1$).

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

21. Module: CCP (PWM Mode)

Timer4 is not available as a clock source for either CCP4 or CCP5 in any PWM mode (CCPxCON<3:2> = 11). Selecting Timer4 as the module's clock source may cause the PWM output to stop generating pulses.

Work around

To use CCP4 or CCP5 in PWM mode, use only Timer2 as the clock source (T3CON<6,3> = 00).

Date Codes that pertain to this issue:

All engineering and production devices.

22. Module: Reset

This version of silicon does not support the functionality described in Note 1 of parameter D002 in **Section 28.1 "DC Characteristics: Supply Voltage"** of the data sheet. The RAM content may be altered during a Reset event if the following conditions are met.

- Device is accessing RAM.
- Asynchronous Reset (i.e., WDT, BOR or $\overline{\text{MCLR}}$ occurs when a write operation is being executed (start of a Q4 cycle).

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

23. Module: External Memory Bus

The A<19:16> EMB address lines and Read/Write control pins ($\overline{\text{OE}}$, $\overline{\text{WRH}}$ and $\overline{\text{WRL}}$) are released to their respective inactive states at the same time, violating the timing condition mentioned in Figure 28-8 and Figure 28-9 in the Device Data Sheet. This may result in a peripheral device on the bus detecting an address change when a write/read is initiated. The bus capacitance and signal delay on the address and control lines can affect the probability of invalid detection.

Work around

Two work arounds are available:

1. Use a latch based on the falling edge of ALE to hold the A<19:16> signals.
2. Add a delay circuit to extend the valid time for A<19:16> signals to ensure the address is valid until read/write signals go inactive.

24. Module: Timer1/3

When Timer1 or Timer3 is operated in Asynchronous External Input mode, unexpected interrupt flag generation may occur if an external clock edge arrives too soon following a firmware write to the TMRxH:TMRxL registers. An unexpected interrupt flag event may also occur when enabling the module or switching from Synchronous to Asynchronous mode.

Work around

This issue only applies when operating the timer in Asynchronous mode. Whenever possible, operate the timer module in Synchronous mode to avoid spurious timer interrupts.

If Asynchronous mode must be used in the application, potential strategies to mitigate the issue may include any of the following:

- Design the firmware so it does not rely on the TMRxIF flag or keep the respective interrupt disabled. The timer still counts normally and does not reset to `0x0000` when the spurious interrupt flag event is generated.
- Design the firmware so that it does not write to the TMRxH:TMRxL registers or does not periodically disable/enable the timer, or switch modes. Reading from the timer does not trigger the spurious interrupt flag events.
- If the firmware must use the timer interrupts and must write to the timer (or disable/enable, or mode switch the timer), implement code to suppress the spurious interrupt event, should it occur. This can be achieved by following the process shown in Example 2.

EXAMPLE 2: ASYNCHRONOUS TIMER MODE WORK AROUND TO AVOID SPURIOUS INTERRUPT

```
//Timer1 update procedure in asynchronous mode
//The code below uses Timer1 as example

T1CONbits.TMR1ON = 0;          //Stop timer from incrementing
PIE1bits.TMR1IE = 0;           //Temporarily disable Timer1 interrupt vectoring
TMR1H = 0x00;                  //Update timer value
TMR1L = 0x00;
T1CONbits.TMR1ON = 1;          //Turn on timer

//Now wait at least two full T1CKI periods + 2TCY before re-enabling Timer1 interrupts.
//Depending upon clock edge timing relative to TMR1H/TMR1L firmware write operation,
//a spurious TMR1IF flag event may sometimes assert. If this happens, to suppress
//the actual interrupt vectoring, the TMR1IE bit should be kept clear until
//after the "window of opportunity" (for the spurious interrupt flag event has passed).
//After the window is passed, no further spurious interrupts occur, at least
//until the next timer write (or mode switch/enable event).

while(TMR1L < 0x02);           //Wait for 2 timer increments more than the Updated Timer
                               //value (indicating more than 2 full T1CKI clock periods elapsed)
NOP();                         //Wait two more instruction cycles
NOP();
PIR1bits.TMR1IF = 0;           //Clear TMR1IF flag, in case it was spuriously set
PIE1bits.TMR1IE = 1;           //Now re-enable interrupt vectoring for timer 1
```

APPENDIX A: REVISION HISTORY

Rev A Document (12/2005)
Original version of this document. Contains silicon issues: 1 (A/D), 2-4 (EUSART), 5 (ECCP), 6 (External Memory Bus), 7 (MSSP), 8 (Timer1) and 9 (PORTE).

Rev B Document (8/2006)
Added silicon issues 10-12 (EUSART), 13-15 (MSSP – SPI Mode), 16-18 (MSSP – I^2C Mode), 19-20 (ECCP – PWM Mode), 21 (CCP – PWM Mode), 22 (Reset) and 23 (External Memory Bus).

Rev C Document (7/2014)
Added Module 24, Timer1/3.

Rev D Document (3/2022)
Added Revision ID A1.

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