Product Change Notification / SYST-23TMCF310

Date:

24-Mar-2022

Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ERRATA - ATmega169A/PA/329A/PA/3290A/PA/649A/P/6490A/P Silicon Errata and Data Sheet Clarifications Revision

Affected CPNs:

SYST-23TMCF310_Affected_CPN_03242022.pdf
SYST-23TMCF310_Affected_CPN_03242022.csv

Notification Text:

SYST-23TMCF310

Microchip has released a new Product Documents for the ATmega169A/PA/329A/PA/3290A/PA/649A/P/6490A/P Silicon Errata and Data Sheet Clarifications of devices. If you are using one of these devices please read the document located at ATmega169A/PA/329A/PA/3290A/PA/649A/P/6490A/P Silicon Errata and Data Sheet Clarifications.

Notification Status: Final

Description of Change: Initial document release.

- Content moved from the data sheet and restructured to the new document template
- Updated the die revision list to reflect die revisions in production

Data Sheet Clarifications added:

- Errata section in data sheet is no longer valid
- 3.2. Power Management and Sleep Modes
- Electrical Characteristics – TA = -40°C to 85°C
  - 3.3.1. Analog Input Offset Voltage (TA = -40°C to 85°C)
  - 3.3.2. Power-Down Specification Limit (TA = -40°C to 85°C)
- Electrical Characteristics – TA = -40°C to 105°C

– 3.4.1. Analog Input Offset Voltage (TA = -40°C to 105°C)
– 3.4.2. Power-Down Specification Limit (TA = -40°C to 105°C)

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 24 March 2022

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

ATmega169A/PA/329A/PA/3290A/PA/649A/P/6490A/P Silicon Errata and Data Sheet Clarifications

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ATmega169A/PA/329A/PA/3290A/PA/649A/P/6490A/P

Silicon Errata and Data Sheet Clarifications

Introduction

The ATmega169A/PA/329A/PA/3290A/PA/649A/P/6490A/P devices you have received conform functionally to the current device data sheet (www.microchip.com/mymicrochip/filehandler.aspx?ddocname=en598055), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the ATmega169A/PA/329A/PA/3290A/PA/649A/P/6490A/P devices.

Note:

- This document summarizes all the silicon errata issues from all revisions of silicon, previous and current.

1. Silicon Issue Summary

- \- Erratum is not applicable.
- X Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision				
		ATmega169A/PA			ATmega329A/PA/3290A/PA	ATmega649A/P/6490A/P
		Rev. I (1)	Rev. J	Rev. K	Rev. D (1)	Rev. B (1)
Timer	2.2.1 Interrupts may be lost when writing the timer registers in the asynchronous timer	X	X	X	X	X

Note:

1. This revision is the initial release of the silicon.

2. Silicon Errata Issues

2.1 Errata Details

- Erratum is not applicable.

X Erratum is applicable.

2.2 Timer

2.2.1 Interrupts May Be Lost When Writing the Timer Registers in the Asynchronous Timer

The interrupt will be lost if writing a timer register that is a synchronous timer clock when the asynchronous Timer/Counter register (TCNTx) is 0x00.

Work Around

Always check that the asynchronous Timer/Counter register neither has the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register (TCCRx), asynchronous Timer Counter Register (TCNTx), or asynchronous Output Compare Register (OCRx).

Affected Silicon Revisions

ATmega169A/PA		
Rev. I	Rev. J	Rev. K
X	X	X

ATmega329A/PA/3290A/PA
Rev. D
X

ATmega649A/P/6490A/P
Rev. B
X

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (www.microchip.com/mymicrochip/filehandler.aspx?ddocname=en598055).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 Errata Section in Data Sheet is no Longer Valid

A clarification for the Errata section in the device data sheet has been made.

The errata content has been moved to a separate document, *ATmega169A/PA/329A/PA/3290A/PA/649A/P/6490A/PSilicon Errata and Data Sheet Clarification* (this document).

See the *Silicon Errata Issues* section of this document for the latest errata.

3.2 Power Management and Sleep Modes

A clarification has been made to the *Active clock domains and wake-up sources in the different sleep modes* table to make the headings visible.

Table 10-1. Active Clock Domains and Wake-Up Sources in the Different Sleep Modes

	Active Clock Domains					Oscillators		Wake-up Sources							Software BOD Disable
Sleep Mode	clk_{CPU}	clk_{FLASH}	clk_{IO}	clk_{ADC}	clk_{ASY}	Main Clock Source Enabled	Timer Osc Enabled	INT0 and Pin Change	USI Start Condition	LCD Controller	Timer2	SPM/ EEPROM Ready	ADC	Other I/O	
Idle			X	X	X	X	X(2)	X	X	X	X	X	X	X	
ADC NRM				X	X	X	X(2)	X(3)	X	X(2)	X(2)	X	X		
Power-down								X(3)	X						X
Power-save					X		X	X(3)	X	X	X				X
Standby(1)						X		X(3)	X						X

Notes:

1. Only recommended with external XTAL or resonator selected as clock source.
2. If either the LCD controller or Timer/Counter2 is running in asynchronous mode.
3. For INT0, only level interrupt.

3.3 Electrical Characteristics – T_A = -40°C to 85°C

3.3.1 Analog Input Offset Voltage (T_A = -40°C to 85°C)

A clarification has been made for the Analog Comparator Input Offset Voltage.

Table 29-1. T_A = -40°C to 85°C, V_{CC} = 1.8V to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IL}	Input low voltage, except XTAL1 pin	V_{CC} = 1.8V - 2.4V V_{CC} = 2.4V - 5.5V	-0.5 -0.5		$0.2V_{CC}$(1) $0.3V_{CC}$(1)	V
V_{IL1}	Input low voltage, XTAL1 pin	V_{CC} = 1.8V - 5.5V	-0.5		$0.1V_{CC}$(1)	
V_{IH}	Input high voltage, except XTAL1 and RESET pins	V_{CC} = 1.8V - 2.4V V_{CC} = 2.4V - 5.5V	$0.7V_{CC}$(2) $0.6V_{CC}$(2)		V_{CC} + 0.5 V_{CC} + 0.5	
V_{IH1}	Input high voltage, XTAL1 pin	V_{CC} = 1.8V - 2.4V V_{CC} = 2.4V - 5.5V	$0.8V_{CC}$(2) $0.7V_{CC}$(2)		V_{CC} + 0.5 V_{CC} + 0.5	
V_{IH2}	Input high voltage, RESET pin	V_{CC} = 1.8V - 5.5V	$0.85V_{CC}$(2)		V_{CC} + 0.5	
V_{OL}	Output low voltage(3), Port A, C, D, E, F, G, H, J	I_{OL} = 10 mA, V_{CC} = 5V I_{OL} = 5 mA, V_{CC} = 3V			0.9 0.6	
V_{OL1}	Output low voltage(3), Port B	I_{OL} = 20 mA, V_{CC} = 5V I_{OL} = 10 mA, V_{CC} = 3V			0.9 0.6	
V_{OH}	Output high voltage(4), Port A, C, D, E, F, G, H, J	I_{OH} = -10 mA, V_{CC} = 5V I_{OH} = -5 mA, V_{CC} = 3V	4.2 2.3			
V_{OH1}	Output high voltage(4), Port B	I_{OH} = -20 mA, V_{CC} = 5V I_{OH} = -10 mA, V_{CC} = 3V	4.2 2.3			
I_{IL}	Input leakage current I/O Pin	V_{CC} = 5.5V, pin low (absolute value)			1	µA
I_{IH}	Input leakage current I/O Pin	V_{CC} = 5.5V, pin high (absolute value)			1	
R_{RST}	Reset pull-up resistor		20		100	kΩ
R_{PU}	I/O Pin pull-up resistor		20		100	kΩ
V_{ACIO}	Analog comparator input offset voltage	V_{CC} = 5V V_{in} = V_{CC}/2		< 10	40	mV
V_{ACIO}	**Analog comparator input offset voltage**	**V_{CC} < 3.6V** **V_{in} < 0.5V**		**<15**	**60(5)**	**mV**
V_{ACIO}	**Analog comparator input offset voltage**	**V_{CC} > 3.6V** **V_{in} < 0.5V**		**<15**	**500(5)**	**mV**
I_{ACLK}	Analog comparator	V_{CC} = 5V V_{in} = V_{CC}/2	-50		50	nA
t_{ACID}	Analog comparator propagation delay	V_{CC} = 2.7V V_{CC} = 4.0V		750 500		ns

Notes:

1. "Max" means the highest value where the pin is ensured to be read as low.
2. "Min" means the lowest value where the pin is ensured to be read as high.
3. Although each I/O port can sink more than the test conditions (20 mA at VCC = 5V, 10 mA at VCC = 3V for Port B and 10 mA at VCC = 5V, 5 mA at VCC = 3V for all other ports) under steady-state conditions (non-transient), observe the following:
   - TQFP and QFN/MLF Package:
     i. The sum of all IOL for all ports should not exceed 400 mA.
     ii. The sum of all IOL for ports A0 - A7, C4 - C7, and G2 should not exceed 100 mA.
     iii. The sum of all IOL for ports B0 - B7, E0 - E7, and G3 - G5 should not exceed 100 mA.
     iv. The sum of all IOL for ports D0 - D7, C0 - C3, and G0 - G1 should not exceed 100 mA.
     v. The sum of all IOL for ports F0 - F7 should not exceed 100 mA.

   If IOL exceeds the test condition, VOL may exceed the related specification. Pins are not ensured to sink current higher than the listed test condition.
4. Although each I/O port can source more than the test conditions (20 mA at VCC = 5V, 10 mA at VCC = 3V for Port B and 10 mA at VCC = 5V, 5 mA at VCC = 3V for all other ports) under steady-state conditions (non-transient), observe the following:
   - TQFP and QFN/MLF Package:
     i. The sum of all IOH for all ports should not exceed 400 mA.
     ii. The sum of all IOH for ports A0 - A7, C4 - C7, and G2 should not exceed 100 mA.
     iii. The sum of all IOH for ports B0 - B7, E0 - E7, and G3 - G5 should not exceed 100 mA.
     iv. The sum of all IOH for ports D0 - D7, C0 - C3, and G0 - G1 should not exceed 100 mA.
     v. The sum of all IOH for ports F0 - F7 should not exceed 100 mA.

   If IOH exceeds the test condition, VOH may exceed the related specification. Pins are not ensured to source current higher than the listed test condition
5. **These values are based on characterization. The max. limit in production can therefore not be assured.**

3.3.2 Power-Down Specification Limit (T_A = -40°C to 85°C)

A clarification for the power-down specification limit has been made. This clarification has corrections that are impractical to mark in bold. The following tables in this section contain the most current information and notes.

Table 29-2. ATmega169A DC Characteristics. T_A = -40°C to 85°C, V_{CC} = 1.8V to 5.5V (unless otherwise noted).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power supply current(1)	Active 1 MHz, V_{CC} = 2V		0.35	1.0	mA
		Active 4 MHz, V_{CC} = 3V		2.3	3.5	
		Active 8 MHz, V_{CC} = 5V		8.4	12.0	
		Idle 1 MHz, V_{CC} = 2V		0.1	0.45	
		Idle 4 MHz, V_{CC} = 3V		0.7	1.2	
		Idle 8 MHz, V_{CC} = 5V		3.0	5.5	
	Power-save mode(2)	32.768 kHz TOSC enabled, V_{CC} = 1.8V		0.55		µA
		32.768 kHz TOSC enabled, V_{CC} = 3V		0.8		
	Power-down mode(2)	WDT enabled, V_{CC} = 3V		6.0	15	
		WDT disabled, V_{CC} = 3V		0.2	3.0	

Notes:

1. All bits are set in the 'Power Reduction Register' on page 42.
2. **Maximum and Typical values for 25°C. Maximum values are test limits in production.**

Table 29-3. ATmega169PA DC Characteristics. T_A = -40°C to 85°C, V_{CC} = 1.8V to 5.5V (unless otherwise noted).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power supply current(1)	Active 1 MHz, V_{CC} = 2V		0.35	0.44	mA
		Active 4 MHz, V_{CC} = 3V		2.3	2.5	
		Active 8 MHz, V_{CC} = 5V		8.4	9.5	
		Idle 1 MHz, V_{CC} = 2V		0.1	0.2	
		Idle 4 MHz, V_{CC} = 3V		0.7	0.8	
		Idle 8 MHz, V_{CC} = 5V		3.0	3.3	
	Power-save mode(2)	32.768 kHz TOSC enabled, V_{CC} = 1.8V		0.55		µA
		32.768 kHz TOSC enabled, V_{CC} = 3V		0.8		
	Power-down mode(2)	WDT enabled, V_{CC} = 3V		6.0	10.0	
		WDT disabled, V_{CC} = 3V		0.2	2.0	

Notes:

1. All bits are set in the 'Power Reduction Register' on page 42.
2. **Maximum and Typical values for 25°C. Maximum values are test limits in production.**

Table 29-4. ATmega329A DC Characteristics. T_A = -40°C to 85°C, V_{CC} = 1.8V to 5.5V (unless otherwise noted).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power supply current(1)	Active 1 MHz, V_{CC} = 2V		0.8	1.5	mA
		Active 4 MHz, V_{CC} = 3V		2.6	3.5	
		Active 8 MHz, V_{CC} = 5V		6.0	12.0	
		Idle 1 MHz, V_{CC} = 2V		0.2	0.45	
		Idle 4 MHz, V_{CC} = 3V		0.7	1.5	
		Idle 8 MHz, V_{CC} = 5V		1.8	5.5	
	Power-save mode(2)	32.768 kHz TOSC enabled, V_{CC} = 1.8V		0.75		µA
		32.768 kHz TOSC enabled, V_{CC} = 3V		0.8		
	Power-down mode(2)	WDT enabled, V_{CC} = 3V		7.5	15.0	
		WDT disabled, V_{CC} = 3V		0.3	3.0	

Notes:

1. All bits are set in the 'Power Reduction Register' on page 42.
2. **Maximum and Typical values for 25°C. Maximum values are test limits in production.**

Table 29-5. ATmega329PA DC Characteristics. T_A = -40°C to 85°C, V_{CC} = 1.8V to 5.5V (unless otherwise noted).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power supply current(1)	Active 1 MHz, V_{CC} = 2V		0.37	0.55	mA
		Active 4 MHz, V_{CC} = 3V		2.4	2.9	
		Active 8 MHz, V_{CC} = 5V		5.3	11.0	
		Idle 1 MHz, V_{CC} = 2V		0.14	0.25	
		Idle 4 MHz, V_{CC} = 3V		0.6	0.9	
		Idle 8 MHz, V_{CC} = 5V		1.6	3.5	
	Power-save mode(2)	32.768 kHz TOSC enabled, V_{CC} = 1.8V		0.75		µA
		32.768 kHz TOSC enabled, V_{CC} = 3V		0.8		
	Power-down mode(2)	WDT enabled, V_{CC} = 3V		6.7	12.0	
		WDT disabled, V_{CC} = 3V		0.2	2.0	

Notes:

1. All bits are set in the 'Power Reduction Register' on page 42.
2. **Maximum and Typical values for 25°C. Maximum values are test limits in production.**

Table 29-6. ATmega3290A DC Characteristics. T_A = -40°C to 85°C, V_{CC} = 1.8V to 5.5V (unless otherwise noted).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power supply current(1)	Active 1 MHz, V_{CC} = 2V		0.8	1.5	mA
		Active 4 MHz, V_{CC} = 3V		2.6	3.5	
		Active 8 MHz, V_{CC} = 5V		6.0	12.0	
		Idle 1 MHz, V_{CC} = 2V		0.2	0.45	
		Idle 4 MHz, V_{CC} = 3V		0.7	1.5	
		Idle 8 MHz, V_{CC} = 5V		1.8	5.5	
	Power-save mode(2)	32.768 kHz TOSC enabled, V_{CC} = 1.8V		0.75		µA
		32.768 kHz TOSC enabled, V_{CC} = 3V		0.8		
	Power-down mode(2)	WDT enabled, V_{CC} = 3V		7.5	15.0	
		WDT disabled, V_{CC} = 3V		0.3	3.0	

Notes:

1. All bits are set in the 'Power Reduction Register' on page 42.
2. **Maximum and Typical values for 25°C. Maximum values are test limits in production.**

Table 29-7. ATmega3290PA DC Characteristics. T_A = -40°C to 85°C, V_{CC} = 1.8V to 5.5V (unless otherwise noted).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power supply current(1)	Active 1 MHz, V_{CC} = 2V		0.37	0.55	mA
		Active 4 MHz, V_{CC} = 3V		2.4	2.9	
		Active 8 MHz, V_{CC} = 5V		5.3	11.0	
		Idle 1 MHz, V_{CC} = 2V		0.14	0.25	
		Idle 4 MHz, V_{CC} = 3V		0.6	0.9	
		Idle 8 MHz, V_{CC} = 5V		1.6	3.5	
	Power-save mode(2)	32.768 kHz TOSC enabled, V_{CC} = 1.8V		0.75		µA
		32.768 kHz TOSC enabled, V_{CC} = 3V		0.8		
	Power-down mode(2)	WDT enabled, V_{CC} = 3V		6.7	12.0	
		WDT disabled, V_{CC} = 3V		0.2	2.0	

Notes:

1. All bits are set in the 'Power Reduction Register' on page 42.
2. **Maximum and Typical values for 25°C. Maximum values are test limits in production.**

Table 29-8. ATmega649A DC Characteristics. T_A = -40°C to 85°C, V_{CC} = 1.8V to 5.5V (unless otherwise noted).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power supply current(1)	Active 1 MHz, V_{CC} = 2V		1.1	1.5	mA
		Active 4 MHz, V_{CC} = 3V		2.8	3.5	
		Active 8 MHz, V_{CC} = 5V		7.0	12.0	
		Idle 1 MHz, V_{CC} = 2V		0.3	0.45	
		Idle 4 MHz, V_{CC} = 3V		0.8	1.5	
		Idle 8 MHz, V_{CC} = 5V		2.5	5.5	
	Power-save mode(2)	32.768 kHz TOSC enabled, V_{CC} = 1.8V		0.75		µA
		32.768 kHz TOSC enabled, V_{CC} = 3V		0.8		
	Power-down mode(2)	WDT enabled, V_{CC} = 3V		7.0	15.0	
		WDT disabled, V_{CC} = 3V		0.25	3.0	

Notes:

1. All bits are set in the 'Power Reduction Register' on page 42.
2. **Maximum and Typical values for 25°C. Maximum values are test limits in production.**

Table 29-9. ATmega649P DC Characteristics. T_A = -40°C to 85°C, V_{CC} = 1.8V to 5.5V (unless otherwise noted).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power supply current(1)	Active 1 MHz, V_{CC} = 2V		1.04	0.55	mA
		Active 4 MHz, V_{CC} = 3V		1.7	2.9	
		V_{CC} 8 MHz, V_{CC} = 5V		5.8	11.0	
		Idle 1 MHz, V_{CC} = 2V		0.25	0.25	
		Idle 4 MHz, V_{CC} = 3V		0.39	0.90	
		Idle 8 MHz, V_{CC} = 5V		1.6	3.50	
	Power-save mode(2)	32.768 kHz TOSC enabled, V_{CC} = 1.8V		0.75		µA
		32.768 kHz TOSC enabled, V_{CC} = 3V		0.8		
	Power-down mode(2)	WDT enabled, V_{CC} = 3V		7.0	10.0	
		WDT disabled, V_{CC} = 3V		0.25	2.0	

Notes:

1. All bits are set in the 'Power Reduction Register' on page 42.
2. **Maximum and Typical values for 25°C. Maximum values are test limits in production.**

Table 29-10. ATmega6490A DC Characteristics. T_A = -40°C to 85°C, V_{CC} = 1.8V to 5.5V (unless otherwise noted).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power supply current(1)	Active 1 MHz, V_{CC} = 2V		1.1	1.5	mA
		Active 4 MHz, V_{CC} = 3V		2.8	3.5	
		Active 8 MHz, V_{CC} = 5V		7.0	12.0	
		Idle 1 MHz, V_{CC} = 2V		0.3	0.45	
		Idle 4 MHz, V_{CC} = 3V		0.8	1.5	
		Idle 8 MHz, V_{CC} = 5V		2.5	5.5	
	Power-save mode(2)	32.768 kHz TOSC enabled, V_{CC} = 1.8V		0.75		µA
		32.768 kHz TOSC enabled, V_{CC} = 3V		0.8		
	Power-down mode(2)	WDT enabled, V_{CC} = 3V		7.0	15.0	
		WDT disabled, V_{CC} = 3V		0.25	3.0	

Notes:

1. All bits are set in the 'Power Reduction Register' on page 42.
2. **Maximum and Typical values for 25°C. Maximum values are test limits in production.**

Table 29-11. ATmega6490P DC Characteristics. T_A = -40°C to 85°C, V_{CC} = 1.8V to 5.5V (unless otherwise noted).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power supply current(1)	Active 1 MHz, V_{CC} = 2V		1.04	0.55	mA
		Active 4 MHz, V_{CC} = 3V		1.7	2.9	
		Active 8 MHz, V_{CC} = 5V		5.8	11.0	
		Idle 1 MHz, V_{CC} = 2V		0.25	0.25	
		Idle 4 MHz, V_{CC} = 3V		0.39	0.90	
		Idle 8 MHz, V_{CC} = 5V		1.6	3.50	
	Power-save mode(2)	32.768 kHz TOSC enabled, V_{CC} = 1.8V		0.75		µA
		32.768 kHz TOSC enabled, V_{CC} = 3V		0.8		
	Power-down mode(2)	WDT enabled, V_{CC} = 3V		7.0	10.0	
		WDT disabled, V_{CC} = 3V		0.25	2.0	

Notes:

1. All bits are set in the 'Power Reduction Register' on page 42.
2. **Maximum and Typical values for 25°C. Maximum values are test limits in production.**

3.4 Electrical Characteristics – T_A = -40°C to 105°C

3.4.1 Analog Input Offset Voltage (T_A = -40°C to 105°C)

A clarification has been made for the Analog Comparator Input Offset Voltage in Table 30-1.

Table 30-1. T_A = -40°C to 105°C, VCC = 1.8V to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IL}	Input low voltage except XTAL1 and $\overline{RESET}$ pins	V_{CC} = 1.8V - 2.4V V_{CC} = 2.4V - 5.5V	-0.5 -0.5		$0.2V_{CC}$(1) $0.3V_{CC}$(1)	V
V_{IL1}	Input low voltage XTAL1 pins	V_{CC} = 1.8V - 5.5V	-0.5		$0.1V_{CC}$(1)	
V_{IL2}	Input low voltage, $\overline{RESET}$ pins	V_{CC} = 1.8V - 5.5V	-0.5		$0.1V_{CC}$(1)	
V_{IH}	Input high voltage except XTAL1 and $\overline{RESET}$ pins	V_{CC} = 1.8V - 2.4V V_{CC} = 2.4V - 5.5V	$0.7V_{CC}$(2) $0.6V_{CC}$(2)		V_{CC} + 0.5 V_{CC} + 0.5	
V_{IH1}	Input high voltage, XTAL1 pin	V_{CC} = 1.8V - 2.4V V_{CC} = 2.4V - 5.5V	$0.8V_{CC}$(2) $0.7V_{CC}$(2)		V_{CC} + 0.5 V_{CC} + 0.5	
V_{IH2}	Input high voltage, $\overline{RESET}$ pins	V_{CC} = 1.8V - 5.5V	$0.9V_{CC}$(2)		V_{CC} + 0.5	
V_{OL}	Output low voltage(3), Port A, C, D, E, F, G	I_{OL} = 10mA, V_{CC} = 5V I_{OL} = 5 mA, V_{CC} = 3V			0.7/1.0(5) 0.5/0.7(5)	
V_{OL1}	Output low voltage(3), Port B	I_{OL} = 20 mA, V_{CC} = 5V I_{OL} = 10 mA, V_{CC} = 3V			0.7/1.0(5) 0.5/0.7(5)	
V_{OH}	Output high voltage(4), Port A, C, D, E, F, G	I_{OH} = -10A, V_{CC} = 5V I_{OH} = -5 mA, V_{CC} = 3V	4.2 2.3			
V_{OH1}	Output high voltage(4), Port B	I_{OH} = -20 mA, V_{CC} = 5V I_{OH} = -10 mA, V_{CC} = 3V	4.2 2.3			
I_{IL}	Input leakage current I/O Pin	V_{CC} = 5.5V, pin low (absolute value)			1	µA
I_{IH}	Input leakage current I/O Pin	V_{CC} = 5.5V, pin high (absolute value)			1	
R_{RST}	Reset pull-up resistor		20		60	kΩ
R_{PU}	I/O Pin pull-up resistor		20		50	
V_{ACIO}	Analog comparator input offset voltage	V_{CC} =5V V_{in} = V_{CC}/2		< 10	40	mV
V_{ACIO}	**Analog comparator input offset voltage**	**V_{CC} < 3.6V** **V_{in} < 0.5V**		**<15**	**60(6)**	**mV**
V_{ACIO}	**Analog comparator input offset voltage**	**V_{CC} > 3.6V** **V_{in} < 0.5V**		**<15**	**500(6)**	**mV**
I_{ACLK}	Analog comparator	V_{CC} = 5V V_{in} = V_{CC}/2	-50		50	nA
t_{ACID}	Analog comparator propagation delay	V_{CC} = 2.7V V_{CC} = 4.0V		750 500		ns

Notes:

1. "Max" means the highest value where the pin is ensured to be read as low
2. "Min" means the lowest value where the pin is ensured to be read as high
3. Although each I/O port can sink more than the test conditions (20 mA at V_{CC} = 5V, 10 mA at V_{CC}= 3V for Port B and 10 mA at V_{CC} = 5V, 5 mA at V_{CC} = 3V for all other ports) under steady-state conditions (non-transient), the following must be observed
   - TQFP and QFN/MLF Package:
     i. The sum of all IOL for all ports should not exceed 400 mA.
     ii. The sum of all IOL for ports A0 - A7, C4 - C7, and G2 should not exceed 100 mA.
     iii. The sum of all IOL for ports B0 - B7, E0 - E7, and G3 - G5 should not exceed 100 mA.
     iv. The sum of all IOL for ports D0 - D7, C0 - C3, and G0 - G1 should not exceed 100 mA.
     v. The sum of all IOL for ports F0 - F7 should not exceed 100 mA.

   If IOL exceeds the test condition, VOL may exceed the related specification. Pins are not ensured to sink current higher than the listed test condition.
4. Although each I/O port can source more than the test conditions (20 mA at VCC = 5V, 10 mA at VCC = 3V for Port B and 10 mA at VCC = 5V, 5 mA at VCC = 3V for all other ports) under steady-state conditions (non-transient), observe the following:
   - TQFP and QFN/MLF Package:
     i. The sum of all IOH for all ports should not exceed 400 mA.
     ii. The sum of all IOH for ports A0 - A7, C4 - C7, and G2 should not exceed 100 mA.
     iii. The sum of all IOH for ports B0 - B7, E0 - E7, and G3 - G5 should not exceed 100 mA.
     iv. The sum of all IOH for ports D0 - D7, C0 - C3, and G0 - G1 should not exceed 100 mA.
     v. The sum of all IOH for ports F0 - F7 should not exceed 100 mA.

   If IOH exceeds the test condition, VOH may exceed the related specification. Pins are not ensured to source current higher than the listed test condition
5. Largest value for ATmega329P and ATmega3290P.
6. **These values are based on characterization. The max. limit in production can therefore not be assured.**

3.4.2 Power-Down Specification Limit (T_A = -40°C to 105°C)

A clarification for the power-down specification limit has been made. This clarification has corrections that are impractical to mark in bold. The following tables in this section contain the most current information and notes.

Sections 30.2.6 and 30.2.3 are not relevant for the devices documented in this data sheet and should be disregarded.

Table 30-2. Current Consumption ATmega169PA T_A = -40°C to 105°C, V_{CC} = 1.8V to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power supply current(1)	Active 1 MHz, V_{CC} = 2V		0.4	0.5	mA
		Active 4 MHz, V_{CC} = 3V		2.3	2.8	mA
		Active 8 MHz, V_{CC} = 5V		9	11	
		Idle 1 MHz, V_{CC} = 2V		0.1	0.2	
		Idle 4 MHz, V_{CC} = 3V		0.8	0.9	
		Idle 8 MHz, V_{CC} = 5V		3.1	3.3	
	Power-save mode(2)	32.768 kHz TOSC enabled, V_{CC} = 1.8V		0.6	1.8	µA
		32.768 kHz TOSC enabled, V_{CC} = 3V		0.9	3	
	Power-down mode(2)	WDT enabled, V_{CC} = 3V		7	11	
		WDT disabled, V_{CC} = 3V		0.2	2.5	

Note:

1. **Maximum and Typical values for 25°C. Maximum values are test limits in production.**

Table 30-3. Current Consumption ATmega329A T_A = -40°C to 105°C, V_{CC} = 1.8V to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power supply current(1)	Active 1 MHz, V_{CC} = 2V		0.35	0.55	mA
		Active 4 MHz, V_{CC} = 3V		1.65	2.9	mA
		Active 8 MHz, V_{CC} = 5V		5.7	11	
		Idle 1 MHz, V_{CC} = 2V		0.1	0.2	
		Idle 4 MHz, V_{CC} = 3V		0.4	0.90	
		Idle 8 MHz, V_{CC} = 5V		1.65	3.5	
	Power-save mode(2)	32.768 kHz TOSC enabled, V_{CC} = 1.8V				µA
		32.768 kHz TOSC enabled, V_{CC} = 3V			3	
	Power-down mode(2)	WDT enabled, V_{CC} = 3V		12	15	
		WDT disabled, V_{CC} = 3V		4.7	5	

Notes:

1. All bits are set in the 'Power Reduction Register' on page 42.
2. **Maximum and Typical values for 25°C. Maximum values are test limits in production.**

Table 30-5. Current Consumption ATmega329PA T_A = -40°C to 105°C, V_{CC} = 1.8V to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power supply current(1)	Active 1 MHz, V_{CC} = 2V		0.35	0.55	mA
		Active 4 MHz, V_{CC} = 3V		1.65	2.9	
		Active 8 MHz, V_{CC} = 5V		5.7	11	
		Idle 1 MHz, V_{CC} = 2V		0.1	0.2	
		Idle 4 MHz, V_{CC} = 3V		0.4	0.90	
		Idle 8 Hz, V_{CC} = 5V		1.65	3.5	
	Power-save mode(2)	32.768 kHz TOSC enabled, V_{CC} = 1.8V				µA
		32.768 kHz TOSC enabled, V_{CC} = 3V			3	
	Power-down mode(2)	WDT enabled, V_{CC} = 3V		12	15	
		WDT disabled, V_{CC} = 3V		4.7	5	

Notes:

1. All bits are set in the 'Power Reduction Register' on page 42.
2. **Maximum and Typical values for 25°C. Maximum values are test limits in production.**

Table 30-6. Current Consumption ATmega3290A T_A = -40°C to 105°C, V_{CC} = 1.8V to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power supply current(1)	Active 1 MHz, V_{CC} = 2V		0.35	0.55	mA
		Active 4 MHz, V_{CC} = 3V		1.65	2.9	
		Active 8 MHz, V_{CC} = 5V		5.7	11	
		Idle 1 MHz, V_{CC} = 2V		0.1	0.2	
		Idle 4 MHz, V_{CC} = 3V		0.4	0.90	
		Idle 8 MHz, V_{CC} = 5V		1.65	3.5	
	Power-save mode(2)	32.768 kHz TOSC enabled, V_{CC} = 1.8V				µA
		32.768 kHz TOSC enabled, V_{CC} = 3V			3	
	Power-down mode(2)	WDT enabled, V_{CC} = 3V		12	15	
		WDT disabled, V_{CC} = 3V		4.7	5	

Notes:

1. All bits are set in the 'Power Reduction Register' on page 42.
2. **Maximum and Typical values for 25°C. Maximum values are test limits in production.**

Table 30-8. Current Consumption ATmega3290PA T_A = -40°C to 105°C, V_{CC} = 1.8V to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power supply current(1)	Active 1 MHz, V_{CC} = 2V		0.35	0.55	mA
		Active 4 MHz, V_{CC} = 3V		1.65	2.9	
		Active 8 MHz, V_{CC} = 5V		5.7	11	
		Idle 1 MHz, V_{CC} = 2V		0.1	0.2	
		Idle 4 MHz, V_{CC} = 3V		0.4	0.90	
		Idle 8 MHz, V_{CC} = 5V		1.65	3.5	
	Power-save mode(2)	32.768 kHz TOSC enabled, V_{CC} = 1.8V				µA
		32.768 kHz TOSC enabled, V_{CC} = 3V			3	
	Power-down mode(2)	WDT enabled, V_{CC} = 3V		12	15	
		WDT disabled, V_{CC} = 3V		4.7	5	

Notes:

1. All bits are set in the 'Power Reduction Register' on page 42.
2. **Maximum and Typical values for 25°C. Maximum values are test limits in production.**

4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc Rev.	Date	Comments
A	03/2022	Initial document release. • Content moved from the data sheet and restructured to the new document template • Updated the die revision list to reflect die revisions in production Data Sheet Clarifications added: • Errata section in data sheet is no longer valid • 3.2. Power Management and Sleep Modes • Electrical Characteristics – TA = -40°C to 85°C – 3.3.1. Analog Input Offset Voltage (TA = -40°C to 85°C) – 3.3.2. Power-Down Specification Limit (TA = -40°C to 85°C) • Electrical Characteristics – TA = -40°C to 105°C – 3.4.1. Analog Input Offset Voltage (TA = -40°C to 105°C) – 3.4.2. Power-Down Specification Limit (TA = -40°C to 105°C)

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