Product Change Notification / SYST-23EQNR513

Date:

24-Mar-2022

Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ERRATA - PIC18F27/47/57Q43 Family Silicon Errata and Data Sheet Clarifications Revision

Affected CPNs:

SYST-23EQNR513_Affected_CPN_03242022.pdf
SYST-23EQNR513_Affected_CPN_03242022.csv

Notification Text:

SYST-23EQNR513

Microchip has released a new Product Documents for the PIC18F27/47/57Q43 Family Silicon Errata and Data Sheet Clarifications of devices. If you are using one of these devices please read the document located at PIC18F27/47/57Q43 Family Silicon Errata and Data Sheet Clarifications.

Notification Status: Final

Description of Change: Added silicon errata items 1.1.2, 1.6.1, 17.1 and data sheet clarifications 2.1 and 2.2

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 24 March 2022

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

PIC18F27/47/57Q43 Family Silicon Errata and Data Sheet Clarifications

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Affected Catalog Part Numbers (CPN)

PIC18F57Q43-E/6LX
PIC18F27Q43-E/SP
PIC18F27Q43-E/ML
PIC18F27Q43-E/SS
PIC18F27Q43-E/SO
PIC18F47Q43-E/MP
PIC18F47Q43-E/P
PIC18F27Q43-E/STX
PIC18F47Q43-E/ML
PIC18F47Q43-E/PT
PIC18F57Q43-E/PT
PIC18F57Q43-I/6LX
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PIC18F27Q43-I/ML
PIC18F27Q43-I/SS
PIC18F27Q43-I/SO
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PIC18F47Q43-I/P
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PIC18F57Q43T-I/6LX
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PIC18F57Q43T-I/PT

PIC18F27/47/57Q43

PIC18F27/47/57Q43 Silicon Errata and Data Sheet Clarifications

The PIC18F27/47/57Q43 devices you have received conform functionally to the current device data sheet (DS40002147F), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC18F27/47/57Q43 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID		
		B0	B2	B3
PIC18F27Q43	0x7480	0xA040	0xA042	0xA043
PIC18F47Q43	0x74A0	0xA040	0xA042	0xA043
PIC18F57Q43	0x74C0	0xA040	0xA042	0xA043

Important: Refer to the **Device/Revision ID** section in the current **"PIC18FXXQ43 Family Programming Specification"** (DS40002079) for more detailed information on Device Identification and Revision IDs for your specific device.

Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions		
				B0	B2	B3
ADCC	Capacitive Voltage Divider	1.1.1.	CVD is only functional on PORTA[2:0] and PORTB[4:0]	X		
ADCC	Double Sample Conversions	1.1.2.	An unexpected acquisition time is added between the first and second conversions.	X	X	X
Oscillator	XT mode	1.2.1.	Maximum clock frequency limited to 2 MHz for XT mode	X	X	
I^2C	I^2C	1.3.1.	The I2CxADR0/1/2/3 registers have incorrect Reset value	X	X	X
I^2C	I^2C	1.3.2.	The I^2C Start and/or Stop flags may be set when I^2C is enabled	X	X	X
SRAM	SRAM read-back	1.4.1.	SRAM read-back can be incorrect	X		
In-Circuit Debug	Software breakpoints	1.5.1.	Software breakpoints are not available	X	X	X
SMT	Reset Bit	1.6.1.	Module stops working if RST bit is set while prescaler setting is not zero	X	X	X
Universal Asynchronous Receiver Transmitter	UART	1.7.1.	UART TXDE signal may go low before the STOP bit has been entirely transmitted	X	X	X

Note: Only those issues indicated in the last column apply to the current silicon revision.

1. Silicon Errata Issues

CAUTION

Notice: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1 Module: Analog-to-Digital Converter with Computation (ADCC)

1.1.1 Capacitive Voltage Divider (CVD)

The CVD feature is only functional on PORTA[2:0] and PORTB[4:0]. This feature is not recommended for use on any other pins.

Work around

None.

Affected Silicon Revisions

B0	B2	B3
X		

1.1.2 Double Sample Conversions

When enabling a Double Sample Conversion (DSEN = 1), with no Precharge time (ADPRE = 0) and no Acquisition time (ADACQ = 0), the maximum number of cycles of acquisition time is inserted prior to the second conversion. The first conversion will be performed as expected with no Precharge time and no Acquisition time. It is only between the first and second conversions where a maximum number of cycles of Acquisition time is performed unexpectedly.

Work around

- Method 1: Disable Double Sample Conversion (DSEN = 0) and perform two single conversions back to back.
- Method 2: If adding acquisition time is acceptable, then select no Precharge time, along with the desired Acquisition time.

Affected Silicon Revisions

B0	B2	B3
X	X	X

1.2 Module: Oscillator

1.2.1 Maximum Clock Frequency Limited to 2 MHz for XT Mode

The maximum clock frequency for the intermediate gain setting that supports quartz crystal and ceramic resonator operation (XT mode) is being reduced from 4 MHz to 2 MHz.

Work around

For crystal or resonator frequencies above 2 MHz, use HS mode.

Affected Silicon Revisions

B0	B2	B3
X	X	

1.3 Module: I²C

1.3.1 The I2CxADR0/1/2/3 Registers Have Incorrect Reset Value

The I2CxADR0/2 registers reset to `0xFF` when the I2CxMD is enabled instead of `0x00`. The I2CxADR1/3 registers reset to `0xFE` when the I2CxMD is enabled instead of `0x00`.

Work around
None.

Affected Silicon Revisions

B0	B2	B3
X	X	X

1.3.2 The I²C Start and/or Stop Flags May Be Set When I²C Is Enabled

When I²C is enabled, erroneous Start and/or Stop conditions may be detected. This can generate erroneous I²C interrupts if enabled.

Work around
Use the following procedure to correctly detect the Start and Stop conditions:

1. Disable the Start and Stop conditions interrupt functions.
2. Enable the I²C module.
3. Wait 250 ns + six instructions cycles ($F_{OSC}/4$).
4. Clear the Start and Stop conditions interrupt flags.
5. Enable the Start and Stop conditions interrupt functions if used.

```
I2CxPIEbits.SCIE = 0;         // Disable Start conditoin interrupt
I2CxPIEbits.PCIE = 0;         // Disable Stop condition interrupt
I2CxCON0bits.EN = 1;          // Enable I2C
Delay();                      // Wait for 250 nS + 6 instruction cycles (FOSC/4)
I2CxPIRbits.SCIF = 0;         // Clear the Start condition interrupt flags
I2CxPIRbits.PCIF = 0;         // Clear the Stop condition interrupt flags
I2CxPIEbits.SCIE = 1;         // Enable Start condition interrupt if used
I2CxPIEbits.PCIE = 1;         // Enable Stop condition interrupt if used
```

Affected Silicon Revisions

B0	B2	B3
X	X	X

1.4 Module: SRAM

1.4.1 SRAM Read-Back

Following a device power-up sequence, there is a possibility that some SRAM locations will not return the expected written value but will read back '00' instead.

Work around
None. The device can only recover by power cycling.

This erroneous condition can be detected by running the following code that writes nonzero values to SRAM and then verifies that the returned read values are not '00'. If a returned value is '00', the application code has to be put into a safe state until a POR event occurs. This code has to be executed immediately after power-up. If the test passes, the device operation will be normal.

```
// SRAM test

FSR0 = 0xcff;        // Write data into RAM address for devices up to 2K RAM
INDF0 = 0x55;
PROD = INDF0;        // Read back data
if (PROD == 0){
    SAFE_STATE();    // RAM incorrectly read, suspend operation and go to Safe state
}

//For devices with more than 2K of SRAM, add the following code
FSR0 = 0x14ff;       // Write data into RAM
INDF0 = 0x55;
PROD = INDF0;        // Read back data
if (PROD == 0){
    SAFE_STATE();    // RAM incorrectly read, suspend operation and go to Safe state
}

//For devices with more than 4K of SRAM, add the following code
FSR0 = 0x24ff;       // Write data into RAM
INDF0 = 0x55;
PROD = INDF0;        // Read back data
if (PROD == 0){
    SAFE_STATE();    // RAM incorrectly read, suspend operation and go to Safe state
}
```

Affected Silicon Revisions

B0	B2	B3
X		

1.5 Module: In-Circuit Debug

1.5.1 Software Breakpoints Are Not Available

When debugging code, software breakpoints will not be available.

Work around
None.

Affected Silicon Revisions

B0	B2	B3
X	X	X

1.6 Module: SMT

1.6.1 Reset Bit

If the SMT clock prescaler is set to any value other than '00', setting the RST bit will cause the module to stop working. The RST bit will remain at the value '1', the counter will not increment, and no interrupts will be generated. The problem is cleared by turning the module off and on, or by a device reset.

Work around

- Method 1: Do not set the RST bit; manual reset is usually not required for typical operation because the measurement logic will reset the counter automatically.
- Method 2: Write zero to the counter manually. The module enable or the clock should be disabled during this.
- Method 3: Use 1:1 prescaler (PS = 00).
- Method 4: Use the CLKREF subsystem to provide a prescaled clock and set PS = 00.

Affected Silicon Revisions

B0	B2	B3
X	X	X

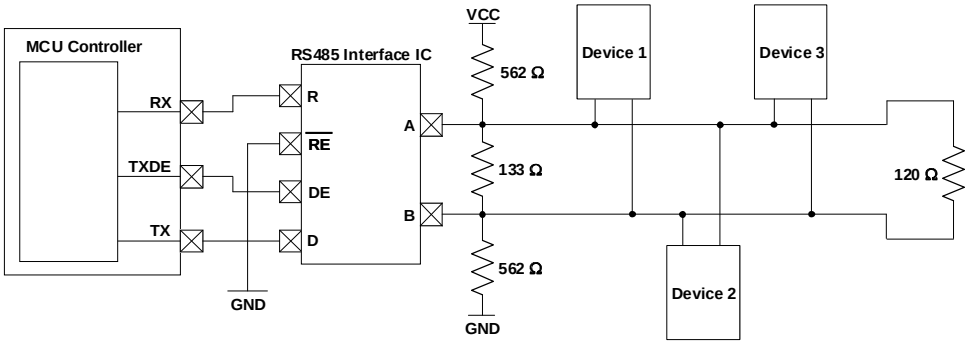
1.7 Module: Universal Asynchronous Receiver Transmitter

1.7.1 UART TXDE Signal May go Low Before The STOP Bit Has Been Entirely Transmitted.

The UART Transmit Drive Enable (TXDE) signal could potentially transition into a low state before the UART STOP bit has been entirely transmitted due to the effects of parasitic capacitance on the TX line. In some applications, this could result in communication being prematurely terminated due to the TXDE bit going low before the STOP bit has had enough time to settle.

Work around

In order to ensure that the STOP bit settles into its final logic state before the TXDE signal transitions low, a biasing circuit can be implemented. A biasing circuit allows the TX line to either be driven high or low, rather than being left in a floating tri-state mode where prolonged rise or fall times could lead to communication being disrupted. This bias circuit should only be implemented on one end of the serial bus, and a termination resistor should be used on the other end. The figure below show an example of a bias circuit that can be used to achieve this. Please note that the resistor values used in this circuit are recommendations, and that the actual resistor values required may vary based on the application.



Affected Silicon Revisions

B0	B2	B3
X	X	X

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40002147F):

Note:

Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1 Memory Programming Specifications

The flash memory cell endurance specification is reduced to **1k** minimum. The corresponding parameter (E_P) will be updated in the next revision of datasheet (DS40002147E).

Table 2-1. Memory Programming

Standard Operating Conditions (unless otherwise stated)							
Param No.	Sym.	Device Characteristics	Min.	Typ†	Max.	Units	Conditions
Data EEPROM Memory Specifications							
MEM20	E_D	DataEE Byte Endurance	100k	—	—	E/W	-40°C ≤ T_A ≤ +85°C
MEM21	T_{D_RET}	Characteristic Retention	—	40	—	Year	Provided no other specifications are violated
MEM22	N_{D_REF}	Total Erase/Write Cycles before Refresh	1M	4M	—	E/W	-40°C ≤ T_A ≤ +85°C
MEM23	V_{D_RW}	V_{DD} for Read or Erase/Write operation	V_{DDMIN}	—	V_{DDMAX}	V	
MEM24	T_{D_BEW}	Byte Erase and Write Cycle Time	—	—	11	ms	
Program Flash Memory Specifications							
MEM30	**E_P**	**Flash Memory Cell Endurance**	**1k**	—	—	**E/W**	**-40°C ≤ T_A ≤ +85°C (Note 1)**
MEM32	T_{P_RET}	Characteristic Retention	—	40	—	Year	Provided no other specifications are violated
MEM33	V_{P_RD}	V_{DD} for Read operation	V_{DDMIN}	—	V_{DDMAX}	V	
MEM34	V_{P_REW}	V_{DD} for Row Erase or Write operation	V_{DDMIN}	—	V_{DDMAX}	V	
MEM35	T_{P_REW}	Self-Timed Page Write	—	—	10	ms	
MEM36	T_{SE}	Self-Timed Page Erase	—	—	11	ms	
MEM37	T_{P_WRD}	Self-Timed Word Write	—	—	75	µs	

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note:

1. Flash Memory Cell Endurance for the Flash memory is defined as: One Row Erase operation and one Self-Timed Write.

2.2 UART Baud Rate Equation

The UART Baud Rate equation in the UxBRG register contains a typo and will provide the incorrect UART Baud Rate. The correct equation is shown below. The correction to this equation is shown in bold.

UART Baud Rate = [Fosc*(1+(BRGS*3)]/[(16*(BRG**+**1))]

3. Appendix A: Revision History

Doc Rev.	Date	Comments
K	03/2022	Added silicon errata items 1.1.2, 1.6.1, 17.1 and data sheet clarifications 2.1 and 2.2
J	07/2021	Added silicon erratum item 1.3.2
H	03/2021	Added silicon erratum item 1.5.1; deleted data sheet clarification 2.1
G	10/2020	Added silicon revision B3 and UART Transmit Collision Interrupt data sheet clarification; updated silicon erratum item 1.3.1
F	08/2020	Added silicon revision B2
E	06/2020	Added silicon erratum item 1.4.1
D	06/2020	Added silicon erratum item 1.3.1
C	04/2020	Added XT mode erratum and Temperature Indicator data sheet clarification
B	02/2020	Added working pins for CVD
A	12/2019	Initial document release

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ISBN: 978-1-5224-9626-7

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