Information note

N° 10306AERRA

Dear customer,

With this Infineon Technologies AG information note, we would like to inform you about the following

MC-ISAR AURIX Release Notes Addendum V26.0 affecting dedicated TC2xx products

On 16 April 2020, Infineon acquired Cypress.
We are now in the process of merging and consolidating our tools and processes for PCN, Information Notes, Errata and Product Discontinuance.
For further details, please visit our website:
https://www.infineon.com/cms/en/about-infineon/company/cypress-acquisition/

Infineon Technologies AG
Postal Address Headquarters: Am Campeon 1-15, D-85579 Neubiberg, Phone +49 (0)89 234-0
Chairman of the Supervisory Board: Dr. Wolfgang Eder
Management Board: Dr. Reinhard Ploss (CEO), Dr. Helmut Gassel, Jochen Hanebeck, Constanze Hufenbecher, Dr. Sven Schneider
Registered Office: Neubiberg
Commercial Register: München HRB 126492

Information note

N° 10306AERRA

▶ **Products affected**	Please refer to attached affected product list 1_cip10306

▶ **Detailed change information**

Subject	MC-ISAR AURIX Release Notes Addendum V26.0 affecting dedicated products
Reason	Update of the Release Notes Addendum due to new known issues

Description

Old	**New**
■ Release Notes Addendum V25.0	■ Release Notes Addendum V26.0

▶ **Product identification**	Not applicable (no change of product)
▶ **Impact of change**	Assessment in Application required !
▶ **Attachments**	1_cip10306 affected product list 3_cip10306 Release Notes Addendum V26.0 (MyICP link)
▶ **Intended start of delivery**	Not applicable

If you have any questions, please do not hesitate to contact your local sales office.

MC-ISAR_AURIX

Release Notes Addendum

Version: V26.0
Date: 2022-02-09

About this document

Scope and Purpose

This release notes addendum documents all the known issues in MCAL Releases. The issues pertaining to 'PR' and 'MR' releases are documented.

This release notes addendum also provides the following information

- The additional information related to 'Safety mechanisms mentioned in Safety Manual' to be considered with MCAL. Refer Section **3**.
- Details on various derivatives supported and derivative restriction applicable for the MCAL drivers. Refer Section **2**.

Following HW errata information have been analysed

1. TC29x_BB_Errata_Sheet_v1_8_10217AERRA.pdf
2. TC29x_BC_Errata_Sheet_v1_4_10218AERRA.pdf
3. TC27x_DC_Errata_Sheet_v1_4_10216AERRA.pdf
4. TC27x_DB_Errata_Sheet_v1_8_10215AERRA.pdf
5. TC27x_CA_Errata_Sheet_v1_9_10214AERRA.pdf
6. TC26x_BB_Errata_Sheet_v1_7_10211AERRA.pdf
7. TC26x_BC_Errata_Sheet_v1_4_10212AERRA.pdf
8. TC23x_AC_Errata_Sheet_v1_5_10210AERRA.pdf
9. TC23x_AB_Errata_Sheet_v1_8_10209AERRA.pdf
10. TC22x_TC21x_AB_Errata_Sheet_v1_7_10207AERRA.pdf
11. TC22x_TC21x_AC_Errata_Sheet_v1_4_10208AERRA.pdf

Note:

The safety findings which were communicated as part of the disclaimers section of release notes of RelXXX* have been closed.
To demonstrate the fulfilment of the safety claim, the corresponding safety artefacts have been modified and evidences are collated as part of the safety case.
With this, the ASIL B Process safety claim is available for the release RelXXX_FS^.
Since the safety relevant productive code delivered in RelXXX* is functionally identical to RelXXX_FS^, the ASIL B Process safety claim implicitly extends to the corresponding RelXXX* Release, assuming the usage of the latest customer documentations[i.e., User Manual, SafetyInformationDocument] delivered along with Release note addendum Ver13.0.
* RelXXX corresponds to the following Releases:
Rel318, Rel320, Rel322, Rel323, Rel314, Rel326, Rel328, Rel330, Rel334, Rel170, Rel180, Rel185, Rel250, Rel270.
^ RelXXX_FS Release Packages are Internal only. RelXXX_FS corresponds to the following Releases:
Rel318_FS, Rel320_FS, Rel322_FS, Rel323_FS, Rel314_FS, Rel326_FS, Rel328_FS, REL330_FS, REL334_FS, REL170_FS, REL180_FS, REL185_FS, REL250_FS, REL270_FS.

Intended audience

This release notes addendum is intended for MCAL users.

Scope of Release Notes Addendum

This release notes addendum, documents known issues in following AURIX MCAL releases.

HW Device	Release / Package Name	Date of Release	Release Quality	Release number / Version
TC297TA_BB	MC-ISAR_<AS_VER>_AURIX_TC29X_BB_<CFG_TYPE>_<PACKAGE_NAME>_V200	31-03-2015	PR	Rel-170/ V2.0.0
TC275_CA, TC277_CA	MC-ISAR_<AS_VER>_AURIX_TC27X_CA_<CFG_TYPE>_<PACKAGE_NAME>_V300	29-05-2015	PR	Rel185/ V3.0.0
TC275_CA, TC277_CA	MC-ISAR_<AS_VER>_AURIX_TC27X_CA_<CFG_TYPE>_<PACKAGE_NAME>_V400	25-01-2016	MR	Rel300/ V4.0.0
TC275_DB, TC277_DB	MC-ISAR_<AS_VER>_AURIX_TC27X_DB_<CFG_TYPE>_<PACKAGE_NAME>_V200	15-09-2015	PR	Rel190/ V2.0.0
TC277_DB TC275_DB	MC-ISAR_<AS_VER>_AURIX_TC27X_DB_PB_BASE_V201 MC-ISAR_<AS_VER>_AURIX_TC27X_DB_PB_STDLIN_COMPLEX_V201	28-09-2015	PR	Rel-192/ V2.0.1
TC275_DB, TC277_DB	MC-ISAR_<AS_VER>_AURIX_TC27X_DB_<CFG_TYPE>_<PACKAGE_NAME>_V300	25-01-2016	MR	Rel302/ V3.0.0
TC264_BB, TC264DA_BB, TC265_BB, TC267_BB	MC-ISAR_<AS_VER>_AURIX_TC26X_BB_<CFG_TYPE>_<PACKAGE_NAME>_V200	19-05-2015	PR	Rel180/ V2.0.0
TC264_BB, TC264DA_BB, TC265_BB, TC267_BB	MC-ISAR_<AS_VER>_AURIX_TC26X_BB_<CFG_TYPE>_<PACKAGE_NAME>_V300	06-11-2015	MR	Rel194/ V3.0.0
TC297_BB, TC297TA_BB, TC298_BB, TC299_BB, TC299TX_BB	MC-ISAR_<AS_VER>_AURIX_TC29X_BB_<CFG_TYPE>_<PACKAGE_NAME>_V210	19-05-2015	PR	Rel180/ V2.1.0

TC297_BB, TC297TA_BB, TC298_BB, TC299_BB, TC299TX_BB	MC-ISAR_<AS_VER>_AURIX_TC29X_BB_<CFG_TYPE>_<PACKAGE_NAME>_V300	30-11-2015	MR	Rel196/ V3.0.0
TC297_BB, TC297TA_BB, TC298_BB, TC299_BB, TC299TX_BB	MC-ISAR_<AS_VER>_AURIX_TC29X_BB_<CFG_TYPE>_<PACKAGE_NAME>_V310_TASKING_5_0_R2	18-12-2015	MR	Rel-198/ V3.1.0
TC234_AB, TC237_AB, TC233_AB	MC-ISAR_<AS_VER>_AURIX_TC23X_AB_<CFG_TYPE>_<PACKAGE_NAME>_V300	15-06-2015	PR	Rel-250/ V3.0.0
TC222_AB, TC223_AB, TC224_AB	MC-ISAR_<AS_VER>_AURIX_TC22X_AB_<CFG_TYPE>_<PACKAGE_NAME>_V200	26-06-2015	PR	Rel-270/ V2.0.0
TC212_AB, TC213_AB, TC214_AB	MC-ISAR_<AS_VER>_AURIX_TC21X_AB_<CFG_TYPE>_<PACKAGE_NAME>_V200	26-06-2015	PR	Rel-270/ V2.0.0
TC26x_BB	MC-ISAR_<AS_VER>_AURIX_TC26X_BB_<CFG_TYPE>_<PACKAGE_NAME>_V310_TASKING_5_0_R2	16-02-2016	MR	Rel-304/ V3.1.0
TC297_BC	MC-ISAR_<AS_VER>_AURIX_TC29X_BC_<CFG_TYPE>_<PACKAGE_NAME>_V400	12-08-2016	MR	Rel-316/ V4.0.0
TC264_BB TC264DA_BB TC265_BB TC267_BB	MC-ISAR_<AS_VER>_AURIX_TC26X_BB_<CFG_TYPE>_<PACKAGE_NAME>_V400	12-08-2016	MR	Rel-312/ V4.0.0
TC234_AB, TC237_AB, TC233_AB	MC-ISAR_<AS_VER>_AURIX_TC23X_AB_<CFG_TYPE>_<PACKAGE_NAME>_V400	12-08-2016	MR	Rel-308/ V4.0.0
TC222_AB, TC223_AB, TC224_AB	MC-ISAR_<AS_VER>_AURIX_TC22X_AB_<CFG_TYPE>_<PACKAGE_NAME>_V300	12-08-2016	MR	Rel-310/ V3.0.0
TC212_AB, TC213_AB, TC214_AB	MC-ISAR_<AS_VER>_AURIX_TC21X_AB_<CFG_TYPE>_<PACKAGE_NAME>_V300	12-08-2016	MR	Rel310/ V3.0.0
TC297_BB	MC-ISAR_AS4XX_AURIX_TC29X_BB_PB_ETH_ENHANCED_V200	29-07-2016	MR	Rel-306/ V2.0.0
TC297_BB	MC-ISAR_AS4XX_AURIX_TC29X_BB_PB_ETH_ENHANCED_V210	15-12-2016	MR	Rel-327/ V2.1.0
TC297TX_BC	MC-ISAR_AS4XX_AURIX_TC29X_BC_PB_CAN_ENHAN	31-01-2017	MR	Rel-329/ V3.0.0

	CED_V300_REL329			
TC29x_BB	MC-ISAR_<AS_VER>_AURIX_TC29X_BB_PB_<PACKAGE_NAME>_V500_REL314	24-02-2017	MR	Rel-314 V5.0.0
TC29x_BC	MC-ISAR_<AS_VER>_AURIX_TC29X_BC_PB_<PACKAGE_NAME>_V500_REL326	24-02-2017	MR	Rel-326 V5.0.0
TC27x_CA	MC-ISAR_<AS_VER>_AURIX_TC27X_CA_PB_<PACKAGE_NAME>_V500_REL318	27-02-2017	MR	Rel-318 V5.0.0
TC27x_DB	MC-ISAR_<AS_VER>_AURIX_TC27X_DB_PB_<PACKAGE_NAME>_V500_REL320	27-02-2017	MR	Rel-320 V5.0.0
TC27x_DC	MC-ISAR_<AS_VER>_AURIX_TC27X_DC_PB_<PACKAGE_NAME>_V500_REL322	27-02-2017	MR	Rel-322 V5.0.0
TC27x_DC	MC-ISAR_<AS_VER>_AURIX_TC27X_DC_PB_<PACKAGE_NAME>_V510_REL323	24-03-2017	MR	Rel-323 V5.1.0
TC26x_BC	MC-ISAR_<AS_VER>_AURIX_TC26X_BC_PB_<PACKAGE_NAME>_V200_REL328	24-03-2017	MR	Rel-328 V2.0.0
TC23x_AC	MC-ISAR_<AS_VER>_AURIX_TC23X_AC_PB_<PACKAGE_NAME>_V201_REL330	15-05-2017	MR	Rel-330 V2.0.1
TC23x_AB	MC-ISAR_<AS_VER>_AURIX_TC23X_AB_PB_<PACKAGE_NAME>_V501_REL334	15-05-2017	MR	Rel-334 V5.0.1
TC22x_AC	MC-ISAR_<AS_VER>_AURIX_TC22X_AC_PB_<PACKAGE_NAME>_V200_REL_350	06-09-2017	PR	Rel-350 V2.0.0
TC21x_AC	MC-ISAR_<AS_VER>_AURIX_TC21X_AC_PB_<PACKAGE_NAME>_V200_REL_350	06-09-2017	PR	Rel-350 V2.0.0
TC22x_AB	MC-ISAR_<AS_VER>_AURIX_TC22X_AB_PB_<PACKAGE_NAME>_V400_REL_332	06-09-2017	MR	Rel-332 V4.0.0
TC21x_AB	MC-ISAR_<AS_VER>_AURIX_TC21X_AB_PB_<PACKAGE_NAME>_V400_REL_332	06-09-2017	MR	Rel-332 V4.0.0
TC23x_AC	MC-ISAR_AS4XX_AURIX_TC23X_AC_PB_BASE_V200_REL-342 MC-ISAR_AS4XX_AURIX_TC23X_AC_PB_COM_BASIC_V200_REL-342 MC-ISAR_AS4XX_AURIX_TC23X_AC_PB_MEM_V200_R	14-09-2017	PR	Rel-342 V2.0.0

	EL-342			
TC297TX_BC	MC-ISAR_AS4XX_AURIX_TC29X_BC_PB_CAN_ENHANCED_V400_REL-353	20-09-2017	MR	Rel-353 V4.0.0
TC26x BB	MC-ISAR_AURIX_TC26X_BB_<PACKAGE_NAME>_PB_V410_REL360	30-11-2017	MR	Rel-360 V4.1.0
TC26x BC	MC-ISAR_AURIX_TC26X_BC_<PACKAGE_NAME>_PB_V210_REL360	30-11-2017	MR	Rel-362 V2.1.0
TC29x BB	MC-ISAR_<AS_VER>_AURIX_TC29X_BB_<CFG_TYPE>_<PACKAGE_NAME>__V520_REL-354	26-02-2018	MR	Rel-354 V5.2.0
TC29x BC	MC-ISAR_<AS_VER>_AURIX_TC29X_BB_<CFG_TYPE>_<PACKAGE_NAME>__V520_REL-356	26-02-2018	MR	Rel-356 V5.2.0
TC297TX BC	MC-ISAR_AS4XX_AURIX_TC29X_BC_PB_CAN_ENHANCED_REL-355_V420	26-02-2018	MR	Rel-355 V4.2.0
TC297 BB	MC-ISAR_AS4XX_AURIX_TC29X_BB_PB_ETH_ENHANCED_V220	02-03-2018	MR	Rel-357 V2.2.0
TC27x CA	MC-ISAR_AURIX_TC27X_CA_<PACKAGE_NAME>_PB_V600_REL368	06-04-2018	MR	Rel-368 V6.0.0
TC27x DB	MC-ISAR_AURIX_TC27X_DB_<PACKAGE_NAME>_PB_V600_REL370	06-04-2018	MR	Rel-370 V6.0.0
TC27x DC	MC-ISAR_AURIX_TC27X_DC_<PACKAGE_NAME>_PB_V600_REL378	06-04-2018	MR	Rel-378 V6.0.0
TC23x_AC	MC-ISAR_<AS_VER>_AURIX_TC23X_AC_PB_<PACKAGE_NAME>_V300_REL374	17-08-2018	MR	Rel-374 V3.0.0
TC23x_AC	MC-ISAR_<AS_VER>_AURIX_TC23X_AC_PB_<PACKAGE_NAME>_V300_REL374_CANENC	17-08-2018	MR	Rel-374_CANENC V3.0.0
TC23x_AB	MC-ISAR_<AS_VER>_AURIX_TC23X_AB_PB_<PACKAGE_NAME>_V600_REL372	17-08-2018	MR	Rel-372 V6.0.0
TC22x_AC	MC-ISAR_<AS_VER>_AURIX_TC22X_AC_PB_<PACKAGE_NAME>_V300_REL-380	17-08-2018	MR	Rel-380 V3.0.0
TC21x_AC	MC-ISAR_<AS_VER>_AURIX_TC21X_AC_PB_<PACKAGE_NAME>_V300_REL-380	17-08-2018	MR	Rel-380 V3.0.0

TC22x_AB	MC-ISAR_<AS_VER>_AURIX_TC22X_AB_PB_<PACKAGE_NAME>_V500_REL-376	17-08-2018	MR	Rel376 V5.0.0
TC21x_AB	MC-ISAR_<AS_VER>_AURIX_TC21X_AB_PB_<PACKAGE_NAME>_V500_REL-376	17-08-2018	MR	Rel-376 V5.0.0
TC26x_BB	MC-ISAR_<AS_VER>_AURIX_TC26X_BB_PB_<PACKAGE_NAME>_V500_REL-400	14-12-2018	MR	Rel-400 V5.0.0
TC26x_BC	MC-ISAR_<AS_VER>_AURIX_TC26X_BC_PB_<PACKAGE_NAME>_V300_REL-400	14-12-2018	MR	Rel-400 V3.0.0
TC29x_BC	MC-ISAR_<AS_VER>_AURIX_TC29X_BC_PB_<PACKAGE_NAME>_V600_REL-405	29-07-2019	MR	Rel-405 V6.0.0
TC29x_BB	MC-ISAR_<AS_VER>_AURIX_TC29X_BB_PB_<PACKAGE_NAME>_V600_REL-405	29-07-2019	MR	Rel-405 V6.0.0
TC27x_DC	MC-ISAR_<AS_VER>_AURIX_TC27X_DC_PB_<PACKAGE_NAME>_V700_REL-405	29-07-2019	MR	Rel-405 V7.0.0
TC27x_DB	MC-ISAR_<AS_VER>_AURIX_TC27X_DB_PB_<PACKAGE_NAME>_V700_REL-405	29-07-2019	MR	Rel-405 V7.0.0
TC27x_CA	MC-ISAR_<AS_VER>_AURIX_TC27X_CA_PB_<PACKAGE_NAME>_V700_REL-405	29-07-2019	MR	Rel-405 V7.0.0
TC21x_AB	MC-ISAR_<AS_VER>_AURIX_TC21X_AB_PB_<PACKAGE_NAME>_V600_REL-410	03-03-2020	MR	Rel-410 V6.0.0
TC21x_AC	MC-ISAR_<AS_VER>_AURIX_TC21X_AC_PB_<PACKAGE_NAME>_V400_REL-410	03-03-2020	MR	Rel-410 V4.0.0
TC22x_AB	MC-ISAR_<AS_VER>_AURIX_TC22X_AB_PB_<PACKAGE_NAME>_V600_REL-410	03-03-2020	MR	Rel-410 V6.0.0
TC22x_AC	MC-ISAR_<AS_VER>_AURIX_TC22X_AC_PB_<PACKAGE_NAME>_V400_REL-410	03-03-2020	MR	Rel-410 V4.0.0
TC23x_AB	MC-ISAR_<AS_VER>_AURIX_TC23X_AB_PB_<PACKAGE_NAME>_V700_REL-410	03-03-2020	MR	Rel-410 V7.0.0
TC23x_AC	MC-ISAR_<AS_VER>_AURIX_TC23X_AC_PB_<PACKAGE_NAME>_V400_REL-410	03-03-2020	MR	Rel-410 V4.0.0
TC22XAB CANENC_LINEN	MC-ISAR_AS4XX_AURIX_TC22X_AB_PB_BASE_V100_REL-410	03-03-2020	MR	Rel-410 V1.0.0

C	MC-ISAR_AS4XX_AURIX_TC22X_AB_PB_COM_BASIC_V100_REL-410 MC-ISAR_AS4XX_AURIX_TC22X_AB_PB_MEM_V100_REL-410			
TC22XAC CANENC_LINENC	MC-ISAR_AS4XX_AURIX_TC22X_AC_PB_BASE_V100_REL-410 MC-ISAR_AS4XX_AURIX_TC22X_AC_PB_COM_BASIC_V100_REL-410 MC-ISAR_AS4XX_AURIX_TC22X_AC_PB_MEM_V100_REL-410	03-03-2020	MR	Rel-410 V1.0.0
TC23XAC CANENC	MC-ISAR_AS4XX_AURIX_TC23X_AC_PB_BASE_V400_REL-410 MC-ISAR_AS4XX_AURIX_TC23X_AC_PB_COM_BASIC_V400_REL-410 MC-ISAR_AS4XX_AURIX_TC23X_AC_PB_MEM_V400_REL-410	03-03-2020	MR	Rel-410 V4.0.0
TC29x_BC	MC-ISAR_<AS_VER>_AURIX_TC29X_BC_PB_<PACKAGE_NAME>_V700_REL-415	12-10-2020	MR	Rel-415 V7.0.0
TC29x_BB	MC-ISAR_<AS_VER>_AURIX_TC29X_BB_PB_<PACKAGE_NAME>_V700_REL-415	12-10-2020	MR	Rel-415 V7.0.0
TC27x_DC	MC-ISAR_<AS_VER>_AURIX_TC27X_DC_PB_<PACKAGE_NAME>_V800_REL-415	12-10-2020	MR	Rel-415 V8.0.0
TC27x_DB	MC-ISAR_<AS_VER>_AURIX_TC27X_DB_PB_<PACKAGE_NAME>_V800_REL-415	12-10-2020	MR	Rel-415 V8.0.0
TC27x_CA	MC-ISAR_<AS_VER>_AURIX_TC27X_CA_PB_<PACKAGE_NAME>_V800_REL-415	12-10-2020	MR	Rel-415 V8.0.0
TC26x_BB	MC-ISAR_<AS_VER>_AURIX_TC26X_BB_PB_<PACKAGE_NAME>_V600_REL-415	12-10-2020	MR	Rel-415 V6.0.0
TC26x_BC	MC-ISAR_<AS_VER>_AURIX_TC26X_BC_PB_<PACKAGE_NAME>_V400_REL-415	12-10-2020	MR	Rel-415 V4.0.0
TC21x_AB	MC-ISAR_<AS_VER>_AURIX_TC21X_AB_PB_<PACKAGE_NAME>_V710_REL-420.1	06-05-2021	MR	Rel-420.1* V7.1.0

TC21x_AC	MC-ISAR_<AS_VER>_AURIX_TC21X_AC_PB_<PACKAGE_NAME>_V510_REL-420.1	06-05-2021	MR	Rel-420.1* V5.1.0
TC22x_AB	MC-ISAR_<AS_VER>_AURIX_TC22X_AB_PB_<PACKAGE_NAME>_V710_REL-420.1	06-05-2021	MR	Rel-420.1* V7.1.0
TC22x_AC	MC-ISAR_<AS_VER>_AURIX_TC22X_AC_PB_<PACKAGE_NAME>_V510_REL-420.1	06-05-2021	MR	Rel-420.1* V5.1.0
TC23x_AB	MC-ISAR_<AS_VER>_AURIX_TC23X_AB_PB_<PACKAGE_NAME>_V810_REL-420.1	06-05-2021	MR	Rel-420.1* V8.1.0
TC23x_AC	MC-ISAR_<AS_VER>_AURIX_TC23X_AC_PB_<PACKAGE_NAME>_V510_REL-420.1	06-05-2021	MR	Rel-420.1* V5.1.0
TC23XAC CANENC	MC-ISAR_AS4XX_AURIX_TC23X_AC_PB_BASE_V510_REL-420.1 MC-ISAR_AS4XX_AURIX_TC23X_AC_PB_COM_BASIC_V510_REL-420.1 MC-ISAR_AS4XX_AURIX_TC23X_AC_PB_MEM_V510_REL-420.1	06-05-2021	MR	Rel-420.1* V5.1.0
TC29x_BC	MC-ISAR_<AS_VER>_AURIX_TC29X_BC_PB_<PACKAGE_NAME>_V800_REL-425	06-10-2021	MR	Rel-425 V8.0.0
TC29x_BB	MC-ISAR_<AS_VER>_AURIX_TC29X_BB_PB_<PACKAGE_NAME>_V800_REL-425	06-10-2021	MR	Rel-425 V8.0.0
TC27x_DC	MC-ISAR_<AS_VER>_AURIX_TC27X_DC_PB_<PACKAGE_NAME>_V900_REL-425	06-10-2021	MR	Rel-425 V9.0.0
TC27x_DB	MC-ISAR_<AS_VER>_AURIX_TC27X_DB_PB_<PACKAGE_NAME>_V900_REL-425	06-10-2021	MR	Rel-425 V9.0.0
TC27x_CA	MC-ISAR_<AS_VER>_AURIX_TC27X_CA_PB_<PACKAGE_NAME>_V900_REL-425	06-10-2021	MR	Rel-425 V9.0.0
TC26x_BB	MC-ISAR_<AS_VER>_AURIX_TC26X_BB_PB_<PACKAGE_NAME>_V700_REL-425	06-10-2021	MR	Rel-425 V7.0.0
TC26x_BC	MC-ISAR_<AS_VER>_AURIX_TC26X_BC_PB_<PACKAGE_NAME>_V500_REL-425	06-10-2021	MR	Rel-425 V5.0.0

Scope of Release Notes Addendum

Note:

<PACKAGE_NAME> = BASE / COM_BASIC / COM_ENHANCED / MEM / CD / DEMOCD / LIB / STDLIN_COMPLEX
<CFG_TYPE> = PB (All except LIB) / PC (Only LIB)
<AS_VER> = AS3XX / AS4XX
*Due to crypto file corruption noticed in Rel-420, Productive patch release Rel-420.1 with the fix was released.

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1 Known Issues Details

This section summarizes all Known Issues Details identified.
Refer *"MC-ISAR_AURIX_ReleaseNotes_Addendum.xlsm"* document provided in the "*MC-ISAR_AURIX_Releasenotes_Addendum.zip*" folder for more details.

2 Derivative Specification

This section explains the supported derivatives and affected modules with respect to derivative.

2.1 Supported Derivatives

1) Supported derivatives for TC27X_CA and TC27X_DB are:

1. SAK-TC275TP-64F200W 2. SAK-TC275TC-64F200W 3. SAK-TC275T-64F200W 4. SAL-TC275TP-64F200W 5. SAL-TC275T-64F200W	1. SAK-TC277TP-64F200S 2. SAK-TC277TC-64F200S 3. SAK-TC277T-64F200S

2) Supported derivatives for TC27X_DC

1. SAL-TC270TP-64F200N	1. SAK-TC275T-64F200N 2. SAK-TC275T-64F200W 3. SAK-TC275TP-64F200N 4. SAL-TC275TP-64F200N 5. SAK-TC275TP-64F200W 6. SAL-TC275TP-64F200W 7. SAK-TC275TC-64F200W 8. SAK-TC275TC-64F200N	1. SAK-TC277T-64F200S 2. SAL-TC277T-64F200S 3. SAK-TC277T-64F200N 4. SAK-TC277TP-64F200N 5. SAL-TC277TP-64F200N 6. SAK-TC277TP-64F200S 7. SAK-TC277TC-64F200N 8. SAK-TC277TC-64F200S

3) Supported derivatives for TC29x_BB are:

1. SAL-TC290TP-128F300 2. SAL-TC290TC-96F300	1. SAK-TC297TP-128F300S 2. SAK-TC297T-128F300S 3. SAK-TC297TP-96F300S 4. SAK-TC297TC-96F300S 5. SAK-TC297T-96F300S 6. SAK-TC297TX-128F300S 7. SAK-TC297TY-128F300S 8. SAK-TC297TA-128F300S 9. SAK-TC297TB-128F300S 10. SAK-TC297TA-64F300S	1. SAL-TC299TP-128F300S 2. SAK-TC299TP-128F300S 3. SAK-TC299T-128F300S 4. SAK-TC299TC-96F300S 5. SAK-TC299TX-128F300S 6. SAK-TC299TY-128F300S
1. SAL-TC298TP-128F300L		

4) Supported derivatives for TC29x_BC are:

1. SAK-TC297TA-64F300S

2. SAK-TC297TB-64F300S 3. SAK-TC297TX-128F300N 4. SAK-TC297TY-128F300S 5. SAK-TC297TA-128F300N 6. SAK-TC297TB-128F300S

5) Supported derivatives for TC26x_BB are:

1. SAL-TC260D-40F200	1. SAK-TC264D-40F200W 2. SAK-TC264DC-40F200W 3. SAL-TC264D-40F200W 4. SAK-TC264DA-40F200W	1. SAK-TC265D-40F200W 2. SAK-TC265DC-40F200W 3. SAL-TC265D-40F200W
1. SAK-TC267D-40F200S 2. SAL-TC267D-40F200S		

6) Supported derivatives for TC26x_BC are:

1. SAL-TC260D-40F200N	1. SAK-TC264DC-40F200W 2. SAK-TC264D-40F200N 3. SAL-TC264D-40F200N 4. SAK-TC264D-40F200W 5. SAK-TC264DA-40F200N 6. SAK-TC264DA-40F200W 7. SAK-TC264DE-40F200Q	1. SAK-TC265DC-40F200W 2. SAK-TC265D-40F200N 3. SAL-TC265D-40F200N 4. SAK-TC265D-40F200W 5. SAK-TC265DE-40F200Q
1. SAK-TC267D-40F200N 2. SAL-TC267D-40F200N 3. SAK-TC267D-40F200S		

7) Supported derivatives for TC23x_AB are:

1. SAK-TC233L-32F200F 2. SAK-TC233L-16F200F 3. SAL-TC233L-32F200F 4. SAL-TC233LP-16F200F 5. SAK-TC233LP-32F200F 6. SAL-TC233LP-32F200F 7. SAK-TC233LP-16F200F 8. SAK-TC233LC-24F133F	1. SAK-TC234L-32F200F 2. SAL-TC234L-32F200F 3. SAK-TC234LP-32F200F 4. SAL-TC234LP-16F200F 5. SAL-TC234LP-32F200F 6. SAK-TC234LP-16F200F	1. SAK-TC237L-32F200S 2. SAL-TC237L-32F200S 3. SAK-TC237LP-32F200S 4. SAL-TC237LP-32F200S

8) Supported derivatives for TC23x_AC are:

1. SAK-TC233LP-32F200N 2. SAL-TC233LP-32F200N 3. SAK-TC233L-32F200N 4. SAK-TC233LP-16F200N 5. SAK-TC233LC-24F133F 6. SAK-TC233LP-32F200F 7. SAL-TC233LP-32F200F 8. SAK-TC233S-32F200N 9. SAL-TC233L-32F200F 10. SAK-TC233L-32F200F 11. SAK-TC233LP-16F200F 12. SAK-TC233SP-32F200N 13. SAK-TC233LP-24F200N	1. SAK-TC234LP-32F200N 2. SAK-TC234L-32F200N 3. SAK-TC234LP-16F200F 4. SAK-TC234L-24F200F 5. SAK-TC234L-24F200N 6. SAK-TC234LC-24F133F 7. SAK-TC234LP-24F200F 8. SAK-TC234L-32F200F 9. SAK-TC234LP-32F200F	1. SAK-TC237LP-32F200N 2. SAL-TC237LP-32F200N 3. SAK-TC237L-32F200S 4. SAK-TC237LP-32F200S 5. SAL-TC237LP-32F200S

9) Supported derivatives for TC22x_AB are:

1. SAK-TC222L-16F133F 2. SAL-TC222L-16F133F 3. SAK-TC222S-16F133F 4. SAK-TC222L-12F133F 5. SAK-TC222S-12F133F	1. SAK-TC223L-16F133F 2. SAL-TC223L-16F133F 3. SAK-TC223S-16F133F 4. SAK-TC223S-12F133F 5. SAK-TC223L-12F133F	1. SAK-TC224L-16F133F 2. SAL-TC224L-16F133F 3. SAK-TC224S-16F133F

10) Supported derivatives for TC21x_AB are:

1. SAK-TC212L-8F133F 2. SAK-TC212S-8F133F 3. SAL-TC212L-8F133F	1. SAK-TC213L-8F133F 2. SAK-TC213S-8F133F 3. SAL-TC213L-8F133F	1. SAK-TC214L-8F133F 2. SAK-TC214S-8F133F 3. SAL-TC214L-8F133F

2.2 Derivative Restriction

1) Derivate Restrictions for TC27X_CA and TC27X_DB are:

#	Module	Description
1	CAN	For the devices SAK-TC277TC-64F200S and SAK-TC275TC-64F200W, CAN FD feature is not present. Hence it is not expected to configure CAN FD related parameters.
2	ETH	For the devices SAK-TC277TC-64F200S and SAK-TC275TC-64F200W, Ethernet module is not present. Hence it is not expected to configure Ethernet related parameters.
3	FLS	For the devices SAK-TC277TC-64F200S and SAK-TC275TC-64F200W, FlsTotalSize must not exceed 147456 (decimal value for 144KB)

2) Derivate Restrictions for TC26X_BB are:

#	Module	Description
1	CAN	For the devices SAK-TC265DC-40F200W and SAK-TC264DC-40F200W, CAN FD feature is not present. Hence it is not expected to configure CAN FD related parameters.
2	ETH	For the devices SAK-TC265DC-40F200W and SAK-TC264DC-40F200W, Ethernet module is not present. Hence it is not expected to configure Ethernet related parameters.
3	FLS	For the devices SAK-TC265DC-40F200W and SAK-TC264DC-40F200W, FlsTotalSize must not exceed 65536 (decimal value for 64KB)
4	MCU	MCU Standby Mode is not available for the given derivatives : SAK-TC265DC-40F200W, SAK-TC264DC-40F200W.

3) Derivate Restrictions for TC29X_BB are:

#	Module	Description
1	CAN	For the devices SAK-TC299TC-96F300S, SAK-TC297TC-96F300S and SAL-TC290TC-96F300, CAN FD feature is not present. Hence it is not expected to configure CAN FD related parameters.
2	ETH	For the devices SAK-TC299TC-96F300S, SAK-TC297TC-96F300S and SAL-TC290TC-96F300, Ethernet module is not present. Hence it is not expected to configure Ethernet related parameters.
3	ERAY	For the devices SAK-TC299TC-96F300S, SAK-TC297TC-96F300S and SAL-TC290TC-96F300, Only one ERAY controller is present. Hence it is not expected to configure the second ERAY controller.
4	FLSLOADER	Flash Size is 6MB for the given derivatives : SAK-TC299TC-96F300S, SAK-TC297TP-96F300S, SAK-TC297TC-96F300S, SAK-TC297T-96F300S, SAL-TC290TC-96F300.
5	FLS	For the devices SAK-TC299TC-96F300S, SAK-TC297TC-96F300S and SAL-TC290TC-96F300, FlsTotalSize must not exceed 196608 (decimal value for 192KB)

4) Derivate Restrictions for TC23X_AB are:

#	Module	Description
1	MCU	CPU frequency is 133 MHz for SAK-TC233LC-24F133F AB For rest TC23x_AB derivatives it is 200 MHz
2	FLSLOADER	Flash Size is 1 MB for the given derivatives : SAK-TC234LP-16F200F, SAK-TC233L-16F200F, SAK-TC233LP-16F200F SAL-TC234LP-16F200F, SAL-TC233LP-16F200F Flash Size is 1.5 MB for the given derivative : SAK-TC233LC-24F133F

5) Derivate Restrictions for TC22X_AB are:

#	Module	Description
1	FLSLOADER	Flash Size is 0.75 MB for the given derivatives : SAK-TC223S-12F133F, SAK-TC222S-12F133F, SAK-TC223L-12F133F SAK-TC222L-12F133F

6) Derivate Restrictions for TC21X_AB are:

#	Module	Description
-	-	-

3 Safety mechanism to be considered by customer

The Aurix Safety Manual [AURIX Safety Manual_V1.4.pdf, 2015-11, Infineon Technologies AG Munich] lists the safety mechanisms for each functional part of the AURIX microcontroller architecture and state the assumptions related to the use of each safety mechanism.

For few AoU's the MCAL Implementation hints are provided below.

3.1 Interrupt source check *

SMU ID	SM1[AoU].IR:SrcCheck
Short Description	Interrupt plausibility check, to detect unexpected triggering of service requests or call of a wrong ISR, based on additional information from the interrupt source.
Applicable to MCAL	Yes

Comments	The customer shall implement Interrupt source check for overall software and for the existing MCAL software, Interrupt source check has to be done in the respective module IRQ file, before the call of MCAL interrupt handle as per AoU in AURIX Safety Manual.
	Hint: As an example, In Spi_Irq.c file before calling Spi_IsrQspiPt(SPI_QSPI0_INDEX) (Phase transition interrupt handler which is invoked at the end of the last channel of last job in a sequence.)following changes has to be done in QSPI0PT_ISR(QSPI0 PT2interrupt)
	/* Check the QSPI0 status register */
	if(SPI_HW_BASE[0].STATUS.B.PT2F == 1U)
	{
	/* Call QSPI0 Interrupt function*/
	Spi_IsrQspiPt(SPI_QSPI0_INDEX);
	/* Clear the PT2F event flag via FLAGSCLEAR register */
	SPI_HW_BASE[0].FLAGSCLEAR.B.PT2C = 1U;
	}
	
	Where #define SPI_HW_BASE ((volatile Ifx_QSPI *)(void *) &(MODULE_QSPI0))

***Applicable only for Rel180, Rel185, Rel190**

3.2 QSPI Protection

SMU ID	SM1[AoU].QSPI:SafeProtocol
Short Description	Safety mechanism to detect the following errors: - Baud Rate Error Detection - Spike Detection
Applicable to MCAL	Yes
Comments	Assumption of Use shall be implemented in all safety related SPI communication which uses QSPI slave loop back mechanism.

3.3 DMA Monitor

SMU ID	SM1[AoU].DMA:Monitor
Short Description	The application software shall verify the integrity of data transferred by DMA.
Applicable to MCAL	Yes
Comments	The Customer shall implement safety mechanism specified in AURIX safety Manual. Hint : Use SPI loop back mechanism or an equivalent safety mechanism.

3.4 Watchdog Timer Initialization Check

SMU ID	SM2[AoU].WDT:InitCheck
Short Description	To detect permanent failures in the configuration registers of the watchdog Timers, the user shall implement a software level safety mechanism verifying the correct watchdog configuration, after initial software initialization and every subsequent configuration change.
Applicable to MCAL	Yes
Comments	The customer shall read and verify Watchdog configuration registers after initialization or mode change to ensure the reload values and other configurations are valid.

3.5 Register Based DMA

SMU ID	SM_AURIX_DMA_5
Short Description	TC23x, TC22x, and TC21x series implement a register-based DMA instead of the SRAM-based DMA of the other series. For these devices, the increased failure rate, related to soft errors in configuration registers, shall be considered by the application. Rationale: in a register-based DMA, the transaction control set of each channel is not monitored by ECC as it is in a SRAM-based DMA.
Applicable to MCAL	Yes
Comments	Dedicated measures on system level are needed. Hint: SDCRC, E2E for DMA transaction.

4 AoU's of Aurix Hardware Safety Manual V1.2, V1.3,V1.4 and V1.5.1

4.1 AoU's considered from AURIX Safety Manual V1.2 2015-01 and AURIX Safety Manual v1.2 Addendum V2.0, 2015-04

AoU ID	Comments/Implementation hints from MCAL
SM1[AoU].CPU:SoftErrorMon	Not Implemented and not applicable for current delivery. CPU error monitoring is not in the scope of MCAL. E.g.: Plausibility check not done at driver level.
SM1[AoU].CPU:SBST	Not Implemented and not applicable for current delivery. CPU Software Based Self-Test is not in the scope of MCAL
SM1[AoU].SPB:TEST	Not Implemented and not applicable for current delivery. SPB Test Pattern is not in the scope of MCAL
SM1[AoU].STM:Plausibility	Not Implemented and not applicable for current delivery. MCAL module doesn't use STM, it is OS/application software to take care.
SM1[AoU].WDT:TIMEOUT	Not Implemented and not applicable for current delivery. Deadline monitoring is part of WDG Manager. WDG driver only provides an interface to service the WDG.
SM1[AoU].WDT:PFM	Not Implemented and not applicable for current delivery. Program flow monitoring is part of WDG Manager. WDG driver only provides an interface to service the WDG.
SM1[AoU].ExtWDT	Not Implemented and not applicable for current delivery. The prerequisite to safety concept of MCAL is system should have SafeTlib/equivalent Software. The SafeTlib/equivalent software shall support monitoring with external watchdog.
SM1[AoU].IR:Monitor	Not Implemented and not applicable for current delivery. Interrupt subsystem is assigned to OS and hence this AoU shall be taken care by OS.
SM1[AoU].IR:SrcCheck	Not Implemented in MCAL but needs implementation for correct usage of MCAL. The customer shall implement Interrupt source check for overall software and for the existing MCAL software, Interrupt source check has to be done in the respective module IRQ file, before the call of MCAL interrupt handle as per AoU. Hint: As an example, In Spi_Irq.c file before calling Spi_IsrQspiPt(SPI_QSPI0_INDEX) (Phase transition interrupt handler which is invoked at the end of the last channel of last job in a sequence.)following changes has to be done in

	QSPI0PT_ISR(QSPI0 PT2interrupt)
	/* Check the QSPI0 status register */
	if(SPI_HW_BASE[0].STATUS.B.PT2F == 1U)
	{
	/* Call QSPI0 Interrupt function*/
	Spi_IsrQspiPt(SPI_QSPI0_INDEX);
	/* Clear the PT2F event flag via FLAGSCLEAR register */
	SPI_HW_BASE[0].FLAGSCLEAR.B.PT2C = 1U;
	}
	
	Where #define SPI_HW_BASE ((volatile Ifx_QSPI *)(void *) &(MODULE_QSPI0))

SM1[AoU].DMA:Monitor	Not Implemented in MCAL but needs implementation for correct usage of MCAL. The Customer shall implement safety mechanism specified in AURIX safety Manual. Hint: Use SPI loop back mechanism or an equivalent safety mechanism. If SPI loop back mechanism is used then the application software shall verify the integrity of data transferred by DMA.
SM1[AoU].CAN: SafeProtocol, SM1[AoU].ERAY: SafeProtocol, SM1[AoU].ETH: SafeProtocol	Not Implemented in MCAL but needs implementation for correct usage of MCAL.
SM1[AoU].QSPI: SafeProtocol	Not Implemented in MCAL but needs implementation for correct usage of MCAL.
SM1[AoU].EVR:CFGMON	Not Implemented and not applicable for current delivery. EVR configuration monitor is not part of MCAL.
SM2[AoU].CPU:LOCKSTEP.ALARM_TEST	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].CPU.TRAP:TEST	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].EVR:MON	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].EVR33:MON	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].EVR13:MON	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].ExtVREG:MON	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].CLK:CLKMON	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].SRAM:ECC	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].LMU.SRAM.ECC:MONITOR	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].SRAM:ADDRMON	Not Implemented and not applicable for current delivery. It is related to start-up test.

SM2[AoU].SRAM:Monitor	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].PFLASH:ECC	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].PFLASH:ADDRMON	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].PFLASH.EDC:CMP	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].PFLASH:Monitor	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].SRI:EDC	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].SRI:EH	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].SPB:EH	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].SPB:TIMEOUT	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].Register:SFF	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].Register:AP	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].STM:AP	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].DMA:AP	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].IR:AP	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].SBCU:AP	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].SMU:AP	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].FCE:AP	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].IOM:AP	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].PORT:AP	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].QSPI:AP	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].MSC:AP	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].CAN:AP	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].SENT:AP	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].ERAY:AP	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].GTM:AP	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].CCU6:AP	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].VADC:AP	Not Implemented and not applicable for current delivery. It

	is related to start-up test.
SM2[AoU].DSADC:AP	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].MTU:AP	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].SCU:AP	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].Ethernet:AP	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].HSSL:AP	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].PSI5:AP	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].SRI:AP	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].HSM:AP	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].CIF:AP	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].I2C:AP	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].CPU.MPU:TEST	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].CPU.BUS.MPU:TEST	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].CPU.AP:TEST	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].WDT:TEST	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].RESET:SSCheck	Not Implemented and not applicable for current delivery. It is related to start-up sw. In MCAL start-up software is a demo file(Mcal.c)
SM2[AoU].SBCU:InitCheck	Not Implemented and not applicable for current delivery.
SM2[AoU].SMU.FSP:TEST	Not Implemented and not applicable for current delivery. It is related to start-up test
SM2[AoU].SMU:InitCheck	Not Implemented and not applicable for current delivery.
SM2[AoU].SMU.LOCK:TEST	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].SMU.ALARM:TEST	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].SMU:TEST	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].SMU.RT:TEST	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].CPU.MPU:InitCheck	Not Implemented and not applicable for current delivery.
SM2[AoU].CPU.BUS.MPU:InitCheck	Not Implemented and not applicable for current delivery.
SM2[AoU].LMU.MPU:InitCheck	Not Implemented and not applicable for current delivery.
SM2[AoU].WDT:InitCheck	Not Implemented in MCAL but needs implementation for correct usage of MCAL. Hint: The customer shall read and verify Watchdog configuration registers after initialization or mode change to ensure the reload values and other configurations are valid.

SM2[AoU].IR:EDC	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].DMA:TIMESTAMP	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].FCE:TEST	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].DMA.DATA:CRC32	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].DMA.ADDR:CRC32	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].LMU.MPU:TEST	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].LMU.AP:TEST	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].IOM:TEST	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].PSRAM:ECC	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].PSRAM:ADDRMON	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].PSRAM:Monitor	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM2[AoU].MTU:AP	Not Implemented and not applicable for current delivery. It is related to start-up test.
SM_AURIX_24	To be taken care by Integrator.
SM_AURIX_25	Not Implemented and not applicable for current delivery. Info to user.
SM_AURIX_17	Not Implemented and not applicable for current delivery. Info to user.
SM_AURIX_18	Not Implemented and not applicable for current delivery.
SM_AURIX_19	Not Implemented and not applicable for current delivery.
SM_AURIX_20	Not Implemented and not applicable for current delivery.
SM_AURIX_22	Not Implemented and not applicable for current delivery.
SM_AURIX_15	Not Implemented and not applicable for current delivery.
SM_AURIX_01	Not Implemented and not applicable for current delivery.
SM_AURIX_02	Not Implemented and not applicable for current delivery.
SM_AURIX_07	Not Implemented and not applicable for current delivery.
SM_AURIX_03	Not Implemented and not applicable for current delivery.
SM_AURIX_04	Not Implemented and not applicable for current delivery.
SM_AURIX_05	Not Implemented and not applicable for current delivery.
SM_AURIX_06	Not Implemented and not applicable for current delivery.
SM_AURIX_9	Not Implemented and not applicable for current delivery.
SM_AURIX_14	Implemented in MCAL (Needs evaluation of integrator for rest of the software)
SM_AURIX_16	Not Implemented and not applicable for current delivery.
SM_AURIX_DEBUG_1	Not Implemented and not applicable for current delivery.
SM_AURIX_DEBUG_2	Not Implemented and not applicable for current delivery.
SM_AURIX_08	Not Implemented in MCAL but needs implementation for correct usage of MCAL
SM_AURIX_FFI_2	Not Implemented and not applicable for current delivery.

SM_AURIX_ISR_1	Not Implemented and not applicable for current delivery. IRQ is the responsibility of user / OS
SM_AURIX_FFI_3	Not Implemented and not applicable for current delivery.
SM_AURIX_OVC_1	Not Implemented and not applicable for current delivery.
SM_AURIX_SMU_4	Not Implemented and not applicable for current delivery. From MCAL only configuration is provided
SM_AURIX_SMU_5	Implemented in MCAL (Needs evaluation of integrator for rest of the software). Configuration possibility provided.
SM_AURIX_SMU_3	Not Implemented and not applicable for current delivery.
SM_AURIX_SMU_2	Not Implemented and not applicable for current delivery.
SM_AURIX_CPU_1	Not Implemented and not applicable for current delivery.
SM_AURIX_CPU_2	Not Implemented and not applicable for current delivery.
SM_AURIX_NLSCPU_4	Not Implemented and not applicable for current delivery.
SM_AURIX_NLSCPU_5	Not Implemented and not applicable for current delivery.
SM_AURIX_NLCPU_3	Not Implemented and not applicable for current delivery.
SM_AURIX_NLCPU_2	Not Implemented and not applicable for current delivery.
SM_AURIX_PMC_1	Not Implemented and not applicable for current delivery.
SM_AURIX_EVR_1	Not Implemented and not applicable for current delivery.
SM_AURIX_EVR_2	Not Implemented and not applicable for current delivery.
SM_AURIX_EVR_4	Not Implemented and not applicable for current delivery.
SM_AURIX_RCU_1	Not Implemented and not applicable for current delivery.
SM_AURIX_RCU_2	Not Implemented and not applicable for current delivery.
SM_AURIX_CCU_1	Not Implemented and not applicable for current delivery.
SM_AURIX_CCU_2	Not Implemented and not applicable for current delivery.
SM_AURIX_WDT_1	Not Implemented and not applicable for current delivery.
SM_AURIX_SRI_1	Not Implemented and not applicable for current delivery.
SM_AURIX_SRI_2	Not Implemented and not applicable for current delivery.
SM_AURIX_SPB_1	Not Implemented and not applicable for current delivery.
SM_AURIX_SPB_2	Not Implemented and not applicable for current delivery.
SM_AURIX_SPB_3	Not Implemented and not applicable for current delivery.
SM_AURIX_CPU_3	Not Implemented and not applicable for current delivery.
SM_AURIX_CPU_4	Not Implemented and not applicable for current delivery.
SM_AURIX_SHARED_SRAMS	Not Implemented and not applicable for current delivery.
SM_AURIX_NLCPU_4	Not Implemented and not applicable for current delivery.
SM_AURIX_NLCPU_5	Not Implemented and not applicable for current delivery.
SM_AURIX_LMU_1	Not Implemented and not applicable for current delivery.
SM_AURIX_LMU_2	Not Implemented and not applicable for current delivery.
SM_AURIX_PMU_1	Not Implemented and not applicable for current delivery.
SM_AURIX_PMU_2	Not Implemented and not applicable for current delivery.
SM_AURIX_PMU_3	Not Implemented and not applicable for current delivery.
SM_AURIX_PMU_4	Not Implemented and not applicable for current delivery.
SM_AURIX_DMA_1	Not Implemented and not applicable for current delivery.
SM_AURIX_DMA_2	Not Implemented and not applicable for current delivery.
SM_AURIX_DMA_3	Not Implemented in MCAL but needs implementation for correct usage of MCAL. The Customer shall implement safety mechanism specified in AURIX safety Manual. Hint: Use SPI

	loop back mechanism or an equivalent safety mechanism
SM_AURIX_DMA_4	Not Implemented and not applicable for current delivery.
SM_AURIX_DMA_5	Not Implemented in MCAL but needs implementation for correct usage of MCAL. Dedicated measures on system level are needed. Hint: SDCRC, E2E for DMA transaction.
SM_AURIX_STM_1	Not Implemented and not applicable for current delivery.
SM_AURIX_STM_2	Not Implemented and not applicable for current delivery.
SM_AURIX_STM_3	Not Implemented and not applicable for current delivery.
SM_AURIX_IR_1	Not Implemented and not applicable for current delivery.
SM_AURIX_IR_2	Not Implemented and not applicable for current delivery.
SM_AURIX_IR_3	Not Implemented in MCAL but needs implementation for correct usage of MCAL.
SM_AURIX_CAN_2	Not Implemented and not applicable for current delivery.
SM_AURIX_CAN_1	Not Implemented and not applicable for current delivery.
SM_AURIX_CAN_3	Not Implemented in MCAL but needs implementation for correct usage of MCAL.
SM_AURIX_CAN_4	Not Implemented and not applicable for current delivery
SM_AURIX_ERAY_2	Not Implemented and not applicable for current delivery
SM_AURIX_ERAY_1	Not Implemented and not applicable for current delivery
SM_AURIX_ERAY_3	Not Implemented in MCAL but needs implementation for correct usage of MCAL.
SM_AURIX_ERAY_4	Not Implemented and not applicable for current delivery
SM_AURIX_QSPI_4	Not Implemented and not applicable for current delivery
SM_AURIX_QSPI_1	Not Implemented and not applicable for current delivery
SM_AURIX_QSPI_2	Not Implemented and not applicable for current delivery
SM_AURIX_QSPI_3	Not Implemented in MCAL but needs implementation for correct usage of MCAL.
SM_AURIX_SERIAL_COMM_1	Not Implemented and not applicable for current delivery
SM_AURIX_ADC_4	Implemented in MCAL. (Needs evaluation of integrator for rest of the software)
SM_AURIX_ADC_5	Implemented in MCAL. (Needs evaluation of integrator for rest of the software)
SM_AURIX_ADC_1	Not Implemented and not applicable for current delivery
SM_AURIX_ADC_2	Implemented in MCAL. (Needs evaluation of integrator for rest of the software)
SM_AURIX_ADC_3	Implemented in MCAL. (Needs evaluation of integrator for rest of the software)
SM_AURIX_DIO_1	Not Implemented and not applicable for current delivery
SM_AURIX_DIO_2	Not Implemented and not applicable for current delivery
SM_AURIX_IOM_1	Not Implemented and not applicable for current delivery
SM_AURIX_IOM_2	Not Implemented and not applicable for current delivery
SM_AURIX_GTM_1	Not Implemented and not applicable for current delivery
SM_AURIX_DIO_3	Implemented in MCAL. (Needs evaluation of integrator for rest of the software)
SM_AURIX_ADAS_1	Not Implemented and not applicable for current delivery
SM_AURIX_EXTVREG_TEST	Not Implemented and not applicable for current delivery
SM_AURIX_EVR_3	Not Implemented and not applicable for current delivery

SM_AURIX_EVR_5	Not Implemented and not applicable for current delivery
SM_AURIX_DFA_CLK_1	Not Implemented and not applicable for current delivery
SM_AURIX_DFA_CLK_2	Not Implemented and not applicable for current delivery
SM_AURIX_SRAM_INIT	Not Implemented and not applicable for current delivery
SM_AURIX_SRAM_ALM	Not Implemented and not applicable for current delivery
SM_AURIX_PSRAM_2	Not Implemented and not applicable for current delivery
SM_AURIX_PSRAM_3	Not Implemented and not applicable for current delivery
SM_AURIX_PMU_1:1	Not Implemented and not applicable for current delivery
SM_AURIX_PMU_1:4	Not Implemented and not applicable for current delivery
SM_AURIX_CPUCRC32_1	Not Implemented and not applicable for current delivery
SM_AURIX_AP_1	Not Implemented and not applicable for current delivery
SM_AURIX_ADC_2:1	Not Implemented and not applicable for current delivery
SM_AURIX_SRI_2:1	Not Implemented and not applicable for current delivery
SM_AURIX_DMA_2:1	Not Implemented and not applicable for current delivery
SM_AURIX_CPU_TRAP_TEST	Not Implemented and not applicable for current delivery
SM_AURIX_CPU_1:1	Not Implemented and not applicable for current delivery
SM_AURIX_CPU_1:2	Not Implemented and not applicable for current delivery
SM_AURIX_EVR_1:1	Not Implemented and not applicable for current delivery
SM_AURIX_CCU_1:1	Not Implemented and not applicable for current delivery
SM_AURIX_CPU_3:1	Not Implemented and not applicable for current delivery
SM_AURIX_LMU_1:1	Not Implemented and not applicable for current delivery
SM_AURIX_CPU_3:2	Not Implemented and not applicable for current delivery
SM_AURIX_CPU_3:3	Not Implemented and not applicable for current delivery
SM_AURIX_PMU_1:2	Not Implemented and not applicable for current delivery
SM_AURIX_PMU_1:6	Not Implemented and not applicable for current delivery
SM_AURIX_PMU_1:3	Not Implemented and not applicable for current delivery
SM_AURIX_PMU_1:5	Not Implemented and not applicable for current delivery
SM_AURIX_PMU_1:7	Not Implemented and not applicable for current delivery
SM_AURIX_SRI_1:1	Not Implemented and not applicable for current delivery
SM_AURIX_SRI_1:3	Not Implemented and not applicable for current delivery
SM_AURIX_SPB_1:3	Not Implemented and not applicable for current delivery
SM_AURIX_SPB_1:1	Not Implemented and not applicable for current delivery
SM_AURIX_SFF_TEST	Not Implemented and not applicable for current delivery
SM_AURIX_SPB_2:1	Not Implemented and not applicable for current delivery
SM_AURIX_CPU_2:1	Not Implemented and not applicable for current delivery
SM_AURIX_CPU_2:2	Not Implemented and not applicable for current delivery
SM_AURIX_2:3	Not Implemented and not applicable for current delivery
SM_AURIX_WDT_TEST	Not Implemented and not applicable for current delivery
SM_AURIX_RCU_2:1	Not Implemented and not applicable for current delivery
SM_AURIX_SPB_1:2	Not Implemented and not applicable for current delivery
SM_AURIX_SMU_2:1	Not Implemented and not applicable for current delivery
SM_AURIX_SMU_3:2	Not Implemented and not applicable for current delivery
SM_AURIX_SMU_3:3	Not Implemented and not applicable for current delivery
SM_AURIX_SMU_3:4	Not Implemented and not applicable for current delivery
SM_AURIX_SMU_TEST_1	Not Implemented and not applicable for current delivery

SM_AURIX_SMU_TEST_2	Not Implemented and not applicable for current delivery
SM_AURIX_CPU_MPU_INIT_1	Not Implemented and not applicable for current delivery
SM_AURIX_CPU_MPU_INIT_2	Not Implemented and not applicable for current delivery
SM_AURIX_LMU_MPU_INIT_1	Not Implemented and not applicable for current delivery
SM_AURIX_WDT_TEST:1	Not Implemented in MCAL but needs implementation for correct usage of MCAL. The customer shall read and verify Watchdog configuration registers after initialization or mode change to ensure the reload values and other configurations are valid.
SM_AURIX_IR_1:1	Not Implemented and not applicable for current delivery
SM_AURIX_DMA_TEST_1	Not Implemented and not applicable for current delivery
SM_AURIX_FCE_TEST_1	Not Implemented and not applicable for current delivery
SM_AURIX_FCE_TEST_2	Not Implemented and not applicable for current delivery
SM_AURIX_DMA_TEST_2	Not Implemented and not applicable for current delivery
SM_AURIX_LMU_MPU_TEST_1	Not Implemented and not applicable for current delivery
SM_AURIX_LMU_AP_TEST_1	Not Implemented and not applicable for current delivery
SM_AURIX_IOM_TEST_1	Not Implemented and not applicable for current delivery
SM_AURIX_PSRAM_1	Not Implemented and not applicable for current delivery
SM_AURIX_PSRAM_1:3	Not Implemented and not applicable for current delivery
SM_AURIX_PSRAM_1:2	Not Implemented and not applicable for current delivery
SM_AURIX_NLCPU_2:1	Not Implemented and not applicable for current delivery
SM_AURIX_NLCPU_2:2	Not Implemented and not applicable for current delivery
SM_AURIX_NLCPU_1	Not Implemented and not applicable for current delivery
SM_AURIX_SPB_3:1	Not Implemented and not applicable for current delivery
SM_AURIX_STM_3:1	Not Implemented and not applicable for current delivery
SM_AURIX_WDT_1:1	Not Implemented and not applicable for current delivery
SM_AURIX_WDT_1:2	Not Implemented and not applicable for current delivery
SM_AURIX_WDT_1:3	Not Implemented and not applicable for current delivery
SM_AURIX_IR_3:1	Not Implemented and not applicable for current delivery
SM_AURIX_IR_3:2	Not Implemented in MCAL but needs implementation for correct usage of MCAL. The customer shall implement Interrupt source check for overall software and for the existing MCAL software, Interrupt source check has to be done in the respective module IRQ file, before the call of MCAL interrupt handle as per AoU.
SM_AURIX_DMA_3:1	Not Implemented in MCAL but needs implementation for correct usage of MCAL. The Customer shall implement safety mechanism specified in AURIX safety Manual. Hint: Use SPI loop back mechanism or an equivalent safety mechanism. If SPI loop back mechanism is used then the application software shall verify the integrity of data transferred by DMA.
SM_AURIX_SAFE_COMM_1	Not Implemented in MCAL but needs implementation for correct usage of MCAL.
SM_AURIX_QSPI_3:1	Not Implemented in MCAL but needs implementation for correct usage of MCAL.
SM_AURIX_EVR_4:1	Not Implemented and not applicable for current delivery
SM_AURIX_26	Not Implemented and not applicable for current delivery

SM_AURIX_27	Not Implemented and not applicable for current delivery
SM_AURIX_28	Not Implemented and not applicable for current delivery
SM_AURIX_29	Not Implemented and not applicable for current delivery
SM_AURIX_DFA_1	Not Implemented and not applicable for current delivery
SM_AURIX_DFA_2	Not Implemented and not applicable for current delivery
SM_AURIX_DFA_3	Implemented in MCAL. (Needs evaluation of integrator for rest of the software)
SM_AURIX_23	To be taken care by Integrator.
SM_AURIX_ALARM_INIT_1	Not Implemented and not applicable for current delivery

4.2 AURIX Safety Manual V1.3 changes w.r.t V1.2

Change Description from Safety manual V1.2 to V1.3	Comments / Implementation hints from MCAL
[0000047041-113, 0000047041-157] Added section 3.10, SM_AURIX_DEBUG_1, SM_AURIX_DEBUG_2	NA for MCAL as it is related to On-Chip Debug Support (OCDS) module
[0000047041-110] Added information for initialization of safety mechanisms in sections 5.1.11, 5.1.12, 5.1.14, 5.1.15	Not in the scope of MCAL as it's a hardware safety mechanism.
[0000047041-161] Improved description of SM2[AoU].Reset:SSCheck in section 5.2.23	Not in the scope of MCAL as it is related to start-up software. In MCAL, start-up software is a demo(Mcal.c)
[0000047041-108, 0000047041-106, 0000047041-116] Added assumptions about PFLASH erase and programming: SM_AURIX_PMU_3, SM_AURIX_PMU_4, in section 4.17	NA for MCAL, System integrator has to take care.
[0000047041-103, 0000047041-104, 0000047041-105] Extended recommendations for the choice of independent redundant ADC channels, Timer channels, and QSPI channels, in section 7	NA for MCAL, as more description/text added to the existing method of using diverse modules as redundant channels
[0000047041-190] added new AoU SM_AURIX_DFA_CLK_2	Not in the scope of MCAL as its user responsibility to configure SMU to react to a clock monitor error with a system reset.
[0000047041-117] section 5.1.11: Enhanced Error Signalling, added new AoU SM_AURIX_SRAM_ALM	NA for MCAL, as it is related to start-up test
[0000047041-200] section 5.3.9: Added recommendation regarding unused SRN	Applicable and considered in MCAL. Only the configured modules SRE are enabled in the respective modules. The operating system to take care of remaining SRN bits.

[0000047041-196] section 4.17 :Improved SM_AURIX_PMU_4	NA for MCAL, System integrator has to take care.
[0000047041-185, 0000047041-151] section 5.1.25: Added recommendation about IR EDC failure mode coverage and for reaction to ALM2[25]	NA for MCAL, as it's a hardware safety mechanism.
[0000047041-165] section 5.3.8 :Added recommendation to check the content of SRC registers after write	NA for MCAL, Interrupt subsystem is assigned to OS and hence this AoU shall be taken care by OS.
[0000047041-189] section 5.2.26 :Extended SM_AURIX_SMU_3:2 with the list of registers to be considered	NA for MCAL as SMU initcheck is not part of MCAL.
[0000047041-153] Added additional hint about checking configuration registers after write in the description of SM1[AoU].SPB:TEST	NA for MCAL as SPB Test Pattern is not in the scope of MCAL
[0000047041-111] section 5.1.39: removed SRI Bus Error from "Error Signalling"	NA for MCAL chapter 5.1.39 is for hardware safety mechanism.
[0000047041-179, 0000047041-208] Removed all references to HSM:AP section 5.2.18, 5.2.19 corrected wording	Not in the scope of MCAL as it is related to start-up test
[0000047041-246, 0000047041-240, 0000047041-300] Section 5.2.45: SM_AURIX_EVR_4:1 Fixed description of SM1[AoU].EVR: CFGMON, and moved it to 5.2 (startup test).	Not in the scope of MCAL as it is related to start-up test
[0000047041-265] Requirement tagging issues, removed following requirements tags: SM_AURIX_FFI_2, SM_AURIX_PSRAM_2, SM_AURIX_PSRAM_3, SM_AURIX_CPU_TRAP_TEST, SM_AURIX_WDT_1:3, SM_AURIX_PMC_1, SM_AURIX_EVR_4, SM_AURIX_DMA_3, SM_AURIX_STM_3, SM_AURIX_IR_3, SM_AURIX_CAN_3, SM_AURIX_QSPI_3, SM_AURIX_RCU_2	NA to MCAL, removal of requirements tags.
[0000047041-272] improved wording of following AoUs (no change in the objectives): SM_AURIX_20, SM_AURIX_07, SM_AURIX_04, SM_AURIX_FFI_3, SM_AURIX_NLSCPU_4, SM_AURIX_PMU_1,	NA for MCAL. Description is provided below : SM_AURIX_20: NA for MCAL.Startup is responsibility of user SM_AURIX_07: NA for MCAL as this is a requirement on ECU design; responsibility of user. SM_AURIX_04: NA for MCAL as this is related to SMU SM_AURIX_FFI_3:

SM_AURIX_SHARED_SRAMS, SM_AURIX_PMU_3, SM_AURIX_PMU_4, SM_AURIX_DMA_4, SM_AURIX_DMA_5, SM_AURIX_IR_3, SM_AURIX_CAN_4, SM_AURIX_ERAY_4, SM_AURIX_GTM_1, SM_AURIX_EXTVREG_TEST, SM_AURIX_SRAM_INIT, SM_AURIX_CPU_1:1, SM_AURIX_CPU_1:2 SM_AURIX_EVR_1:1, SM_AURIX_CCU_1:1, SM_AURIX_CPU_3:1, SM_AURIX_CPU_3:2, SM_AURIX_PMU_1:6, SM_AURIX_SRI_1:3, SM_AURIX_SPB_2:1, SM_AURIX_CPU_2:1, SM_AURIX_CPU_2:2, SM_AURIX_WDT_TEST, SM_AURIX_SPB_1:2, SM_AURIX_SMU_2:1, SM_AURIX_SMU_3:2, SM_AURIX_CPU_MPU_INIT_1, SM_AURIX_CPU_MPU_INIT_2, SM_AURIX_DMA_TEST_1, SM_AURIX_FCE_TEST_1, SM_AURIX_DMA_TEST_2, SM_AURIX_LMU_MPU_TEST_1, SM_AURIX_PSRAM_1:2, SM_AURIX_NLCPU_1, SM_AURIX_IR_1, SM_AURIX_WDT_1:1 6 About Error Reaction and Fault Tolerance 7 About Dependent Failures Changed names of section 6 and 7: "6 About Error Reaction and Fault Tolerance" becomes "6 Error Reaction and Fault Tolerance Considerations" becomes "7 Dependent Failures Considerations"	NA for MCAL software as it's a hardware safety mechanism. SM_AURIX_NLSCPU_4: NA for MCAL as it is start-up self-tests. SM_AURIX_PMU_1: NA for MCAL software as it's a hardware safety mechanism. SM_AURIX_SHARED_SRAMS: NA for MCAL software as it's a hardware safety mechanism. SM_AURIX_PMU_3, SM_AURIX_PMU_4: NA for MCAL, Applicable for SafeTlib as reading back / checking of FSR for errors is part of SafeTlib. SM_AURIX_DMA_4: NA for MCAL as DMA SRAM errors leads to SMU alarm; configuration of alarm reaction is responsibility of user. SM_AURIX_DMA_5: Dedicated measures on system level are needed e.g. SDCRC, E2E for DMA transaction. SM_AURIX_IR_3: Removed in Safety manual V1.3 SM_AURIX_CAN_4: NA for MCAL as SRAM errors leads to SMU alarm; configuration of alarm reaction is responsibility of user SM_AURIX_ERAY_4: NA for MCAL as SRAM errors leads to SMU alarm; configuration of alarm reaction is responsibility of user SM_AURIX_GTM_1: NA for MCAL as SRAM errors leads to SMU alarm; configuration of alarm reaction is responsibility of user SM_AURIX_EXTVREG_TEST : NA for MCAL as it is Start-up test. SM_AURIX_SRAM_INIT: NA for MCAL software as it's a hardware safety mechanism. SM_AURIX_CPU_1:1, SM_AURIX_CPU_1:2, SM_AURIX_EVR_1:1, SM_AURIX_CCU_1:1, SM_AURIX_CPU_3:1, SM_AURIX_CPU_3:2, SM_AURIX_CPU_2:2, SM_AURIX_WDT_TEST, SM_AURIX_SPB_1:2, SM_AURIX_SMU_2:1, SM_AURIX_SMU_3:2, SM_AURIX_CPU_MPU_INIT_1, SM_AURIX_CPU_MPU_INIT_2, SM_AURIX_DMA_TEST_1, SM_AURIX_FCE_TEST_1, SM_AURIX_DMA_TEST_2, SM_AURIX_LMU_MPU_TEST_1, SM_AURIX_PSRAM_1:2: NA for MCAL as it is start-up self-tests. SM_AURIX_NLCPU_1: NA for MCAL as CPU Software Based Self-Test is not in the scope of MCAL SM_AURIX_IR_1: NA for MCAL as it's a hardware safety mechanism. SM_AURIX_WDT_1:1 NA for MCAL, it is part of WDG Manager.
SM_AURIX_07	NA for MCAL as this is a requirement on ECU design; responsibility of user
SM_AURIX_04	NA for MCAL as this is related to SMU
SM_AURIX_FFI_3	NA for MCAL software as it's a hardware safety mechanism.
0000047041-244] sections 4.23, 4.25, 4.26, 7	For each new requirement, the comments are given below.

Application Dependent Parts Redundant scenario described with more details for digital I/Os, ADC, and QSPI. Also aligned with DFA, and list of Dependent Failure Initiators completed and split into DFI applicable to basic device operation, DFI applicable to all redundant peripheral scenarios, DFI specific to each specific application usage scenario. new requirements:	
SM_AURIX_GTM_DFI_1	Not in the scope of MCAL, System integrator needs to take care.
SM_AURIX_GTM_DFI_2	Not in the scope of MCAL, System integrator needs to take care.
SM_AURIX_GTM_DFI_3	Not in the scope of MCAL, System integrator needs to take care.
SM_AURIX_GTM_DFI_4	Not in the scope of MCAL, System integrator needs to take care.
SM_AURIX_GTM_DFI_5	Not in the scope of MCAL, System integrator needs to take care.
SM_AURIX_GPI_DFI_1	Not in the scope of MCAL, System integrator needs to take care.
SM_AURIX_GPO_DFI_1	Not in the scope of MCAL, System integrator needs to take care.
SM_AURIX_QSPI_DFI_1	Not in the scope of MCAL, System integrator needs to take care.
removed requirements: SM_AURIX_DFA_1, SM_AURIX_DFA_2, SM_AURIX_DFA_3	NA for MCAL, as removal of requirements.
[0000047041-248] section 5.3.11 :added SM1[AoU].HSSL:SafeProtocol	NA for MCAL, HSSL driver is provided as demo driver from MCAL.
[0000047041-206] Sections 5.15.3, 5.3.13 added runtime test for LMU SRAM. SM1[AoU].LMU.DP:TEST	NA for MCAL as LMU SRAM run test is not part of MCAL.
[0000047041-245] Sections 5.3.5, 5.3.6 removed references to AURIX internal WDT. Goal is to leave the implementation of these safety mechanisms open.	NA for MCAL, deadline monitoring and program flow monitoring is part of WDG Manager. WDG driver only provides an interface to service the WDG.
[0000047041-275, 0000047041-278] Renamed section 3.4 into "Operating Modes" (was previously "Safe State Support"), extended the list of operating modes, modified wording of SM_AURIX_18	NA for MCAL. Maintaining normal run-time mode is responsibility of user
[0000047041-280] Section 5.3.4 :SM_AURIX_STM_3:1 Added additional hints to the description of SM1[AoU].STM: Plausibility.	NA for MCAL , OS / Application software to take care

[0000047041-209, 0000047041-214, 0000047041-238] Section 5.1.32: updated SM1 [HW].SMU: LOCK Error Signalling. Section 5.2.26: SM_AURIX_SMU_3:2 extended list of registers to be checked Section 5.2.27: fixed SM_AURIX_SMU_3:3 (no alarm or SPB error generated)	SM1[HW].SMU:LOCK : NA for MCAL software as it's a hardware safety mechanism SM_AURIX_SMU_3:2: NA for MCAL as its related to start-up test SM_AURIX_SMU_3:3 : NA for MCAL as its related to start-up test
[0000047041-253] add or removed information in following AoUs (does not change the meaning of the AoU): SM_AURIX_22, SM_AURIX_08, SM_AURIX_SPB_2:1	SM_AURIX_22 : NA for MCAL as it's a hardware safety mechanism SM_AURIX_08: Applicable, provided as part of Safety app note. SM_AURIX_SPB_2:1 : NA for MCAL as its related to start-up test
[0000047041-282] 5.11, 5.12, 5.13, 5.15 minor fixes in safety mechanisms description and error detection time.	NA for MCAL as it's a hardware safety mechanism
[0000047041-291] Section 5.11 :SM_AURIX_SRAM_INIT added clarification that this is only needed after a Cold PORST	NA for MCAL as it is related to start-up code.
[0000047041-241] 4.5 fixed wording of SM_AURIX_NLSCPU_4 5.3.2 improved SBST description.	NA for MCAL, only description is improved.
[0000047041-279, -217] Section 1.1, and 1.4 fixed description of the SEooC Section 3.1: improved parts categories description, added comments to the list of parts in table 3.	NA for MCAL, only description is improved.
[0000047041-219] Section 4.16 :removed EMEM from the list of peripheral SRAM instances Section 4.28 :add safety mechanisms for EMEM and limitations (notes)	NA for MCAL software as it's a hardware safety mechanism
[0000047041-221] Sections 5.1.22, 5.1.21 fixed SRI EDC description: behavior in case of failure during SRI transaction.	NA for MCAL as its related to start-up test
[0000047041-276] Section 5.2.9: simplified text of SM_AURIX_PMU_1:2, and added references Section 5.2.10 :simplified text of SM_AURIX_PMU_1:3, and added references Section 5.2.11: simplified text of SM_AURIX_PMU_1:5, and added references	NA for MCAL as its related to start-up test

[0000047041-252] Section 4.15: SM_AURIX_LMU_1 added SM1[HW].LMU:PD:EDC to the list Section 5.1.36 :modified field "error detection time" Section 5.1.52: created SM1[HW].LMU:PD:EDC	NA for MCAL software as it's a hardware safety mechanism
[0000047041-212] Section 5.1.29 :SM_AURIX_CPUCRC32_1 updated: Non-Lockstep CPU only	NA for MCAL software as it's a hardware safety mechanism
[0000047041-215] Section 5.3.12: in SM1[AoU].QSPI:SafeProtocol description, removed alternative using another QSPI module as slave to monitor some properties of the communication	Applicable. Assumption of Use shall be implemented in all safety related SPI communication which uses QSPI slave loop back mechanism
[0000047041-320] Section 5.1.1 :improved wording in field "product configuration" Section 5.1.34: improved wording in field "description" Section 5.1.37 :improved wording in fields "description" and "limitations and recommendations"	NA for MCAL, terminology improvement
[0000047041-311] Section 5.1.22: aligned alarms descriptions with user manual Section 5.2.14: added references to support the software implementation	NA for MCAL as it's a hardware safety mechanism or start-up test
[0000047041-309] Section 4.12.2 :SM_AURIX_SPB_1 added SM1[HW].SPB:EH to the list of hardware safety mechanisms for SPB Sections 4.24.2, 5.1.41 added SM1[HW].PSI5-S:AP Section 5.2.18: added SM2[AoU].PMU:AP and SM2[AoU].PSI5-S:AP	NA for MCAL as it's a hardware safety mechanism or start-up test
[0000047041-321] Section 5.1.46: Fixed error signalling description for Endinit protection (alarm) Section 5.2.26: added a recommendation to verify ARSTDIS and RSTCON by software after configuration	NA for MCAL as it's a hardware safety mechanism
[0000047041-325] Sections 4.28, 5.1.41, 5.2.18 removed all references to SM1[HW].CIF:AP Section 4.28: added a note in 4.28 that CIF has no ACCEN protection	NA for MCAL as it's a hardware safety mechanism
[0000047041-315]	NA for MCAL as it's a hardware safety mechanism or start-up

Sections 5.1.16, 5.1.17, 5.1.18, 5.1.19, Section 5.1.20 :fixed "error detection time" Section 5.20: fixed wording and added references to CBABSTAT and CBABCFG Section 5.2.9: SM_AURIX_PMU_1:2 added that SM2[AoU].PFLASH:ECC must also be tested	test
[0000047041-257] Section 3.8.2: SM_AURIX_5 change "pull device" into "pull-down device" Section 4.3 :SM_AURIX_SMU_5 clarified assumed configuration or error pin	Applicable, Configuration possibility provided from PORT driver.
[0000047041-277] General terminology improvement: Consolidated usage of "user" and "integrator". Both terms replaced by "system integrator". Consolidated usage of "user software" and "application software". "User software" replaced by "application software. Section 1.6.2 :added definition of "application software" Section 1.6.3 :added definition of "system level"	NA for MCAL, terminology improvement
[0000047041-299] Section 3.9.1: SM_AURIX_9 updated the hint for the implementation of this AoU (Note)	Not in the scope of MCAL as it is related to start-up sequence
[0000047041-307] Section 5.1.27: added limitations to the usage of SM1[HW].DMA:TIMESTAMP	NA for MCAL software as it's a hardware safety mechanism and MCAL doesn't use DMA timestamp feature.
[0000047041-217] Sections 1.1, 1.4 updated SEooC description Section 3.1: updated definition of part types and list of parts	NA for MCAL as only SEooC definition text is changed.
[0000047041-211] Section 5.1.4: SM_AURIX_EVR_3 added note that the AoU is only valid for TC27x, TC29x, and TC26x	NA for MCAL as EVR is not part of MCAL
[0000047041-340] Section 5.2.4 :added recommendations for testing the system PLL clock monitor	Not in the scope of MCAL as it is related to start-up test
[0000047041-347] Section 3.7: added figure 4 to illustrate startup phase Section 3.7.1: SM_AURIX_20 added reference to figure 4 Section 3.7.2: SM_AURIX_22 added reference to figure 4 Section 3.7.2 :added new AoU	NA for MCAL, Just info to user.

SM_AURIX_30 for startup check of all safety mechanisms configuration registers	
[0000047041-349] Section 4.1.1: Removed reference to safety analysis report. Section 5: removed reference to safety analysis report.	NA for MCAL, reference removal
[0000047041-350] Section 3.2: Updated Top Level Safety Requirements	See below comments Top Level Safety Requirement 4 and Top Level Safety Requirement 3.
Top Level Safety Requirement 4: Avoid undetected unavailability of a safety mechanism implemented by the microcontroller SEooC for longer than the multiple point fault detection interval in order to reach the target value for LFM.	NA for MCAL. SafeTlib or similar software to be used.
Top Level Safety Requirement 3: Provide information related to the avoidance of dependent failures to enable the monitoring of application dependent parts failure modes caused by random hardware faults by means of internal functional redundancies. At least the following redundancy use cases shall be considered: GTM TIM /CCU6 (or GPT12) GTM TIM/TIM, GTM TOM/TIM GTM TOM/CCU6/IOM GTM TOM/TOM/IOM GPI/GPI GPO/GPO QSPI/QSPI VADC/VADC DSADC/VADC	GTM TIM/TIM, GTM TOM/TOM/IOM, QSPI/QSPI not supported in the existing MCAL without additional safety measure. VADC/VADC : Limitation are mentioned in the Aurix_MC-ISAR_SoftwareSafetyInformation document. DSADC/VADC : Not in the scope of MCAL.

4.3 AURIX Safety Manual V1.4 changes w.r.t V1.3

Change Description from Safety manual V1.3to V1.4	Comments / Implementation hints from MCAL
[0000047041-363] Section 4.28.1: SM_AURIX_ADAS_2 New AoU specific to ADAS products	Safety applications should not use EMEM as several generic hardware safety mechanisms are not available.
[0000047041-365] Sections 4.26.4, 4.26.5 Fixed figures 14 and 15 as they were not representing the correct scenario (swapped the two	Does not impact MCAL. Only Documentation update.

figures)	
[0000047041-368] Section 5.1.40 :extended SM1[HW].LMU:AP safety mechanism description	NA for MCAL. Only Documentation update
[0000047041-354, 0000047041-358] Section 5.1.50 :fixed description of SM1[HW].Register:SFF, and added reference to SM1[HW].Register:FTSFF	NA for MCAL, it is related to hardware safety mechanism.
[0000047041-360] Section 5.2.27: changed hint that SMU need to be in START state for this test, actually it must be in RUN state	NA for MCAL.
[0000047041-348] Section 8 :SM_AURIX_31 New AoU specific to bare die products	NA for MCAL, more of hardware design consideration for system integrators.

4.4 AURIX Safety Manual V1.5.1 changes w.r.t V1.4

Change Description from Safety manual V1.5.1 to V1.4	Comments / Implementation hints from MCAL
[0000047041-422] Section 5.3.10: Added cross-references	Only cross-reference addition
[0000047041-421] Section 4.25.1: Added note for usage of TC23x ADAS ADCs in redundant VADC VADC scenario	Redundant Acquisition Using two VADC Groups not impacting MCAL
[0000047041-419] Section 3.8.2: Changed cross-reference from 4.2.5 to 4.3	Only cross-reference addition
[0000047041-417] Section 7.3: Added attention section to mention missing dependent failure initiator in VADC-VADC Application Dependant Scenario	Not impacting MCAL. Note to integerator.
[0000047041-416] Section 3.1: Added ERU to list of non-safety related parts	Not safety related. Documentation/information update.
[0000047041-414] Section 4.5.1: Updated 1st and 2nd attention section. Scope of SBST on CPU core refined according to SBST Safety Analysis	Note to integerator. Not impacting MCAL
[0000047041-404] Section 5.2.26: Typo in SMU Alarm configuration register names	Typo correction. Already analyzed as part of STL. Reanalysis is not done.
[0000047041-402] Section 4.15.2, 5.2.41: New AoU SM_AURIX_LMU_SRAM_2	Not impacting MCAL. Note to integerator.
[0000047041-401]	Note to integerator. Not impacting MCAL

Section 4.7.2: Added reference to AP32329 AURIX™ Secondary Voltage Monitors - Setting threshold levels	
[0000047041-400] Section 3.1: Added SPB to SRI Bridge and IR to list of critical parts	General information. Not impacting MCAL.
[0000047041-399] Section 1.4: Replaced the term "single channel software applications" by "non-Lockstep CPU"	Documentation
[0000047041-398] Section 5.2.34: Added WDTxCON0.PW, WDTxCON1.PAR and WDTxCON1.TCR to list of register to check	WDT is a QM module and Initcheck is not part of the driver scope.
[0000047041-395] Section 5.2.31, 5.2.32, 5.2.33: Extended description of CPU MPU, BUS MPU and LMU MPU safety mechanisms	Description improvement "The safety mechanism shall consist of reading the relevant configuration registers and comparing the read value to the expected value". Not impacting MCAL
[0000047041-392] Section 5.2.3: Removed reference to SM2[HW].BANDGAP:HWBIST. This safety mechanism is obsolete	Obsolete SM
[0000047041-390] Section 5.3.13: Added SENT, ASCLIN and PSI5 SafeProtocol safety mechanisms	Not impacting MCAL. E-to-E requirements included in Safety case.
[0000047041-389] Section 5.1.27: Modified limitation on timestamp usage with circular buffer with regards to erratum DMA_TC.034	Timestamp feature isn't supported by the driver. Refer All devices MC-ISAR_HWErrataAnalysis.xls.
[0000047041-388] Section 5.1.31: Added limitation to usage of DMA Address CRC safety mechanism	Not impacting MCAL. Limitation already taken into consideration and documented in the UM.
[0000047041-383, 0000047041-384] Section 1.1, 1.6.1: Added notes to introduce requirement tags and differentiate them from safety mechanism tags	Documentation improvement
[0000047041-381, 0000047041-413] Section 4.25.1: Updated figure 9 and 10 and added table 7 and 9 to support BGA416 package	Redundant Acquisition Using two VADC Groups not impacting MCAL
[0000047041-379] Section 4.15: Added TC23x ADAS in the list of devices implementing the LMU SRAM	Documentation update. Not impacting MCAL.
[0000047041-377] Section 5.3.10: SM_AURIX_DMA_3:1 completely reworked the description of	Documentation update, enhancement in representation alone. Not impacting MCAL.

SM1[AoU].DMA:Monitor with a better identification of the failure modes to be covered by software and additional implementation hints	
[0000047041-376] Section 4.16: Removed FSI0 from table 5. FSI0 RAM is neither accessible nor testable. Typo corrected: GTM MSC0/1 replaced by GTM MCS0/1	General information. Not impacting MCAL.
0000047041-443], [0000047041-444] Section 5.1.27: Added limitation on DMA timestamp usage with regards to erratum DMA_TC.063, and usage with circular buffer with regards to erratum DMA_TC.034	Timestamp feature isn't supported by the driver. Refer All devices MC-ISAR_HWErrataAnalysis.xls.
[0000047041-442] Section 5.1.30: Added limitation in the usage of DMA Data CRC.	Not impacting MCAL. Limitation already taken care in module implementation.
[0000047041-438] Section 5.2.41: Description of SM_AURIX_LMU_SRAM_2 updated and relocated in sub-chapter 5.2	Not impacting MCAL. Note to integerator.
[0000047041-435] Section 1.1: Typo in requirement tag. SM_AURIX_25 corrected into SM_AURIX_24	Requirement tag correction. Documentation
[0000047041-434], [0000047041-439] Section 5.1.12, 5.1.15: Extended error signalling section of SRAM Address Monitor and SRAM Error Tracking safety mechanisms	Not impacting MCAL. Note to integerator.
[0000047041-431], [0000047041-432], [0000047041-433] Section 3.4, 4.3.1: Fragmented tagging issue solved	Documentation
[0000047041-422] Section 5.3.10: Added cross-references	Only cross-reference addition
[0000047041-421] Section 4.25.1: Added note for usage of TC23x ADAS ADCs in redundant VADC VADC scenario	Redundant Acquisition Using two VADC Groups not impacting MCAL

5 New AoU's additional to Aurix_MC-ISAR_SoftwareSafetyInformation V3.0

Module	AoU

General	The integrator shall protect the Stack memory from the corruption using MPU protection to avoid corruption of stack memory leading to wrong behavior.
General	If Flash, SRAM ECC alarm (uncorrectable), is triggered application shall not rely on any MCAL data (for example, ADC conversion result). Refer SM_AURIX_CPU_3 and SM_AURIX_PMU_1 in HW Safety Manual for more information.
General	Integrator shall ensure that the valid pointer is passed to <Mod>_GetVersionInfoApi() to avoid memory corruption, if wrong pointer is passed. Valid pointer means: no NULLPTR and a writeable location with appropriate access rights for the caller
General	The integrator shall not call <Mod>_Init() and <Mod>_DeInit() APIs from QM partition for drivers targeted to be used with ASIL claim.
General	It is assumed that the integrated system shall support to have mixed ASIL software with software modules (below RTE) and SW-Cs (above RTE)
General	It is assumed that the invoked OS calls are developed by integrator according to ISO26262 based on the ASIL level of the intended application
MCU	The integrator shall not call the following APIs from QM partition, if MCU driver is targeted to be used with ASIL claim. a. Mcu_InitClock() b. Mcu_DistributePllClock() c. Mcu_RampToBackUpClockFreq() d. Mcu_17_CcuconRegUpdate() e. Mcu_SetMode() f. Mcu_SetStandbyCtrlReg()
MCU	The integrator shall provide access to Mcu_Init() API for all the resources used by GTM complex driver, if used in the system for the GTM complex driver initialization including the required SFRs.
MCU	The integrator shall ensure that GTM ISRs for TOM and ATOM are called with correct module and channel numbers.
PWM	The integrator shall verify the correctness of initialization done by the Pwm_17_Gtm_Init() API, after initialization of all modules to ensure no corruption of variables and SFR. Alternatively, verify the generated PWM signals using redundancy (for example, feedback or loopback mechanisms using ICU driver) to detect the errors in the generated PWM signal.
ICU	The integrator shall not call Icu_17_GtmCcu6_SetMode() API from QM partition, if ICU driver is targeted to be used with ASIL claim.

ICU	The integrator shall not use the Wakeup functionality in QM partition, if ICU driver targeted to be used with ASIL claim.
GPT	The integrator shall not call Gpt_SetMode() API from QM partition, if GPT driver is targeted to be used with ASIL claim.
ADC	The integrator shall ensure that buffer provided is properly aligned (16bit memory alignment required, in case 10bit or 12bit resolution is used for any channel).
ADC	The integrator shall read the data only after confirming the channel specific conversion is completed in polling mode using Adc_17_GetChannelStatus() API.
ADC	The integrator shall configure the different pairs of ERU units to ASIL and QM ADC hardware groups. For example, ERU0 and ERU1 can be assigned to ASIL ADC hardware groups, ERU2 and ERU3 can be assigned to QM ADC hardware groups.
ADC	The integrator shall limit one TOM/ATOM module to one driver, for instance TOM0 shall be allocated to ADC and TOM1 shall be allocated to GPT/PWM.
SPI	The integrator shall not call the following APIs from QM partition, if SPI driver is targeted to be used with ASIL claim. a. Spi_SetAsyncMode() b. Spi_AsyncTransmit() c. Spi_SyncTransmit() d. Spi_WriteIB() e. Spi_SetupEB() f. Spi_IsrQspiError() g. Spi_IsrQspiPt() h. Spi_IsrDMAQspiRx() i. Spi_IsrDmaError() j. Spi_IsrDmaQspiTxRuntime() k. Spi_IsrQspiUsr()
PORT	The integrator shall not call the Port_RefreshPortDirection() API from QM partition, if PORT driver is targeted to be used with ASIL claim.
PORT	The integrator shall call Port_SetPinDirection() and Port_SetPinMode() APIs from QM and ASIL partition, only for the pins of a different port.
DIO	The integrator shall call Dio_WriteChannelGroup() API from QM and ASIL partition, only for the channel groups of a different port.
MCALLIB	The integrator shall ensure that the APIs Mcal_SafetyModifyAccess() and Mcal_SafetyCheckAccess() are not

	1. Called concurrently from other cores 2. Called when Mcal_ResetSafetyENDINIT_Timed()/Mcal_SetSafetyENDINIT_Timed() are being executed or vice versa
MCALLIB	The integrator shall ensure that the valid values are passed to all MCALLIB APIs as per the input parameter range, if these functions are called directly in applications.
MCALLIB	The integrator shall ensure that the APIs Mcal_SafetyModifyAccess() and Mcal_SafetyCheckAccess() are not 1. Called concurrently from other cores 2. Called when Mcal_ResetSafetyENDINIT_Timed()/Mcal_SetSafetyENDINIT_Timed() are being executed or vice versa

Revision History

Date	Version	Description of change
2022-02-09	V26.0	Release notes addendum 2022-02 – (Issue confirmed till 07-Feb-2022) – Added REL425 release information
2021-08-05	V25.0	Release notes addendum 2021-08 – (Issue confirmed till 23-Jul-2021) – Added REL420.1 release information. – Added section 4.4 AURIX Safety manual V1.5.1 changes w.r.t V1.4 – Added new AoU's in section 5
2021-03-03	V24.0	Release notes addendum 2021-02 (Issue confirmed till 18-Feb-2021 are considered)
2020-11-18	V23.0	Release notes addendum 2020-11 (Issue confirmed till 17-Nov-2020 are considered) – Added REL415 release information. – Following new Errata sheets are verified : TC29x_BB_Errata_Sheet_v1_8_10217AERRA.pdf TC29x_BC_Errata_Sheet_v1_4_10218AERRA.pdf TC27x_DC_Errata_Sheet_v1_4_10216AERRA.pdf TC27x_DB_Errata_Sheet_v1_8_10215AERRA.pdf TC27x_CA_Errata_Sheet_v1_9_10214AERRA.pdf TC26x_BB_Errata_Sheet_v1_7_10211AERRA.pdf TC26x_BC_Errata_Sheet_v1_4_10212AERRA.pdf TC23x_AC_Errata_Sheet_v1_5_10210AERRA.pdf TC23x_AB_Errata_Sheet_v1_8_10209AERRA.pdf TC22x_TC21x_AB_Errata_Sheet_v1_7_10207AERRA.pdf TC22x_TC21x_AC_Errata_Sheet_v1_4_10208AERRA.pdf
2020-06-12	V22.0	Release notes addendum 2020-06 (Issue confirmed till 01-June-2020 are considered)
2020-04-29	V21.1	FEE specific Releasenotes Addendum. (Issue confirmed till 21-Jan-2020 are considered) – Added following new FEE issues. 1) 0000051018-3127 2) 0000051018-3128 – Added REL410 release applicability to the above JIRAs only. **Note:** Complete list of open issues for REL410 will be published in next Releasenotes Addendum.
2020-02-03	V21.0	Release notes addendum 2020-01 (Issue confirmed till 21-Jan-2020 are considered)
2019-10-23	V20.1	Release notes addendum 2019-10 (Issue confirmed till 02-Sep-2019 are considered) – Following new Errata sheets are verified : TC26x_BB_Errata_Sheet_v1_6_022_19.pdf

Date	Version	Description of change
		TC26x_BC_Errata_Sheet_v1_3_024_19.pdf
2019-09-20	V20.0	Release notes addendum 2019-09 (Issue confirmed till 02-Sep-2019 are considered) – Added REL405 release information. – Following new Errata sheets are verified : TC29x_BB_Errata_Sheet_v1_7_029_190.pdf TC29x_BC_Errata_Sheet_v1_3_030_190.pdf TC27x_DC_Errata_Sheet_v1_3_028_190.pdf TC27x_DB_Errata_Sheet_v1_7_027_190.pdf TC27x_CA_Errata_Sheet_v1_8_026_190.pdf TC23x_AC_Errata_Sheet_v1_4_097_19.pdf TC23x_AB_Errata_Sheet_v1_7_096_19.pdf TC22x_TC21x_AB_Errata_Sheet_v1_6_094_19.pdf TC22x_TC21x_AC_Errata_Sheet_v1_3_095_19.pdf
2019-05-10	V19.0	Release notes addendum 2019-05 (Issue confirmed till 02-May-2019 are considered)
2019-02-12	V18.0	Release notes addendum 2019-02 (Issue confirmed till 30-Jan-2019 are considered) – Added TC26xBB and TC26xBC REL400 release information. – Updated Scope of Release Notes Addendum section for missing release i.e. TC26xBB Rel-304.
2018-10-23	V17.0	Release notes addendum 2018-10 (Issue confirmed till 12-Oct-2018 are considered) – Added REL374, REL372, REL380 and REL376 release information. - Updated release note addendum for REL-180, REL-185, REL-250 and for REL-270. – Following new Errata sheets are verified : TC29x_BB_Errata_Sheet_v1_6_162_17.pdf TC29x_BC_Errata_Sheet_v1_2_163_17.pdf TC26x_BB_Errata_Sheet_v1_5_164_17.pdf TC26x_BC_Errata_Sheet_v1_2_165_17.pdf TC23x_AC_Errata_Sheet_v1_3_063_18.pdf TC23x_AB_Errata_Sheet_v1_6_062_18.pdf TC22x_TC21x_AB_Errata_Sheet_v1_5_064_18.pdf TC22x_TC21x_AC_Errata_Sheet_v1_2_065_18.pdf
2018-05-28	V16.0	Updated release note addendum for REL170
2018-05-08	V15.0	Release notes addendum 2018-04 (Issues reported till 24-April-2018 are considered) – Added REL170, REL192, REL198, REL368, REL370 and REL378 release information. – Following new Errata sheets are verified : TC27x_DC_Errata_Sheet_v1_2_184_17.pdf TC27x_DB_Errata_Sheet_v1_6_183_17.pdf TC27x_CA_Errata_Sheet_v1_7_182_17.pdf
2018-01-12	V14.0	Release notes addendum 2018-01

Date	Version	Description of change
		(Issues reported till 15-Dec-2017 are considered) – Editorial changes (Feature re-ordering of the issues) – New issues are added under section 1.1 – New issues details are added under section 2.1 – Following new Errata sheets are verified : TC26x_BB_Errata_Sheet_v1_4_098_17.pdf TC26x_BC_Errata_Sheet_v1_1_099_17.pdf
2017-08-10	V13.0	Release notes addendum 2017-07 (Issues reported till 15-July-2017 are considered) Note added in cover sheet with respect to ASIL B claim. Section 1 updated. New issues are added under section 1.1. Section 2 updated. New issues details are added under section 2.1. New Errata sheets verified : TC29x_BB_Errata_Sheet_v1_5_054_17.pdf TC29x_BC_Errata_Sheet_v1_1_055_17.pdf TC27x_CA_Errata_Sheet_v1_6_029_17.pdf TC26x_BC_Errata_Sheet_v1_0.pdf TC23x_AB_Errata_Sheet_v1_4_052_17.pdf TC22x_TC21x_AB_Errata_Sheet_v1_3_070_17.pdf TC22x_TC21x_AC_Errata_Sheet_v1_0_071_17.pdf
2017-07-18	V12.2	Reformulation of workaround for 0000051018-683 JIRA.
2017-07-06	V12.1	Updated workaround and description for 0000051018-683 JIRA.
2017-06-06	V12.0	Release notes addendum 2017-05 (Issues reported till 16-May-2017 are considered) Section 1 updated New issues are added under section 1.1 Section 2 updated New issues details are added under section 2.1 Section 3.1 updated with device details of 23x AC, 26x BC, 27x DC New Errata sheet verified : TC23x_AC_Errata_Sheet_v1_1_053_17.pdf New Release information added for : Rel314, Rel326, Rel318, Rel320, Rel322, Rel323, Rel328, Rel330, Rel334
2017-02-24	V11.0	Release notes addendum 2017-01 (Issues till 02-Feb-2017 are considered) – Editorial changes (Feature re-ordering of the issues) – New issues are added under section 1.1 New issues details are added under section 2.1 Added Chapter 6 “New AoU’s additional to Aurix_MC-ISAR_SoftwareSafetyInformation V3.0” Added the following new releases – MR - TC297_BB (Rel306/V2.0.0) – MR - TC297_BB (Rel327/V2.1.0) MR - TC297TX_BC (Rel329/V3.0.0)
2016-12-15	V10.0	Release notes addendum 2016-12

Revision History

Date	Version	Description of change
		(Issues till 29-Nov-2016 are considered) – Editorial changes (Feature re-ordering of the issues) – New issues are added under section 1.1 New issues details are added under section 2.1
2016-09-30	V9.0	Release notes addendum 2016-09 (Issues till 22-Sept-2016 are considered) – Editorial changes (Feature re-ordering of the issues) – New issues are added under section 1.1 New issues details are added under section 2.1
2016-06-14	V8.0	Release notes addendum 2016-06 (Issues till 31-May-2016 are considered) – Editorial changes (Feature re-ordering of the issues) – New issues are added under section 1.1 New issues details are added under section 2.1
2016-05-03	V7.0	Release notes addendum 2016-05 (Issues till 25-April-2016 are considered) – Editorial changes (Feature re-ordering of the issues) – New issues are added under section 1.1 Rolling forecast column is added in section 2 and section 2.1
2016-03-18	V6.0	Release notes addendum 2016-03 (Issues till 15-Mar-2016 are considered) – Editorial changes (Feature re-ordering of the issues) – New issues are added in Section 1.1 – HW Errata's which have been analysed are added in Front page – Added back following previous PR releases PR - TC26xBB (Rel180/V2.0.0) PR - TC29xBB (Rel180/V2.1.0)) – Added following new releases MR - TC27xCA (Rel300/V4.00) MR - TC27xDB (Rel302/V3.0.0)
2016-02-03	V5.1	New issue about release Notes not properly conveying the information that "Released Items" are productive code is added in Section 3.3 and details available in Section 4
2016-01-05	V5.0	Release notes addendum 2016-01 (Issues till 04-Jan-2016 are considered) – Removed following releases PR - TC26xBB (Rel180/V2.0.0) PR - TC29xBB (Rel180/V2.1.0) – Added following releases MR - TC26xBB (Rel194/V3.00) MR - TC29xBB (Rel196/V3.0.0) – Streamlined Issues applicable to all releases in Section 3.1. – Added new issues for releases based on its applicability in Section 3.2.

Revision History

Date	Version	Description of change
		– Added details of Issues in Section 4. Added Section 7.3 . AURIX Safety Manual V1.4 changes w.r.t V1.3
2015-11-06	V4.0	Release notes addendum 2015-11 – Addendum for the given Releases – TC27X_CA : V300 – TC27X_DB : V200 – TC29X_BB : V210 – TC26X_BB : V200 – TC23X_AB : V300 – TC22X_AB : V200 – TC21X_AB : V200 Added Section 5. AoU's of Aurix Hardware Safety Manual V1.2 and V1.3
2015-09-03	V3.0	Release notes addendum 2015-09 – Addendum for the given Releases – TC27X_CA : V300 – TC27X_DB : V100 – TC29X_BB : V210 – TC26X_BB : V200 – TC23X_AB : V300 – TC22X_AB : V200 – TC21X_AB : V200 Added Section 4. Safety mechanism to be considered.
2015-06-15	V2.0	Release notes addendum 2015-06 – Addendum for the given Releases – TC27X_CA : V300 – TC29X_BB : V210 – TC26X_BB : V200 Added Section 3. Supported Derivative and Derivative Restriction Info
2015-02-27	V1.0	Release notes addendum 2015-02 – Addendum for the given Releases – TC27X_BC : V240 – TC27X_CA : V200 – TC29X_BB : V100 – TC26X_BB : V100 TC23X_AB : V200

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MC-ISAR AURIX Release Notes Addendum V26.0 affecting dedicated products

Sales name	SP number	OPN	Package
SAK-TC233L-32F200F AB	SP001268346	TC233L32F200FABKXUMA1	PG-TQFP-100-23
SAK-TC233L-32F200F AB	SP004396818	TC233L32F200FABKXUMA2	PG-TQFP-100-23
SAK-TC233L-32F200F AC	SP001674224	TC233L32F200FACKXUMA1	PG-TQFP-100-23
SAK-TC233L-32F200F AC	SP001700652	TC233L32F200FACKXQMA1	PG-TQFP-100-23
SAK-TC233L-32F200N AC	SP001408138	TC233L32F200NACKXUMA1	PG-TQFP-100-23
SAK-TC233LC-24F133F AB	SP001270740	TC233LC24F133FABKXUMA1	PG-TQFP-100-23
SAK-TC233LC-24F133F AC	SP001584028	TC233LC24F133FACKXUMA1	PG-TQFP-100-23
SAK-TC233LC-24F133N AC	SP002725546	TC233LC24F133NACKXUMA1	PG-TQFP-100-23
SAK-TC233LP-16F200F AB	SP001270730	TC233LP16F200FABKXUMA1	PG-TQFP-100-23
SAK-TC233LP-16F200F AC	SP001682994	TC233LP16F200FACKXUMA1	PG-TQFP-100-23
SAK-TC233LP-16F200N AC	SP001627900	TC233LP16F200NACKXUMA1	PG-TQFP-100-23
SAK-TC233LP-24F200N AC	SP002944554	TC233LP24F200NACKXUMA1	PG-TQFP-100-23
SAK-TC233LP-32F200F AB	SP001268348	TC233LP32F200FABKXUMA1	PG-TQFP-100-23
SAK-TC233LP-32F200F AC	SP001399222	TC233LP32F200FACKXUMA1	PG-TQFP-100-23
SAK-TC233LP-32F200F AC	SP001692512	TC233LP32F200FACKXQMA1	PG-TQFP-100-23
SAK-TC233LP-32F200N AC	SP001397720	TC233LP32F200NACKXUMA1	PG-TQFP-100-23
SAK-TC233LP-32F200N AC	SP001641894	TC233LP32F200NACKXQMA1	PG-TQFP-100-23
SAK-TC233S-32F200N AC	SP001658270	TC233S32F200NACKXUMA1	PG-TQFP-100-23
SAK-TC233S-32F200N AC	SP001720744	TC233S32F200NACKXQMA1	PG-TQFP-100-23
SAK-TC233SP-32F200N AC	SP001689232	TC233SP32F200NACKXUMA1	PG-TQFP-100-23
SAK-TC233SP-32F200N AC	SP001708334	TC233SP32F200NACKXQMA1	PG-TQFP-100-23
SAK-TC234L-24F200F AC	SP001658274	TC234L24F200FACKXUMA1	PG-TQFP-144-27
SAK-TC234L-24F200N AC	SP001624402	TC234L24F200NACKXUMA1	PG-TQFP-144-27
SAK-TC234L-32F200F AB	SP001268350	TC234L32F200FABKXUMA1	PG-TQFP-144-27
SAK-TC234L-32F200F AC	SP001658280	TC234L32F200FACKXUMA1	PG-TQFP-144-27
SAK-TC234L-32F200N AC	SP001408144	TC234L32F200NACKXUMA1	PG-TQFP-144-27
SAK-TC234LA-32F200F AB	SP001276932	TC234LA32F200FABKXUMA1	PG-TQFP-144-27
SAK-TC234LC-24F133F AC	SP001584026	TC234LC24F133FACKXUMA1	PG-TQFP-144-27
SAK-TC234LH-32F200F AB	SP005184614	TC234LH32F200FABKXUMA1	PG-TQFP-144-27
SAK-TC234LP-24F200F AC	SP001658278	TC234LP24F200FACKXUMA1	PG-TQFP-144-27
SAK-TC234LP-32F200F AB	SP001268352	TC234LP32F200FABKXUMA1	PG-TQFP-144-27
SAK-TC234LP-32F200F AC	SP001399224	TC234LP32F200FACKXUMA1	PG-TQFP-144-27
SAK-TC234LP-32F200F AC	SP002574662	TC234LP32F200FACKXQMA1	PG-TQFP-144-27
SAK-TC234LP-32F200N AC	SP001397714	TC234LP32F200NACKXUMA1	PG-TQFP-144-27
SAK-TC234LP-32F200N AC	SP001642890	TC234LP32F200NACKXQMA1	PG-TQFP-144-27
SAK-TC234LX-32F200F AB	SP001350934	TC234LX32F200FABKXUMA1	PG-TQFP-144-27
SAK-TC234LX-32F200F AB	SP001689442	TC234LX32F200FABKXQMA1	PG-TQFP-144-27
SAK-TC237L-32F200S AB	SP001268354	TC237L32F200SABKXUMA1	PG-LFBGA-292-6
SAK-TC237L-32F200S AC	SP001658282	TC237L32F200SACKXUMA1	PG-LFBGA-292-6
SAK-TC237LP-32F200N AC	SP001397698	TC237LP32F200NACKXUMA1	PG-LFBGA-292-6

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Sales name	SP number	OPN	Package
SAK-TC237LP-32F200S AB	SP001268356	TC237LP32F200SABKXUMA1	PG-LFBGA-292-6
SAK-TC237LP-32F200S AC	SP001399220	TC237LP32F200SACKXUMA1	PG-LFBGA-292-6
SAK-TC264D-40F200N BC	SP001676268	TC264D40F200NBCKXUMA2	PG-LQFP-144-22
SAK-TC264D-40F200W BB	SP001257822	TC264D40F200WBBKXUMA1	PG-LQFP-144-22
SAK-TC264D-40F200W BC	SP001399214	TC264D40F200WBCKXUMA1	PG-LQFP-144-22
SAK-TC264DA-40F200N BC	SP001676270	TC264DA40F200NBCKXUMA2	PG-LQFP-144-22
SAK-TC264DA-40F200N BC	SP004374874	TC264DA40F200NBCKXUMA3	PG-LQFP-144-22
SAK-TC264DA-40F200W BB	SP001257824	TC264DA40F200WBBKXUMA1	PG-LQFP-144-22
SAK-TC264DA-40F200W BB	SP005562408	TC264DA40F200WBBKXUMA3	PG-LQFP-144-22
SAK-TC264DA-40F200W BC	SP001399218	TC264DA40F200WBCKXUMA1	PG-LQFP-144-22
SAK-TC264DC-40F200W BB	SP001399740	TC264DC40F200WBBKXUMA1	PG-LQFP-144-22
SAK-TC264DC-40F200W BC	SP001611462	TC264DC40F200WBCKXUMA1	PG-LQFP-144-22
SAK-TC265D-40F200N BC	SP001397662	TC265D40F200NBCKXUMA1	PG-LQFP-176-22
SAK-TC265D-40F200W BB	SP001257830	TC265D40F200WBBKXUMA1	PG-LQFP-176-22
SAK-TC265D-40F200W BB	SP005337974	TC265D40F200WBBKXUMA2	PG-LQFP-176-22
SAK-TC265D-40F200W BC	SP001399216	TC265D40F200WBCKXUMA1	PG-LQFP-176-22
SAK-TC265DC-40F200W BB	SP001363114	TC265DC40F200WBBKXUMA1	PG-LQFP-176-22
SAK-TC265DC-40F200W BC	SP001611464	TC265DC40F200WBCKXUMA1	PG-LQFP-176-22
SAK-TC267D-40F200N BC	SP001592934	TC267D40F200NBCKXUMA1	PG-LFBGA-292-6
SAK-TC267D-40F200S BB	SP001270092	TC267D40F200SBBKXUMA1	PG-LFBGA-292-6
SAK-TC267D-40F200S BC	SP001662612	TC267D40F200SBCKXUMA1	PG-LFBGA-292-6
SAK-TC275T-64F200N DC	SP001651570	TC275T64F200NDCKXUMA1	PG-LQFP-176-22
SAK-TC275T-64F200W CA	SP001106358	TC275T64F200WCAKXUMA1	PG-LQFP-176-22
SAK-TC275T-64F200W DB	SP001217592	TC275T64F200WDBKXUMA1	PG-LQFP-176-22
SAK-TC275T-64F200W DC	SP001662592	TC275T64F200WDCKXUMA1	PG-LQFP-176-22
SAK-TC275TC-64F200N DC	SP001667658	TC275TC64F200NDCKXUMA1	PG-LQFP-176-22
SAK-TC275TC-64F200W CA	SP001217626	TC275TC64F200WCAKXUMA1	PG-LQFP-176-22
SAK-TC275TC-64F200W DB	SP001217602	TC275TC64F200WDBKXUMA1	PG-LQFP-176-22
SAK-TC275TC-64F200W DC	SP001611466	TC275TC64F200WDCKXUMA1	PG-LQFP-176-22
SAK-TC275TP-64F200N DC	SP001397622	TC275TP64F200NDCKXUMA1	PG-LQFP-176-22
SAK-TC275TP-64F200N DC	SP001630432	TC275TP64F200NDCKXQMA1	PG-LQFP-176-22
SAK-TC275TP-64F200W CA	SP001105592	TC275TP64F200WCAKXUMA1	PG-LQFP-176-22
SAK-TC275TP-64F200W CA	SP001332056	TC275TP64F200WCAKXQMA1	PG-LQFP-176-22
SAK-TC275TP-64F200W DB	SP001217586	TC275TP64F200WDBKXUMA1	PG-LQFP-176-22
SAK-TC275TP-64F200W DC	SP001366138	TC275TP64F200WDCKXUMA1	PG-LQFP-176-22
SAK-TC277T-64F200N DC	SP001665660	TC277T64F200NDCKXUMA1	PG-LFBGA-292-6
SAK-TC277T-64F200N DC	SP005337796	TC277T64F200NDCKXUMA2	PG-LFBGA-292-10
SAK-TC277T-64F200S CA	SP001146094	TC277T64F200SCAKXUMA1	PG-LFBGA-292-6
SAK-TC277T-64F200S CA	SP005337784	TC277T64F200SCAKXUMA2	PG-LFBGA-292-10
SAK-TC277T-64F200S DB	SP001217632	TC277T64F200SDBKXUMA1	PG-LFBGA-292-6

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Sales name	SP number	OPN	Package
SAK-TC277T-64F200S DB	SP005337792	TC277T64F200SDBKXUMA2	PG-LFBGA-292-10
SAK-TC277T-64F200S DC	SP001662590	TC277T64F200SDCKXUMA1	PG-LFBGA-292-6
SAK-TC277T-64F200S DC	SP005337794	TC277T64F200SDCKXUMA2	PG-LFBGA-292-10
SAK-TC277TC-64F200N DC	SP001667664	TC277TC64F200NDCKXUMA1	PG-LFBGA-292-6
SAK-TC277TC-64F200N DC	SP005345020	TC277TC64F200NDCKXUMA2	PG-LFBGA-292-10
SAK-TC277TC-64F200S CA	SP001217636	TC277TC64F200SCAKXUMA1	PG-LFBGA-292-6
SAK-TC277TC-64F200S CA	SP005337788	TC277TC64F200SCAKXUMA2	PG-LFBGA-292-10
SAK-TC277TC-64F200S DB	SP001217638	TC277TC64F200SDBKXUMA1	PG-LFBGA-292-6
SAK-TC277TC-64F200S DB	SP005337798	TC277TC64F200SDBKXUMA2	PG-LFBGA-292-10
SAK-TC277TC-64F200S DC	SP001611468	TC277TC64F200SDCKXUMA1	PG-LFBGA-292-6
SAK-TC277TC-64F200S DC	SP005337800	TC277TC64F200SDCKXUMA3	PG-LFBGA-292-10
SAK-TC277TC-64F200S DC	SP005345022	TC277TC64F200SDCKXUMA2	PG-LFBGA-292-10
SAK-TC277TP-64F200N DC	SP001397616	TC277TP64F200NDCKXUMA1	PG-LFBGA-292-6
SAK-TC277TP-64F200N DC	SP003475204	TC277TP64F200NDCKXQMA1	PG-LFBGA-292-6
SAK-TC277TP-64F200N DC	SP005337810	TC277TP64F200NDCKXUMA3	PG-LFBGA-292-10
SAK-TC277TP-64F200N DC	SP005345024	TC277TP64F200NDCKXUMA2	PG-LFBGA-292-10
SAK-TC277TP-64F200S CA	SP001146098	TC277TP64F200SCAKXUMA1	PG-LFBGA-292-6
SAK-TC277TP-64F200S CA	SP005337786	TC277TP64F200SCAKXUMA2	PG-LFBGA-292-10
SAK-TC277TP-64F200S DB	SP001217634	TC277TP64F200SDBKXUMA1	PG-LFBGA-292-6
SAK-TC277TP-64F200S DB	SP005337806	TC277TP64F200SDBKXUMA2	PG-LFBGA-292-10
SAK-TC277TP-64F200S DC	SP001366136	TC277TP64F200SDCKXUMA1	PG-LFBGA-292-6
SAK-TC277TP-64F200S DC	SP005337808	TC277TP64F200SDCKXUMA3	PG-LFBGA-292-10
SAK-TC277TP-64F200S DC	SP005345026	TC277TP64F200SDCKXUMA2	PG-LFBGA-292-10
SAK-TC297T-96F300N BC	SP001684616	TC297T96F300NBCKXUMA1	PG-LFBGA-292-6
SAK-TC297T-96F300N BC	SP005411081	TC297T96F300NBCKXUMA2	PG-LFBGA-292-10
SAK-TC297T-96F300S BB	SP001265616	TC297T96F300SBBKXUMA1	PG-LFBGA-292-6
SAK-TC297TA-128F300N BC	SP001397668	TC297TA128F300NBCKXUMA1	PG-LFBGA-292-6
SAK-TC297TA-128F300N BC	SP005337844	TC297TA128F300NBCKXUMA2	PG-LFBGA-292-10
SAK-TC297TA-128F300S BB	SP001130460	TC297TA128F300SBBKXUMA1	PG-LFBGA-292-6
SAK-TC297TA-128F300S BB	SP005337840	TC297TA128F300SBBKXUMA2	PG-LFBGA-292-10
SAK-TC297TA-128F300S BC	SP001662208	TC297TA128F300SBCKXUMA1	PG-LFBGA-292-6
SAK-TC297TA-128F300S BC	SP005337846	TC297TA128F300SBCKXUMA2	PG-LFBGA-292-10
SAK-TC297TA-64F300S BB	SP001265584	TC297TA64F300SBBKXUMA1	PG-LFBGA-292-6
SAK-TC297TA-64F300S BC	SP001662210	TC297TA64F300SBCKXUMA1	PG-LFBGA-292-6
SAK-TC297TC-96F300S BB	SP001265598	TC297TC96F300SBBKXUMA1	PG-LFBGA-292-6
SAK-TC297TC-96F300S BB	SP005411079	TC297TC96F300SBBKXUMA2	PG-LFBGA-292-10
SAK-TC297TC-96F300S BC	SP005411082	TC297TC96F300SBCKXUMA2	PG-LFBGA-292-10
SAK-TC297TP-128F300N BC	SP001396392	TC297TP128F300NBCKXUMA1	PG-LFBGA-292-6
SAK-TC297TP-128F300N BC	SP005411083	TC297TP128F300NBCKXUMA2	PG-LFBGA-292-10
SAK-TC297TP-128F300S BB	SP001207656	TC297TP128F300SBBKXUMA1	PG-LFBGA-292-6

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Sales name	SP number	OPN	Package
SAK-TC297TP-128F300S BC	SP001366094	TC297TP128F300SBCKXUMA1	PG-LFBGA-292-6
SAK-TC297TP-128F300S BC	SP005411084	TC297TP128F300SBCKXUMA2	PG-LFBGA-292-10
SAK-TC297TP-96F300N BC	SP001662190	TC297TP96F300NBCKXUMA1	PG-LFBGA-292-6
SAK-TC297TP-96F300N BC	SP005425539	TC297TP96F300NBCKXUMA2	PG-LFBGA-292-10
SAK-TC297TP-96F300S BB	SP001001102	TC297TP96F300SBBKXUMA1	PG-LFBGA-292-6
SAK-TC297TT-128F300N BC	SP001789674	TC297TT128F300NBCKXUMA1	PG-LFBGA-292-6
SAK-TC297TX-128F300N BC	SP001397674	TC297TX128F300NBCKXUMA1	PG-LFBGA-292-6
SAK-TC297TX-128F300N BC	SP005337854	TC297TX128F300NBCKXUMA2	PG-LFBGA-292-10
SAK-TC297TX-128F300S BB	SP001265592	TC297TX128F300SBBKXUMA1	PG-LFBGA-292-6
SAK-TC297TX-128F300S BB	SP005337850	TC297TX128F300SBBKXUMA2	PG-LFBGA-292-10
SAK-TC297TX-128F300S BC	SP001662196	TC297TX128F300SBCKXUMA1	PG-LFBGA-292-6
SAK-TC297TY-128F300S BB	SP001265594	TC297TY128F300SBBKXUMA1	PG-LFBGA-292-6
SAK-TC299T-128F300S BC	SP001662172	TC299T128F300SBCKXUMA1	PG-LFBGA-516-5
SAK-TC299TC-96F300S BB	SP001265604	TC299TC96F300SBBKXUMA1	PG-LFBGA-516-5
SAK-TC299TC-96F300S BC	SP001611508	TC299TC96F300SBCKXUMA1	PG-LFBGA-516-5