Product Change Notification / SYST-14ZXYE103

Date:

15-Mar-2022

Product Category:

Microprocessors

PCN Type:

Document Change

Notification Subject:

Data Sheet - SAMA5D2 Series Data Sheet Document Revision

Affected CPNs:

SYST-14ZXYE103_Affected_CPN_03152022.pdf
SYST-14ZXYE103_Affected_CPN_03152022.csv

Notification Text:

SYST-14ZXYE103

Microchip has released a new Product Documents for the SAMA5D2 Series Data Sheet of devices. If you are using one of these devices please read the document located at SAMA5D2 Series Data Sheet.

Notification Status: Final

Description of Change:

1) Global: Editorial changes throughout.

2) System Controller: Updated Block Diagram.

3) External Memories: I/O Lines Usage vs. Operating Mode: updated unit.

4) CPU System Bus Matrix (CPUMX)

a) Block Diagram: added.

b) Description: updated.

c) Embedded Characteristics: updated.

d) Remap: updated.

5) 18. Matrix (H64MX/H32MX)

a) Table Host to Client Access on H32MX: updated.

b) Table Peripheral Identifiers:

-updated PMC/PID1, PIT/PID3, WDT/PID4 and RSTC/PID73

-updated Note(3)

6) Watchdog Timer (WDT)

a) Block Diagram: updated.

b) Functional Description: updated.

c) WDT_CR: updated LOCKMR description.

7) Reset Controller (RSTC)

a) Block Diagram: modified.

b) Embedded Characteristics: updated.

c) 32.768 kHz Crystal Oscillator Failure Detection Reset: added.

d) Reset State Priorities: updated.

e) RSTC_SR: updated RSTTYP description.

f) RSTC_MR: added SCKSW at index 1, and description.

8) Real-time Clock (RTC)

a) Embedded Characteristics: updated.

b) Waveform Generation: updated.

c) RTC_CALR: updated.

d) Updated bit descriptions in RTC_CR, RTC_MR, RTC_TIMALR, RTC_CALALR.

9) Slow Clock Controller (SCKC)

a) Description: updated.

b) Block Diagram: updated.

c) Functional Description: updated.

10) Clock Generator: 12 MHz RC Oscillator Clock Frequency Adjustment: deleted.

11) Power Management Controller (PMC)

a) Throughout: SLCK renamed to TD_SLCK.

b) Figure Main System Bus Clock Controller: updated.

c) Programmable Clock Controller: updated.

d) Asynchronous Partial Wake-Up: updated.

e) Register Summary: offset 0x0110 now ‘reserved’.

f) Updated:

- CKGR_MOR
- PMC_IER
- PMC_IDR
- PMC_SR
- PMC_IMR

12) Parallel Input/Output Controller (PIO)

a) General Purpose or Peripheral Function Selection: updated.

b) Open-Drain Mode: added note.

c) Input Glitch and Debouncing Filters: updated.

13) DDR-SDRAM Controller (MPDDRC)

a) Product Dependencies, Initialization Sequence: added new step in initialization sequences

b) MPDDRC_CR: updated DIS_DLL and NDQS descriptions.

14) Static Memory Controller (SMC)

a) Embedded Characteristics: updated NFC_RAM characteristics.

b) HSMC_PMECCFG: updated SPAREEN and AUTO bit descriptions.

15) DMA Controller (XDMAC)

a) Updated memory-to-memory transfer information in:

- XDMAC Transfer Software Operation

- XDMAC Software Requirements

- XDMAC_CC

16) LCD Controller (LCDC)

a) Embedded Characteristics: modified bullets on Output mode.

b) Window Position, Size, Scaling and Striding Attributes: table title changed to “Window Size” from “YUV Mode and Window Size”.

c) YUV Frame Buffer Memory Mapping: replaced “interleaved” with “packed” throughout.

17) Gigabit Ethernet MAC (GMAC)

a) Embedded Characteristics, Priority Queueing in the DMA: updated.

b) 1588 Timestamp Unit: updated.

c) Updated table Receive Buffer Descriptor Entry.

d) Data Paths with Packet Buffers Included: modified figure (GMII becomes PHY TX Interface, PHY RX Interface) Updated MAC Transmit Block.

e) Interrupts: modified first sentence.

f) GMAC_NCR: modified bit descriptions.

g) GMAC_NCFGR: modified text for DBW and IRXER.

h) GMAC_TSR: added text for TXGO and HRESP.

i) GMAC_RBQB, GMAC_TBQB: modified text.

j) GMAC_RXUDAR, GMAC_TXUDAR: added.

18) USB Device High Speed Port (UDPHS)

a) Block Diagram: updated.

b) UDPHS_CTRL: updated EN_UDPHS bit description

19) USB Host High Speed Port (UHPHS)

a) UHPHS_ASYNCLISTADDR: removed sentence referring to non-existing UHPHS_CTRLDSSEGMENT register.

b) Corrected reset values for:

- UHPHS_HCSPARAMS

- UHPHS_HCCPARAMS

- UHPHS_PORTSCx

20) Flexible Serial Communication Controller (FLEXCOM)

a) Figure 46-2 and Figure 46-3: updated

b) RS485 Mode: Updated figure Example of RTS Drive with Timeguard and added Note.

c) Local Loopback Test Mode: added

d) Data Transfer:

- Table SPI Bus Protocol Mode: modified

- Figure titles modified to SPI Transfer Format (NCPHA = 1, 8 bits per transfer) Mode 0 and 2 and SPI Transfer Format (NCPHA = 0, 8 bits per transfer) Mode 1 and 3

e) Digital Filter: added.

f) Text added to:

- FIFO Multiple Data Access

- SPI Multiple Data Access

- TWI Multiple Data Access

g) Updated note in:

- FLEX_US_RHR

- FLEX_US_RHR (FIFO_MULTI_DATA)

- FLEX_US_THR

- FLEX_US_THR (FIFO_MULTI_DATA)

- FLEX_SPI_RDR

- FLEX_SPI_RDR (FIFO_MULTI_DATA_16)

- FLEX_SPI_RDR (FIFO_MULTI_DATA_8)

- FLEX_SPI_TDR

- FLEX_SPI_TDR (FIFO_MULTI_DATA)

- FLEX_TWI_RHR

- FLEX_TWI_RHR (FIFO_ENABLED)

- FLEX_TWI_THR

- FLEX_TWI_RHR (FIFO_ENABLED)

- FLEX_TWI_CR (FIFO_ENABLED)

- FLEX_TWI_SR (FIFO ENABLED)

h) FLEX_TWI_FILTR: added note.

21) Serial Peripheral Interface (SPI)

a) Local Loopback Test Mode: added.

b) Data Transfer: updated SPI Bus Prototcol Modes and figure titles.

22) Quad Serial Peripheral Interface (QSPI)

a) QSPI Block Diagram: modified.

b) Serial Clock Phase and Polarity: modified.

c) Table QSPI Bus Clock Modes: modified.

d) Scrambling/Unscrambling Function: updated.

e) SPI Local Loopback Test Mode: added.

f) QSPI_MR: modified SMRM.

g) QSPI_SCR: modified CPHA, CPOL.

23) Image Sensor Controller (ISC)

a) ISC Clock Management: updated.

b) ISC_CC_GB_OG: renamed field from ROFST to GOFST.

24) Controller Area Network (MCAN)

a) Power Management: removed “To achieve these frequencies, PMCGCLK must select the UPLLCK (480 MHz) as source clock and divide by 24,12, or 6.”

b) Standard Message ID Filter Element: corrected SFT index.

c) Updated:

- Dedicated Tx Buffers

- Tx Queue

d) Register Summary: offset 0x08 now ‘reserved’

25) Timer Counter (TC)

a) Embedded Characteristics: modified.

b) Table 53-2: modified.

c) Added note under 53.4. Pin List

d) Timer Counter Clock Assignment: deleted note on TIMER_CLOCK5.

e) Interrupt Sources: modified.

f) 53.6.3. Clock Selection: modified.

- Updated: 53.6.6. Trigger Events, Figure 53-5, Figure 53-7

g) TC_EMR: updated TRIGSRCB description.

26) Pulse Width Modulation Controller (PWM)

a) Throughout: updated number of comparison units.

b) PWM Controller Block Diagram: modified.

c) Fault Protection: modified.

d) External Trigger Mode Block Diagram: added.

e) Cycle-By-Cycle Duty Mode: LED String Control: modified.

f) Recoverable Fault: added 1 paragraph.

g) PWM External Trigger Mode: modified and new content added.

h) Application Example: modified.

27) Advanced Encryption Standard Bridge (AESB): Interrupt Sources: modified title and content.

28) Secure Hash Algorithm (SHA)

a) Throughout: updated FIPS specification reference

b) Updated Internal Registers for Initial Hash Value or Expected Hash Result

c) Manual Mode: modified step 4 & step 8

d) DMA Mode: added Note

e) Automatic Padding, SHA_MSR: added note

f) SHA_CR: updated FIRST bit description

g) SHA_IDATARx: updated IDATA field description

29) True Random Number Generator (TRNG)

a) Figure 62-1: updated.

b) Added:

- First Value Read after Power-up

- Entropy

30) Analog Comparator Controller (ACC): ACC_WPSR: updated bit descriptions.

31) Security Module (SECUMOD)

a) Updated:

- SECUMOD Block Diagram

- I/O Lines Description

- Interrupt Sources

- Memory Mapping

- Internal Random Number Generator (IRNG)

- PIO Backup Controller

- Erasing Secure Memories

32) Electrical Characteristics

a) Updated:

- 66.11.4.3. Example of LSB Computation

- 66.11.4.4. Gain and Offset Errors

- GMAC Timing Constraints

33) Schematic Checklist: Removed from data sheet to create standalone document, SAMA5D2 Hardware Design Considerations.

Impacts to Data Sheet: See above details.

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 15 Mar 2022

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

SAMA5D2 Series Data Sheet

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Affected Catalog Part Numbers(CPN)

ATSAMA5D28A-CU
ATSAMA5D27A-CU
ATSAMA5D24A-CU
ATSAMA5D22A-CU
ATSAMA5D27A-CUR
ATSAMA5D24A-CUR
ATSAMA5D22A-CUR
ATSAMA5D27B-CU
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