Product Change Notification / SYST-02WMHA586

Date:

07-Mar-2022

Product Category:

16-Bit - Microcontrollers and Digital Signal Controllers

PCN Type:

Document Change

Notification Subject:

ERRATA - dsPIC33CK256MP508 Family Silicon Errata and Data Sheet Clarification

Affected CPNs:

SYST-02WMHA586_Affected_CPN_03072022.pdf
SYST-02WMHA586_Affected_CPN_03072022.csv

Notification Text:

SYST-02WMHA586

Microchip has released a new Product Documents for the dsPIC33CK256MP508 Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at dsPIC33CK256MP508 Family Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change: 1. Updated the work around information for silicon issues 2 (I2C) and 3 (I2C).

2. Added data sheet clarifications 2 (Electrical Characteristics), 3 (Inter-Integrated Circuit (I2C)),4 (Instruction Set Summary), 5 (High-Speed, 12-Bit Analog-to-Digital Converter (ADC)) and 6 (Special Features). The I2C standard uses the terminology *"Master"* and *"Slave"*. The equivalent Microchip terminology used in this document is *"Host"* and *"Client"*, respectively.
Impacts to Data Sheet: None
Reason for Change: To Improve Productivity
Change Implementation Status: Complete
Date Document Changes Effective: 07 March 2022
NOTE: Please be advised that this is a change to the document only the product has not been changed.
Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

dsPIC33CK256MP508 Family Silicon Errata and Data Sheet Clarification

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Affected Catalog Part Numbers (CPN)

DSPIC33CK256MP505-H/PTVAO
DSPIC33CK256MP202T-I/2N
DSPIC33CK256MP502T-I/2N
DSPIC33CK128MP202T-I/2N
DSPIC33CK128MP502T-I/2N
DSPIC33CK64MP202T-I/2N
DSPIC33CK64MP502T-I/2N
DSPIC33CK32MP202T-I/2N
DSPIC33CK32MP502T-I/2N
DSPIC33CK256MP502T-I/2NVAO
DSPIC33CK256MP202T-I/SS
DSPIC33CK256MP502T-I/SS
DSPIC33CK128MP202T-I/SS
DSPIC33CK128MP502T-I/SS
DSPIC33CK64MP202T-I/SS
DSPIC33CK64MP502T-I/SS
DSPIC33CK32MP202T-I/SS
DSPIC33CK32MP502T-I/SS
DSPIC33CK256MP205T-I/M4
DSPIC33CK256MP505T-I/M4
DSPIC33CK128MP205T-I/M4
DSPIC33CK128MP505T-I/M4
DSPIC33CK64MP205T-I/M4
DSPIC33CK64MP505T-I/M4
DSPIC33CK32MP205T-I/M4
DSPIC33CK32MP505T-I/M4
DSPIC33CK256MP206T-I/MR
DSPIC33CK256MP506T-I/MR
DSPIC33CK128MP206T-I/MRC01
DSPIC33CK128MP206T-I/MR
DSPIC33CK128MP506T-I/MR
DSPIC33CK64MP206T-I/MR
DSPIC33CK64MP506T-I/MR
DSPIC33CK32MP206T-I/MR
DSPIC33CK32MP506T-I/MR
DSPIC33CK256MP203T-I/M5
DSPIC33CK256MP503T-I/M5
DSPIC33CK32MP502T-E/SS
DSPIC33CK32MP502T-E/SSVAO
DSPIC33CK256MP205T-E/M4
DSPIC33CK256MP505T-E/M4
DSPIC33CK64MP205T-E/M4C03
DSPIC33CK128MP205T-E/M4C06
DSPIC33CK128MP205T-E/M4
DSPIC33CK128MP505T-E/M4
DSPIC33CK64MP205T-E/M4

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DSPIC33CK32MP205T-E/M4
DSPIC33CK128MP505T-E/M4V02
DSPIC33CK64MP505T-E/M4VAO
DSPIC33CK256MP206T-E/MR
DSPIC33CK256MP506T-E/MR
DSPIC33CK256MP506T-E/MRC01
DSPIC33CK128MP206T-E/MR
DSPIC33CK128MP506T-E/MR
DSPIC33CK64MP206T-E/MR
DSPIC33CK64MP506T-E/MR
DSPIC33CK32MP206T-E/MR
DSPIC33CK32MP506T-E/MR
DSPIC33CK256MP506T-E/MRVAO
DSPIC33CK256MP203T-E/M5
DSPIC33CK256MP503T-E/M5
DSPIC33CK128MP203T-E/M5
DSPIC33CK128MP503T-E/M5
DSPIC33CK64MP203T-E/M5
DSPIC33CK64MP503T-E/M5
DSPIC33CK32MP203T-E/M5
DSPIC33CK32MP503T-E/M5
DSPIC33CK64MP503T-E/M5VAO
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DSPIC33CK64MP206T-E/PTC03
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DSPIC33CK128MP506T-E/PT
DSPIC33CK64MP206T-E/PT
DSPIC33CK64MP506T-E/PT
DSPIC33CK32MP206T-E/PT
DSPIC33CK32MP506T-E/PT
DSPIC33CK256MP506T-E/PTV08
DSPIC33CK256MP206T-E/PTVAO
DSPIC33CK256MP506T-E/PTVAO
DSPIC33CK64MP206T-E/PTVAO
DSPIC33CK64MP506T-E/PTVAO
DSPIC33CK256MP208T-E/PT
DSPIC33CK256MP508T-E/PT
DSPIC33CK256MP508T-E/PTC02
DSPIC33CK128MP208T-E/PTC05
DSPIC33CK128MP208T-E/PT
DSPIC33CK128MP508T-E/PT
DSPIC33CK64MP208T-E/PT
DSPIC33CK64MP508T-E/PT
DSPIC33CK128MP508T-E/PTV03
DSPIC33CK256MP508T-E/PTVAO
DSPIC33CK256MP205T-E/PT

DSPIC33CK256MP505T-E/PT
DSPIC33CK256MP505T-E/PTC03
DSPIC33CK32MP205T-E/PTC04
DSPIC33CK128MP205T-E/PTC05
DSPIC33CK128MP205T-E/PT
DSPIC33CK128MP505T-E/PT
DSPIC33CK64MP205T-E/PT
DSPIC33CK64MP505T-E/PT
DSPIC33CK32MP205T-E/PT
DSPIC33CK32MP505T-E/PT
DSPIC33CK256MP505T-E/PTV06
DSPIC33CK256MP505T-E/PTV07
DSPIC33CK256MP505T-E/PTVAO
DSPIC33CK128MP205T-E/PTVAO
DSPIC33CK128MP505T-E/PTVAO
DSPIC33CK64MP505T-E/PTVAO
DSPIC33CK64MP203-H/M5
DSPIC33CK64MP503-H/M5
DSPIC33CK32MP203-H/M5
DSPIC33CK32MP503-H/M5
DSPIC33CK256MP206-H/PT
DSPIC33CK256MP506-H/PT
DSPIC33CK128MP206-H/PT
DSPIC33CK128MP506-H/PT
DSPIC33CK64MP206-H/PT
DSPIC33CK64MP506-H/PT
DSPIC33CK32MP206-H/PT
DSPIC33CK32MP506-H/PT
DSPIC33CK256MP208-H/PT
DSPIC33CK256MP508-H/PT
DSPIC33CK128MP208-H/PT
DSPIC33CK128MP508-H/PT
DSPIC33CK64MP208-H/PT
DSPIC33CK64MP508-H/PT
DSPIC33CK256MP205-H/PT
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DSPIC33CK128MP205-H/PT
DSPIC33CK128MP505-H/PT
DSPIC33CK64MP205-H/PT
DSPIC33CK64MP505-H/PT
DSPIC33CK32MP205-H/PT
DSPIC33CK32MP505-H/PT
DSPIC33CK128MP203T-I/M5C01
DSPIC33CK64MP203T-I/M5C02
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DSPIC33CK256MP503T-I/M5VAO
DSPIC33CK64MP203T-I/M5VAO
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DSPIC33CK256MP502T-E/2N
DSPIC33CK64MP202T-E/2NC02
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DSPIC33CK64MP202T-E/2N
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DSPIC33CK256MP502-I/SS
DSPIC33CK32MP202-I/SSC01
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DSPIC33CK64MP502-I/SS
DSPIC33CK32MP202-I/SS
DSPIC33CK32MP502-I/SS
DSPIC33CK256MP205-I/M4
DSPIC33CK256MP505-I/M4
DSPIC33CK128MP205-I/M4C01
DSPIC33CK128MP205-I/M4
DSPIC33CK128MP505-I/M4
DSPIC33CK64MP205-I/M4
DSPIC33CK64MP505-I/M4
DSPIC33CK32MP205-I/M4
DSPIC33CK32MP505-I/M4
DSPIC33CK256MP206-I/MR
DSPIC33CK256MP506-I/MR
DSPIC33CK128MP206-I/MRC01
DSPIC33CK128MP206-I/MR
DSPIC33CK128MP506-I/MR
DSPIC33CK64MP206-I/MR
DSPIC33CK64MP506-I/MR
DSPIC33CK32MP206-I/MR
DSPIC33CK32MP506-I/MR
DSPIC33CK256MP203-I/M5
DSPIC33CK256MP503-I/M5
DSPIC33CK64MP203-I/M5C02
DSPIC33CK64MP503-I/M5C03
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DSPIC33CK32MP503-I/M5
DSPIC33CK64MP203-I/M5VAO
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DSPIC33CK32MP506-I/PT
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DSPIC33CK64MP205-I/PTC04
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DSPIC33CK128MP502-H/2N
DSPIC33CK64MP202-H/2N
DSPIC33CK64MP502-H/2N
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DSPIC33CK32MP502-H/SS
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DSPIC33CK256MP505-H/M4
DSPIC33CK128MP205-H/M4
DSPIC33CK128MP505-H/M4
DSPIC33CK64MP205-H/M4
DSPIC33CK64MP505-H/M4
DSPIC33CK32MP205-H/M4
DSPIC33CK32MP505-H/M4
DSPIC33CK256MP205-H/M4VAO
DSPIC33CK256MP206-H/MR
DSPIC33CK256MP506-H/MR
DSPIC33CK128MP206-H/MR
DSPIC33CK128MP506-H/MR
DSPIC33CK64MP206-H/MR
DSPIC33CK64MP506-H/MR
DSPIC33CK32MP206-H/MR
DSPIC33CK32MP506-H/MR
DSPIC33CK256MP203-H/M5
DSPIC33CK256MP503-H/M5
DSPIC33CK128MP203-H/M5
DSPIC33CK128MP503-H/M5

dsPIC33CK256MP508

dsPIC33CK256MP508 Family Silicon Errata and Data Sheet Clarification

The dsPIC33CK256MP508 family devices that you have received conform functionally to the current Device Data Sheet (DS70005349**J**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the dsPIC33CK256MP508 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**B3**).

Data Sheet clarifications and corrections start on page 9, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various dsPIC33CK256MP508 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)		
		A1	B2	B3
dsPIC33CK256MP508 Family With CAN FD				
dsPIC33CK256MP508	0x7C74	0x0001	0x0004	0x0005
dsPIC33CK256MP506	0x7C73			
dsPIC33CK256MP505	0x7C72			
dsPIC33CK256MP503	0x7C71			
dsPIC33CK256MP502	0x7C70			
dsPIC33CK128MP508	0x7C64			
dsPIC33CK128MP506	0x7C63			
dsPIC33CK128MP505	0x7C62			
dsPIC33CK128MP503	0x7C61			
dsPIC33CK128MP502	0x7C60			

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"dsPIC33CK256MP508 Family Flash Programming Specification"* (DS70005300) for detailed information on Device and Revision IDs for your specific device.

TABLE 1: SILICON DEVREV VALUES (CONTINUED)

Part Number	Device ID[1]	Revision ID for Silicon Revision[2]		
		A1	B2	B3
dsPIC33CK256MP508 Family With CAN FD (Continued)				
dsPIC33CK64MP508	0x7C54	0x0001	0x0004	0x0005
dsPIC33CK64MP506	0x7C53			
dsPIC33CK64MP505	0x7C52			
dsPIC33CK64MP503	0x7C51			
dsPIC33CK64MP502	0x7C50			
dsPIC33CK32MP506	0x7C43			
dsPIC33CK32MP505	0x7C42			
dsPIC33CK32MP503	0x7C41			
dsPIC33CK32MP502	0x7C40			
dsPIC33CK256MP508 Family Without CAN FD				
dsPIC33CK256MP208	0x7C34	0x0001	0x0004	0x0005
dsPIC33CK256MP206	0x7C33			
dsPIC33CK256MP205	0x7C32			
dsPIC33CK256MP203	0x7C31			
dsPIC33CK256MP202	0x7C30			
dsPIC33CK128MP208	0x7C24			
dsPIC33CK128MP206	0x7C23			
dsPIC33CK128MP205	0x7C22			
dsPIC33CK128MP203	0x7C21			
dsPIC33CK128MP202	0x7C20			
dsPIC33CK64MP208	0x7C14			
dsPIC33CK64MP206	0x7C13			
dsPIC33CK64MP205	0x7C12			
dsPIC33CK64MP203	0x7C11			
dsPIC33CK64MP202	0x7C10			
dsPIC33CK32MP206	0x7C03			
dsPIC33CK32MP205	0x7C02			
dsPIC33CK32MP203	0x7C01			
dsPIC33CK32MP202	0x7C00			

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format “DEVID DEVREV”.

2: Refer to the *“dsPIC33CK256MP508 Family Flash Programming Specification”* (DS70005300) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions		
				A1	B2	B3
I²C	Interrupt	1.	In Client mode, incorrect interrupt is generated when DHEN = 1.	X	X	X
I²C	Error	2.	Bus collision error cannot be cleared.	X	X	X
I²C	Error	3.	False bus collision error generated.	X	X	X
I²C	Idle	4.	Address cannot be received in Idle mode.	X	X	X
Oscillator	PLL	5.	FRCDIVN drives the PLL instead of the FRC.	X	X	X
Oscillator	HS, XT	6.	Removed.			
PWM	Dead Time	7.	When feed-forward PCI is used for dead-time compensation (DTCMPSEL = 1), the PWMx outputs are overridden.	X	X	X
UART	OERR	8.	The OERR bit cannot be cleared by software.	X	X	X
UART	FERR	9.	The FERR bit will not get set if one Stop bit is received.	X	X	X
UART	OERR	10.	The 9th byte received will not be available to be read.	X	X	X
UART	TRMT	11.	The TRMT bit takes time to set on the last transmit completion.	X	X	X
UART	TRMT	12.	The TRMT bit is unreliable when there is back-to-back Break character transmission.	X	X	X
UART	Idle	13.	The RIDLE bit takes one instruction cycle to get cleared after ABAUD is set.	X	X	X
UART	TXWRE	14.	The TXWRE bit (UxSTAH[7]) cannot be cleared once it gets set.	X	X	X
UART	Address Detect	15.	When writing to UxP1 with UTXBRK = 1, the content of P1 will not get transmitted.	X	X	X
UART	Address Detect	16.	In Address Detect mode, the content of P1 is not transmitted on writing to P1 with UTXBRK = 1.	X	X	X
UART	Sleep	17.	When waking from Sleep with a UART reception, SLPEN needs to be set in addition to WAKE = 1.	X	X	X
UART	Smart Card	18.	The Wait Time Counter Interrupt Flag (WTCIF) is set when the last character transmitted has the bit, LAST = 0.	X	X	X
UART	XOFF	19.	XOFF is transmitted when one empty space remains in the RX buffer.	X	X	X
MBIST	MBISTDONE	20.	After executing a Reset, the MBISTDONE bit will always be set.	X	X	X
CPU	FLIM Instruction	21.	When the operands are of different signs, the FLIM instruction may not force the correct data limit.	X	X	X
SCCP/ MCCP	Clock Source	22.	Using FOSC as the clock source may cause synchronization issues.	X	X	X
I²C	SMBus 3.0	23.	When Configuration bit, SMBEN (FDEVOPT[10]) = 1, the SMBus 3.0 VIH minimum specification may not be met.	X		
I/O	POR	24.	Spike on I/O at POR.	X		
CPU	DIV.SD Instruction	25.	Overflow bit is not getting set when an overflow occurs.	X	X	X
CPU	MAXAB/MINAB/ MINZAB Instructions	26.	MAXAB, MINAB and MINZAB do not work for different sign operands.	X	X	X
DMA	ADC Triggers	27.	DMA is triggered continuously from ADC.	X		
PWM	Time Base Capture	28.	PWM Capture Status (CAP) flag will not set again under certain conditions.	X	X	X
I²C	I²C	29.	All instances of I²C may exhibit errors and should not be used.	X		
Oscillator	VCO and AVCO Dividers	30.	Main and auxiliary PLL external VCO dividers can fail to output the clock signal.	X	X	

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**B3**).

1. Module: I²C

In Client mode with DHEN = 1 (Data Hold Enable), if software sends a NACK, a Client interrupt is asserted at the 9th falling edge of the clock.

Work around

Software should ignore the Client interrupt that is asserted after sending a NACK.

Affected Silicon Revisions

A1	B2	B3					
X	X	X					

2. Module: I²C

In Client mode, the Bus Collision Detect bit (BCL) cannot be cleared when bus collision detection is enabled (SBCDE = 1).

Work around

In the bus collision interrupt routine, once the interrupt is asserted, clear the BCL after Stop condition setup time.

1. On actual bus collision, BCL bit cannot be cleared. To clear the BCL bit, the I²C module should be disabled first, followed by clearing the BCL bit and re-enabling the I²C module.
2. The BCL bit can be cleared if it was falsely asserted during a Stop bit.

   False and actual bus collision can be distinguished by keeping the bus collision interrupt priority higher than that of the Client interrupt priority.

Affected Silicon Revisions

A1	B2	B3					
X	X	X					

3. Module: I²C

In Client mode, false bus collision triggers are generated when the bus collision is enabled (SBCDE = 1) and a Stop bit is received.

Work around

In the bus collision interrupt routine, once the interrupt is asserted, clear the BCL after the Stop condition setup time. Refer to TSU:STO for the Stop condition setup time in **Table 33-34** of **Section 33.0 "ELECTRICAL CHARACTERISTICS"** in the current device data sheet (DS70005349**J**).

Affected Silicon Revisions

A1	B2	B3					
X	X	X					

4. Module: I²C

In Client mode, an address cannot be received when the device is in Idle and the module is set for discontinue in Idle (I2CSIDL = 1).

Work around

None.

Affected Silicon Revisions

A1	B2	B3					
X	X	X					

5. Module: Oscillator

When using the 8 MHz internal FRC Oscillator with Primary PLL as either a system clock or a peripheral source, FRCDIVN drives the PLL instead of the FRC.

This means that the PLL FRC input selection is subject to the FRCDIV[2:0] bits and could lead to a condition where the minimum PLL input requirement of 8 MHz is not maintained.

Work around

Ensure FRCDIV[2:0] bits are maintained as zero when using FRCPLL as either a system clock or a peripheral source.

Affected Silicon Revisions

A1	B2	B3					
X	X	X					

6. Module: Oscillator

This errata is no longer applicable to any silicon revisions of this product. See **Section 2.5 "External Oscillator Pins"** in the current device data sheet (DS70005349**J**) for guidance on oscillator design to avoid start-up related issues.

7. Module: PWM

When feed-forward PCI is used for dead-time compensation (DTCMPSEL = 1), the PWMx outputs are overridden.

Work around

Use Sync PCI (DTCMPSEL = 0) for dead-time compensation.

Affected Silicon Revisions

A1	B2	B3					
X	X	X					

8. Module: UART

Once the UART receive buffer overflows and the OERR bit (UxSTA[1]) is set, the OERR bit cannot be cleared by software.

Work around

1. Make sure that the receive buffer never overflows. Do not let the OERR bit get set by reading the received data byte on each byte reception.
2. Disable and enable UART before clearing the OERR bit.

Affected Silicon Revisions

A1	B2	B3					
X	X	X					

9. Module: UART

When the UART is operating with STSEL[1:0] = 2 (two Stop bits sent, two checked at receive), the FERR bit will not get set if one Stop bit is received.

Work around

3. Use STSELx = 3 instead of STSELx = 2. When operating with STSELx = 3 mode, the UART will be configured to send two Stop bits, but check one at receive.

Affected Silicon Revisions

A1	B2	B3					
X	X	X					

10. Module: UART

When the receive buffer overflows, the 9th byte received will get lost and cannot be read.

Work around

Do not allow the OERR bit to get set by reading the received data byte on each byte reception.

Affected Silicon Revisions

A1	B2	B3					
X	X	X					

11. Module: UART

At low BRG value, the TRMT bit takes time to set on the last transmit completion, which may result in the transmitted data getting lost.

Work around

1. Use the UTXBE bit to monitor for the next transmit.
2. Provide a delay to stabilize the POSC.

Affected Silicon Revisions

A1	B2	B3					
X	X	X					

12. Module: UART

The Transmit Shifter Empty (TRMT) bit is unreliable when there is back-to-back Break character transmission.

Work around

Poll the UART Transmit Break bit, UTXBRK (UxMODE[8]), to be cleared instead of the TRMT bit.

Affected Silicon Revisions

A1	B2	B3					
X	X	X					

13. Module: UART

During the UART Auto-Baud Detection sequence, the RIDLE bit takes one instruction cycle to get cleared after ABAUD is set.

Work around

Ignore the RIDLE bit until the Auto-Baud Detection sequence is complete.

Affected Silicon Revisions

A1	B2	B3					
X	X	X					

14. Module: UART

Once the TX Write Transmit Error Status bit, TXWRE (UxSTAH[7]), gets set, the TXWRE cannot be cleared by a single clear instruction.

Work around

Use multiple clear instructions in a loop until the TXWRE bit gets cleared.

Affected Silicon Revisions

A1	B2	B3					
X	X	X					

15. Module: UART

In UART Address Detect mode, writing to UxP1 with UTXBRK = 1 should cause a Break to be transmitted, followed by the content in P1, but the content of P1 will not get transmitted.

Work around

After writing to P1, wait for UTXBRK to get clear and then rewrite to P1.

Affected Silicon Revisions

A1	B2	B3					
X	X	X					

16. Module: UART

In Address Detect mode, the content of P1 is not transmitted on writing to P1 with UTXBRK = 1.

Work around

Write P1 a second time after waiting for the Break transmission to start.

Affected Silicon Revisions

A1	B2	B3					
X	X	X					

17. Module: UART

When waking from Sleep with a UART reception, SLPEN needs to be set in addition to WAKE = 1.

Work around

Set the SPLEN bit in addition to WAKE before entering Sleep.

Affected Silicon Revisions

A1	B2	B3					
X	X	X					

18. Module: UART

In Smart Card T = 1 mode, the Wait Time Counter Interrupt Flag (WTCIF) is set when the last character transmitted has the bit, LAST = 0.

Work around

Ignore WTC interrupt events on non-last bytes.

Affected Silicon Revisions

A1	B2	B3					
X	X	X					

19. Module: UART

In Software Flow Control mode, XOFF is transmitted when one empty space remains in the RX buffer. XOFF transmission can get further delayed if the transmitter has already been loaded, resulting in XOFF transmission on a receive buffer full event.

Work around 1

Give a minimum one-byte delay before each byte transmission.

Work around 2

Use the UART RX interrupt with URXISEL[2:0] set to at least two empty slots. This allows the RX buffer to be read in time to prevent RX buffer overflow.

Affected Silicon Revisions

A1	B2	B3					
X	X	X					

20. Module: MBIST

After a Reset, the MBISTDONE status bit will be set regardless of a BIST test being executed. If a BIST is requested and executed, the MBISTDONE bit will be set as expected.

Work around

None.

Affected Silicon Revisions

A1	B2	B3					
X	X	X					

21. Module: CPU

The FLIM instruction may incorrectly limit the data range when operating on signed operands of different sign values. If the operands are either all negative or all positive, the limit is correct.

Work around

None.

Affected Silicon Revisions

A1	B2	B3					
X	X	X					

22. Module: SCCP/MCCP

When FOSC is selected as the clock source using the CLKSEL[2:0] bits (CCPxCON1L[10:8]), unexpected operation may occur. For proper SCCP/MCCP input clock synchronization, do not use FOSC as the system clock source.

Work around

Use any of the other available clock sources in CLKSEL[2:0].

Affected Silicon Revisions

A1	B2	B3					
X	X	X					

23. Module: I²C

When selecting SMBus 3.0 operation using Configuration bit, SMBEN (FDEVOPT[10]), the Voltage Input High (VIH) of the SMBus 3.0 specification minimum may not be met.

Work around

None.

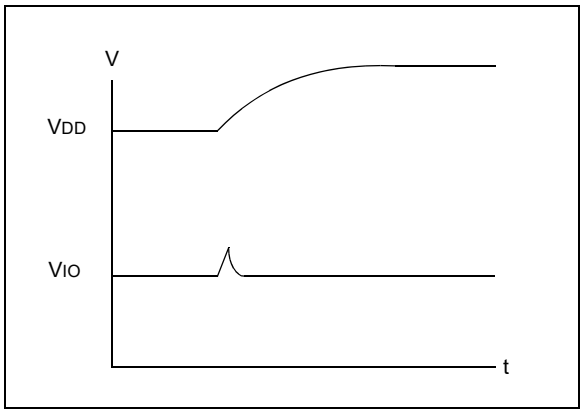
Affected Silicon Revisions

A1	B2	B3					
X							

24. Module: I/O

During a fast device power-up when the VDD ramp is less than 4 mS, the I/O pins may drive up to 100 µA current for a duration of up to 10 µS (Figure 1-1).

FIGURE 1-1: I/O RAMP



Work around

1. Slow down the VDD ramp time (greater than 4 mS for VDD to ramp 0V to 3.3V).
2. Ensure the circuitry that is connected to the pins can endure this pulse.

Example applications affected may include complementary power switches, where a transient current shoot-through might occur. High-voltage applications with complementary switches should power the high-voltage 200 µSec later than powering the dsPIC® device to avoid the current shoot-through. This behavior is specific to each device and not affected by aging.

Affected Silicon Revisions

A1	B2	B3					
X							

25. Module: CPU

When using the Signed 32-by-16-bit Division instruction, DIV.SD, the Overflow bit may not always get set when an overflow occurs.

Work around

Test for and handle overflow conditions outside of the div.sd instruction.

Affected Silicon Revisions

A1	B2	B3					
X	X	X					

26. Module: CPU

When operating on signed operands of different sign values, the output for MAXAB, MINAB and MINZAB instructions may be incorrect. If the operands are either all negative or all positive, the output is correct.

Work around

None.

Affected Silicon Revisions

A1	B2	B3					
X	X	X					

27. Module: DMA

The DMA receives multiple continuous triggers from the ADC until the trigger event from the ADC is cleared. The OVRUNIF flag (DMAINTn[3]) will be set. When the OVRUNIF bit changes state from '0' to '1', a DMA interrupt is generated.

Work around

Ignore the OVRUNIF bit and the first DMA interrupt. Clear the ADC trigger source (ANxRDY) with a DMA read of the ADC buffer, ADCBUFx, for the corresponding ADC channel.

Affected Silicon Revisions

A1	B2	B3					
X							

28. Module: PWM

When using a PWM Control Input (PCI) to trigger a time base capture, the Capture Status flag, CAP (PGxSTAT[5]), may not set again under certain conditions. When a subsequent PWM capture event occurs while, or just after, reading the current capture value from the PGxCAP register, the Capture Status Flag, CAP, will not set again.

Work around

Read the PWM Generator Capture (PGxCAP, x = 1 to 8) register at a known time to avoid the condition. The timing of the PGxCAP read operation can be scheduled by using PWM Generator x (1-8) interrupt or any of the six PWM Event (A-F) interrupts corresponding to the PCI event which triggered the time base capture. Read the PGxCAP value after the CAP bit has set within the interrupt.

Affected Silicon Revisions

A1	B2	B3					
X	X	X					

29. Module: I^2C

All instances of I^2C/SMBus may exhibit errors and should not be used. When operating I^2C/SMBus in a noisy environment, the I^2C module may exhibit various errors. These errors may include, but are not limited to, corrupted data, unintended interrupts or the I^2C bus getting hung up due to injected noise. Examples of system noise include, but are not limited to, PWM outputs or other pins toggled at high speed adjacent to the I^2C pins. Both Host and Client I^2C/SMBus modes may exhibit this issue.

Work around

If I^2C is required, use a software I^2C implementation. An example I^2C software library is available from Microchip:

www.microchip.com/dsPIC33C_I2C_SoftwareLibrary

Affected Silicon Revisions

A1	B2	B3					
X							

30. Module: Oscillator

At PLL start-up, the main and auxiliary PLL VCO dividers may occasionally halt and not provide a clock output. The VCO and AVCO dividers can be selected as clock sources for different peripheral modules, including the ADC, PWM, DAC, CAN FD, UART, etc. VCO and AVCO divider outputs, FVCO/2, FVCO/3, FVCO/4, FVCODIV, AFVCO/2, AFVCO/3, AFVCO/4 and AFVCODIV outputs are affected.

Work around

1. Use another clock source, such as the FOSC, PLL or APLL output (FPOLLO and AFPOLLO) instead of the VCO or AVCO dividers.
2. If the application requires the VCO/AVCO divider, test the clock source before using the peripheral in the end application. System resources, including a timer, I/O pin state or interrupts, can be used to detect and verify peripheral activity for presence of the VCO divider clock output. Any type of Reset may recover the VCO divider clock (Software Reset, WDT, MCLR or POR).

Affected Silicon Revisions

A1	B2	B3					
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70005349**J**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Electrical Characteristics

Table 33-41 has been updated as shown below in **bold**.

TABLE 33-41: OPERATIONAL AMPLIFIER SPECIFICATIONS

Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended							
Param No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Comments
OA01	GBWP	Gain Bandwidth Product	—	20	—	MHz	
OA02	SR	Slew Rate	—	40	—	V/µs	
OA03	VIOFF	Input Offset Voltage	-3**(3)**	**-1/+1**	+3**(3)**	**mV**	**Unity gain configuration**
			-8	**-3/+3**	**+8**	**nA**	**Open-loop configuration**
OA04	VIBC	Input Bias Current	—	—	—	mV	Note 2
OA05	VICM	Common-Mode Input Voltage Range	AVSS	—	AVDD	V	NCHDISx = 0
			AVSS	—	AVDD – 1.4	V	NCHDISx = 1
OA07	CMRR	Common-Mode Rejection Ratio	—	68	—	dB	
OA08	PSRR	Power Supply Rejection Ratio	—	74	—	dB	
OA09	VOR	Output Voltage Range	AVSS	—	AVDD	mV	0.5V input overdrive, no output loading (Note 1)
OA11	CLOAD	Output Load Capacitance	—	—	30	pF	Including output pin capacitance (Note 1)
OA12	IOUT	Output Current Drive Strength	—	3	—	mA	Sink and source
OA13	PMARGIN	Phase Margin	44	—	—	degree	Unity gain (Note 1)
OA14	GMARGIN	Gain Margin	7	—	—	dB	Unity gain (Note 1)
OA15	OLG	Open-Loop Gain	68	75	—	dB	Note 1

Note 1: These parameters are for design guidance only and are not tested in manufacturing.

2: The op amps use CMOS input circuitry with negligible input bias current. The maximum “effective bias current” is the I/O pin leakage specified by electrical Parameter DI50.

3: Parameters are characterized but not tested in manufacturing.

2. Module: Electrical Characteristics

Table 33-7 has been updated as shown below in **bold**.

TABLE 33-7: POWER-DOWN CURRENT (IPD)(2)

Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended						
Parameter No.	Characteristic	Typ.(1)	Max.	Units	Conditions	
DC60	Base Power-Down Current	270	650	µA	-40°C	3.3V
		419	**1400**	µA	+25°C	
		940	7250	µA	+85°C	
		5.59	18.5	mA	+125°C(3)	

3. Module: Inter-Integrated Circuit (I^2C)

Equation 18-1 has been updated as shown below in **bold**.

EQUATION 18-1: COMPUTING BAUD RATE RELOAD VALUE

$$I2CxBRG = ((\mathbf{1/F_{SCL} - Delay}) \bullet \mathbf{F_P/2}) - 2$$

4. Module: Instruction Set Summary

Table 31-2 has been updated as shown below in **bold**.

5. Module: High-Speed, 12-Bit Analog-to-Digital Converter (ADC)

In **Section 13.2 "Temperature Sensor"**, the ADC channel that is connected to a forward-biased diode has changed from AN19 to AN24.

6. Module: Special Features

In **Register 30-20: VREGCON: Voltage Regulator Control Register**, the Unimplemented bits[14:6] have been changed from Read as '1' to Read as '0' and have a new Note 1:

Note 1: Hardware resets this register only on a POR Reset.

TABLE 31-2: INSTRUCTION SET OVERVIEW

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles(1)	Status Flags Affected
36	DIV.S(2)	DIV.S Wm,Wn	Signed 16/16-bit Integer Divide	1	**6**	N,Z,C,OV
		DIV.SD Wm,Wn	Signed 32/16-bit Integer Divide	1	**6**	N,Z,C,OV
37	DIV.U(2)	DIV.U Wm,Wn	Unsigned 16/16-bit Integer Divide	1	**6**	N,Z,C,OV
		DIV.UD Wm,Wn	Unsigned 32/16-bit Integer Divide	1	**6**	N,Z,C,OV

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (5/2018)

Initial release of this document; issued for revision A1.

Rev B Document (9/2018)

Added silicon issues 21 (CPU), 22 (SCCP/MCCP) and 23 (I^2C).

Rev C Document (12/2018)

Added silicon issues 24 (I/O), 25 (CPU), 26 (CPU) and 27 (CPU).

Rev D Document (3/2019)

Added silicon issues 28 (DMA) and 29 (PWM).

Updated reference to current Device Data Sheet revision (DS70005349**F**).

Rev E Document (10/2019)

Updated silicon issue 24 (I/O) and silicon issue 28 (PWM).

Removed silicon issue 27 (CPU) which stated that the upper byte of the destination register may not be persistent.

Updated reference to current Device Data Sheet revision (DS70005349**G**).

Rev F Document (12/2019)

Added silicon issue 29 (I^2C).

Rev G Document (6/2020)

Added silicon issue 30 (Oscillator).

Added data sheet clarification (Document Revision History).

Removes silicon issue 6 (Oscillator) since it is no longer applicable.

Rev H Document (7/2020)

Added silicon revision B2.

Updated the wording in silicon issue 29 (I^2C).

Removed data sheet clarification (Electrical Characteristics) since it was addressed in the latest device data sheet.

Rev J Document (2/2021)

Added silicon revision B3.

Added data sheet clarification 1 (Electrical Characteristics).

Rev K Document (3/2022)

Updated the work around information for silicon issues 2 (I^2C) and 3 (I^2C).

Added data sheet clarifications 2 (Electrical Characteristics), 3 (Inter-Integrated Circuit (I2C)), 4 (Instruction Set Summary), 5 (High-Speed, 12-Bit Analog-to-Digital Converter (ADC)) and 6 (Special Features).

The I^2C standard uses the terminology *"Master"* and *"Slave"*. The equivalent Microchip terminology used in this document is *"Host"* and *"Client"*, respectively.

NOTES:

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China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

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India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
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