



## Product Change Notification / SYST-17WQJD265

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**Date:**

18-Feb-2022

**Product Category:**

Driver / Interface ICs

**PCN Type:**

Document Change

**Notification Subject:**

Data Sheet - MIC5891 - 8-Bit Serial-Input Latched Source Driver

**Affected CPNs:**

[SYST-17WQJD265\\_Affected\\_CPN\\_02182022.pdf](#)

[SYST-17WQJD265\\_Affected\\_CPN\\_02182022.csv](#)

**Notification Text:**

SYST-17WQJD265

Microchip has released a new Product Documents for the MIC5891 - 8-Bit Serial-Input Latched Source Driver of devices. If you are using one of these devices please read the document located at [MIC5891 - 8-Bit Serial-Input Latched Source Driver](#).

**Notification Status:** Final

**Description of Change:** Corrected the device marking specification in Section 5.1, Package Marking Information.

**Impacts to Data Sheet:** None

**Reason for Change:** To Improve Productivity

**Change Implementation Status:** Complete

**Date Document Changes Effective:** 18 Feb 2022

**NOTE:** Please be advised that this is a change to the document only the product has not been changed.

**Markings to Distinguish Revised from Unrevised Devices:** N/A

## Attachments:

[MIC5891 - 8-Bit Serial-Input Latched Source Driver](#)

Please contact your local [Microchip sales office](#) with questions or concerns regarding this notification.

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## 8-Bit Serial-Input Latched Source Driver

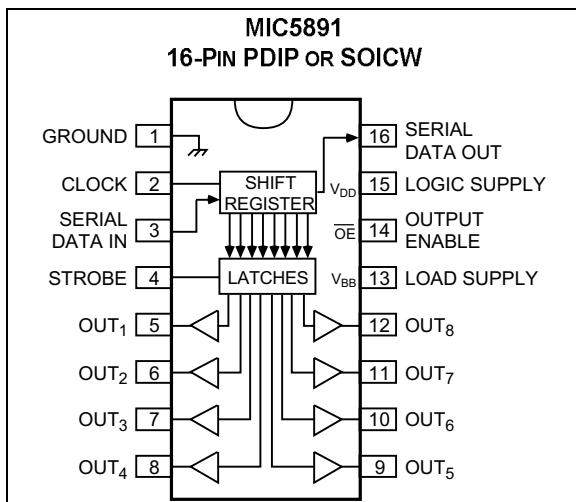
### Features

- High-Voltage, High-Current Outputs
- Output Transient Protection Diodes
- CMOS-, PMOS-, NMOS-, and TTL-Compatible Inputs
- 5 MHz Typical Data Input Rate
- Low-Power CMOS Latches

### Applications

- Alphanumeric and Bar Graph Displays
- LED and Incandescent Displays
- Relay and Solenoid Drivers
- Other High-Power Loads

### Package Type



### General Description

The MIC5891 latched driver is a high-voltage, high-current integrated circuit comprised of eight CMOS data latches, CMOS control circuitry for the common STROBE and OUTPUT ENABLE, and bipolar Darlington transistor drivers for each latch.

Bipolar/MOS construction provides extremely low power latches with maximum interface flexibility.

The MIC5891 will typically operate at 5 MHz with a 5V logic supply.

The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS logic levels. TTL circuits may be used with appropriate pull-up resistors to ensure a proper logic-high input.

A CMOS serial data output allows additional drivers to be cascaded when more than 8 bits are required.

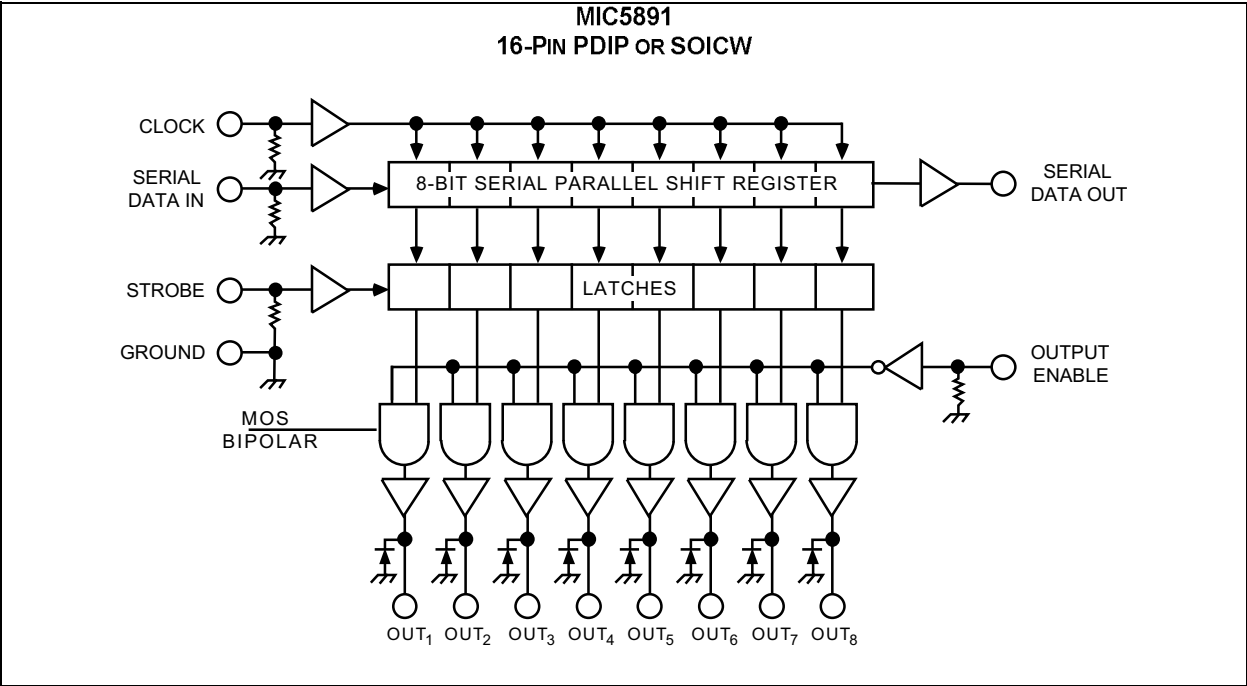
The MIC5891 has open-emitter outputs with suppression diodes for protection against inductive load transients. The output transistors are capable of sourcing 500 mA and will sustain at least 35V in the on-state.

Simultaneous operation of all drivers at maximum rated current requires a reduction in duty cycle due to package power limitations. Outputs may be paralleled for higher load current capability.

The MIC5891 is available in a 16-pin plastic DIP package (N) and 16-pin wide SOIC package (WM).

# MIC5891

## Functional Diagram



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings † (Note 1, Note 2, Note 3)

|   |                                |
|---|--------------------------------|
| Output Voltage ( $V_{OUT}$ ) .....            | +50V                           |
| Logic Supply Voltage Range ( $V_{DD}$ ) ..... | +4.5V to +15V                  |
| Load Supply Voltage Range ( $V_{BB}$ ) .....  | +5.0V to +50V                  |
| Input Voltage Range ( $V_{IN}$ ) .....        | -0.3V to ( $V_{DD} + 0.3V$ )   |
| Continuous Collector Current ( $I_C$ ) .....  | 500 mA                         |
| Package Power Dissipation .....               | See <a href="#">Figure 2-1</a> |

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Note 1:**  $T_A = +25^\circ\text{C}$ .

**2:** Derate at the rate of 20 mW/°C above  $T_A = +25^\circ\text{C}$ .

**3:** Microchip CMOS devices have input-static protection, but are susceptible to damage when exposed to extremely high static electrical charges.

**TABLE 1-1: ALLOWABLE DUTY CYCLES**

| Number of Outputs ON at<br>$I_{OUT} = -200\text{ mA}$ | Maximum Allowable Duty Cycles at a $T_A$ of: |       |       |
|---|--|-------|-------|
|   | +50°C  | +60°C | +70°C |
| 8   | 53%  | 47%   | 41%   |
| 7   | 60%  | 54%   | 48%   |
| 6   | 70%  | 64%   | 56%   |
| 5   | 83%  | 75%   | 67%   |
| 4   | 100%   | 94%   | 84%   |
| 3   | 100%   | 100%  | 100%  |
| 2   | 100%   | 100%  | 100%  |
| 1   | 100%   | 100%  | 100%  |

# MIC5891

## Electrical Characteristics

| Electrical Characteristics: $V_{BB} = 50V$ , $V_{DD} = 5V$ to $12V$ ; $T_A = 25^\circ C$ , unless noted. (Note 1). |                            |              |      |  |            |  |
|--|----------------------------|--------------|------|--|------------|--|
| Parameters   | Sym.                       | Min.         | Typ. | Max.   | Units      | Conditions                                       |
| Output Leakage Current   | $I_{CEX}$                  | —            | —    | -50  | $\mu A$    | $T_A = +25^\circ C$                              |
|  |                            | —            | —    | -100   | $\mu A$    | $T_A = +85^\circ C$                              |
| Output Saturation Voltage  | $V_{CE(SAT)}$              | —            | —    | 2.3  | V          | $I_{OUT} = -100$ mA, $T_A = +85^\circ C$         |
|  |                            | —            | —    | 2.4  | V          | $I_{OUT} = -225$ mA, $T_A = +85^\circ C$         |
|  |                            | —            | —    | 2.5  | V          | $I_{OUT} = -350$ mA, $T_A = +85^\circ C$         |
| Output Sustaining Voltage  | $V_{CE(SUS)}$              | 35           | —    | —  | V          | $I_{OUT} = -350$ mA, $L = 2$ mH                  |
| Input Voltage  | $V_{IN(1)}$<br>$V_{IN(0)}$ | 3.5          | —    | $V_{DD}+0.3$                                   | V          | $V_{DD} = 5.0V$                                  |
|  |                            | 10.5         | —    | $V_{DD}+0.3$                                   | V          | $V_{DD} = 12V$                                   |
|  |                            | $V_{SS}-0.3$ | —    | 0.8  | V          | $V_{DD} = 5.0V$ to $12V$                         |
| Input Current  | $I_{IN(1)}$                | —            | —    | 120  | $\mu A$    | $V_{DD} = V_{IN} = 5.0V$                         |
|  |                            | —            | —    | 240  | $\mu A$    | $V_{DD} = 12V$                                   |
| Input Impedance  | $Z_{IN}$                   | 100          | —    | —  | k $\Omega$ | $V_{DD} = 5.0V$                                  |
|  |                            | 50           | —    | —  | k $\Omega$ | $V_{DD} = 12V$                                   |
| Maximum Clock Frequency  | $f_c$                      | 3.3          | —    | —  | MHz        | —  |
| Serial Data Output Resistance  | $R_{OUT}$                  | —            | —    | 20   | k $\Omega$ | $V_{DD} = 5.0V$                                  |
|  |                            | —            | —    | 6.0  | k $\Omega$ | $V_{DD} = 12V$                                   |
| Turn-On Delay  | $t_{PLH}$                  | —            | —    | 2.0  | $\mu s$    | Output Enable to Output,<br>$I_{OUT} = -350$ mA  |
| Turn-Off Delay   | $t_{PHL}$                  | —            | —    | 10   | $\mu s$    | Output Enable to Output,<br>$I_{OUT} = -350$ mA  |
| Supply Current   | $I_{BB}$                   | —            | —    | 10   | mA         | All outputs on, all outputs open                 |
|  |                            | —            | —    | 200  | $\mu A$    | All outputs off                                  |
|  | $I_{DD}$                   | —            | —    | 100  | $\mu A$    | $V_{DD} = 5V$ , all outputs off,<br>inputs = 0V  |
|  |                            | —            | —    | 200  | $\mu A$    | $V_{DD} = 12V$ , all outputs off,<br>inputs = 0V |
|  |                            | —            | —    | 1.0  | mA         | $V_{DD} = 5V$ , one output on,<br>inputs = 0V    |
| —  | —                          | 3.0          | mA   | $V_{DD} = 12V$ , one output on,<br>inputs = 0V |            |  |
| Diode Leakage Current  | $I_H$                      | —            | —    | 50   | $\mu A$    | $T_A = +25^\circ C$ ; Max. $V_{BB}$              |
|  |                            | —            | —    | 100  | $\mu A$    | $T_A = +85^\circ C$ ; Max. $V_{BB}$              |
| Diode Forward Voltage  | $V_F$                      | —            | —    | 2.0  | V          | $I_F = 350$ mA; $V_{BB}$ open                    |

**Note 1:** Specification for packaged product only.

**2:** Positive (negative) current is defined as going into (coming out of) the specified device pin.

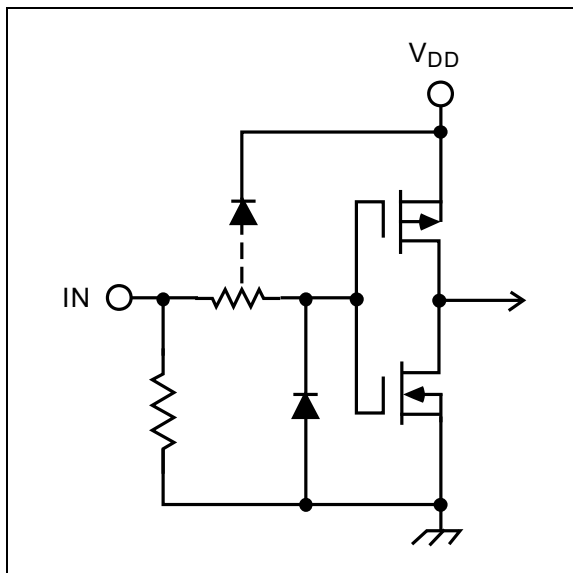
**3:** Operation of these devices with standard TTL may require the use of appropriate pull-up resistors.

## TEMPERATURE SPECIFICATIONS

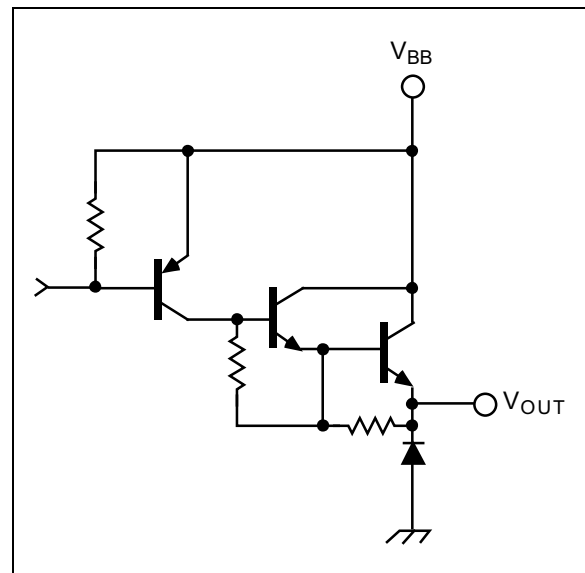
| Parameters                  | Sym.  | Min. | Typ. | Max. | Units | Conditions |
|-----------------------------|-------|------|------|------|-------|------------|
| <b>Temperature Ranges</b>   |       |      |      |      |       |            |
| Operating Temperature Range | $T_A$ | -40  | —    | +85  | °C    | Note 1     |
| Storage Temperature Range   | $T_S$ | -65  | —    | +150 | °C    | —          |

**Note 1:** The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e.,  $T_A$ ,  $T_J$ ,  $\theta_{JA}$ ). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

## Typical Circuits



**FIGURE 1-1:** Typical Input Circuit

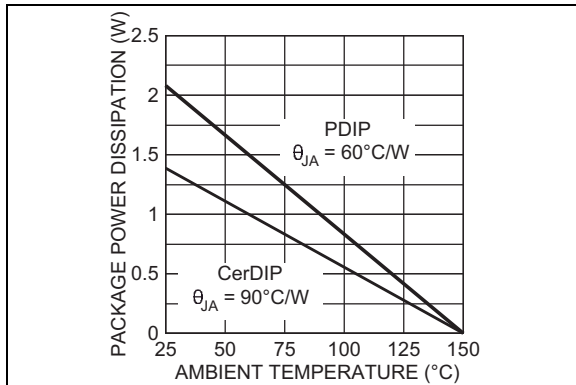


**FIGURE 1-2:** Typical Output Circuit.

# MIC5891

## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

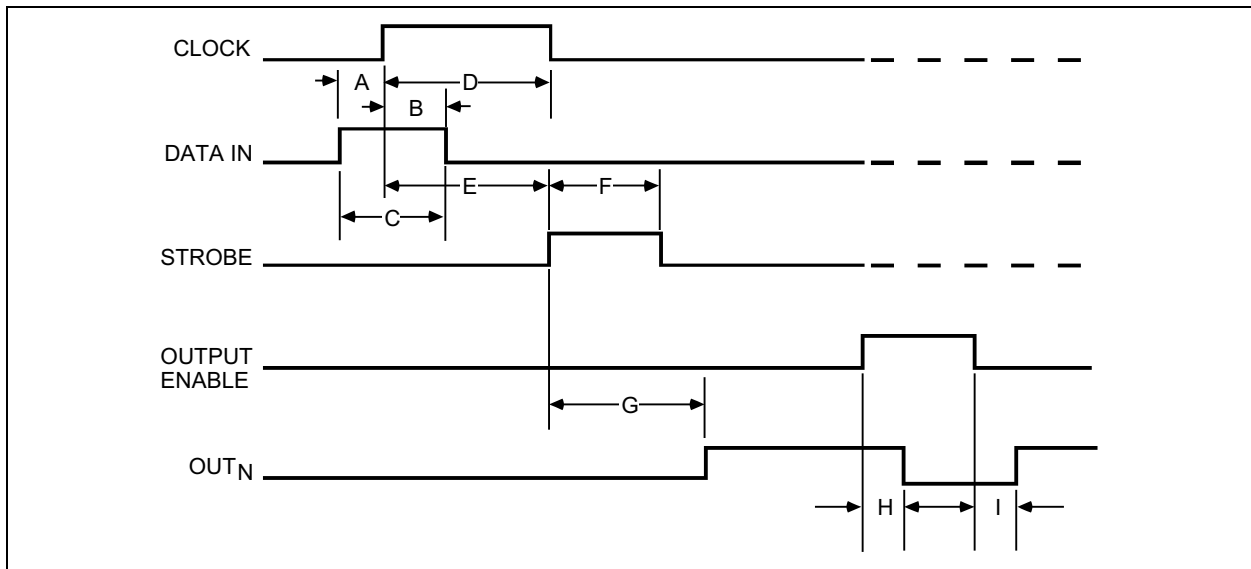


**FIGURE 2-1:** Allowable Package Power Dissipation vs. Temperature.



## 3.0 TIMING CONDITIONS

The descriptions of the timing conditions are listed below [Figure 3-1](#).



**FIGURE 3-1:** Timing Conditions.

**TABLE 3-1: TIMING CONDITIONS PARAMETERS**

| V <sub>DD</sub> = 5.0V, Logic levels are V <sub>DD</sub> and ground. |  |  |
|--|--|--|
| Reference  | Parameter  | Value  |
| A  | Minimum data active time before clock pulse (data set-up time) | 75 ns  |
| B  | Minimum data active time after clock pulse (data hold time)    | 75 ns  |
| C  | Minimum data pulse width                                       | 150 ns   |
| D  | Minimum clock pulse width                                      | 150 ns   |
| E  | Minimum time between clock activation and strobe               | 300 ns   |
| F  | Minimum strobe pulse width                                     | 100 ns   |
| G  | Typical time between strobe activation and output transition   | 1.0 μs   |
| H  | Turn-off delay   | See <a href="#">Electrical Characteristics</a> |
| I  | Turn-on delay  | See <a href="#">Electrical Characteristics</a> |

**TABLE 3-2: TRUTH TABLE**

| Serial Data Input | Clock Input | Shift Register Contents  | Serial Data Output | Strobe Input | Latch Contents   | Output Enable | Output Content   |
|-------------------|-------------|--|--------------------|--------------|--|---------------|--|
|                   |             | I <sub>1</sub> I <sub>2</sub> I <sub>3</sub> ... I <sub>N-1</sub> I <sub>N</sub> |                    |              | I <sub>1</sub> I <sub>2</sub> I <sub>3</sub> ... I <sub>N-1</sub> I <sub>N</sub> |               | I <sub>1</sub> I <sub>2</sub> I <sub>3</sub> ... I <sub>N-1</sub> I <sub>N</sub> |
| H                 |             | H R <sub>1</sub> R <sub>2</sub> ... R <sub>N-2</sub> R <sub>N-1</sub>            | R <sub>N-1</sub>   | —            | —  | —             | —  |
| L                 |             | L R <sub>1</sub> R <sub>2</sub> ... R <sub>N-2</sub> R <sub>N-1</sub>            | R <sub>N-1</sub>   |              |  |               |  |
| X                 |             | R <sub>1</sub> R <sub>2</sub> R <sub>3</sub> ... R <sub>N-1</sub> R <sub>N</sub> | R <sub>N</sub>     |              |  |               |  |
| —                 | —           | X X X ... X X  | X                  | L            | R <sub>1</sub> R <sub>2</sub> R <sub>3</sub> ... R <sub>N-1</sub> R <sub>N</sub> | L             | P <sub>1</sub> P <sub>2</sub> P <sub>3</sub> ... P <sub>N-1</sub> P <sub>N</sub> |
|                   |             | P <sub>1</sub> P <sub>2</sub> P <sub>3</sub> ... P <sub>N-1</sub> P <sub>N</sub> | P <sub>N</sub>     | H            | P <sub>1</sub> P <sub>2</sub> P <sub>3</sub> ... P <sub>N-1</sub> P <sub>N</sub> |               |  |
|                   |             | —  | —                  | —            | X X X ... X X  |               |  |

L = Low Logic Level, H = High Logic Level, X = Irrelevant, P = Present State, R = Previous State.

## 4.0 APPLICATION INFORMATION

Serial data present at the input is transferred into the shift register on the rising edge of the CLOCK input pulse. Additional CLOCK pulses shift data information towards the SERIAL DATA OUTPUT. The serial data must appear at the input prior to the rising edge of the CLOCK input waveform.

The 8 bits present in the shift register are transferred to the respective latches when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Most applications where the latching feature is not used (STROBE tied high) require the OUTPUT ENABLE input to be high during serial data entry.

Outputs are active (controlled by the latch state) when the OUTPUT ENABLE is low. All outputs are low (disabled) when the OUTPUT ENABLE is high. OUTPUT ENABLE does not affect the data in the shift register or latch.

## 5.0 PACKAGING INFORMATION

### 5.1 Package Marking Information

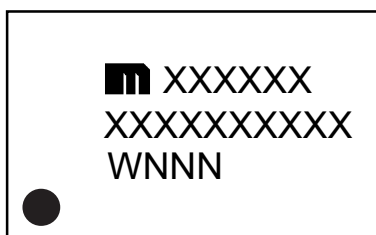
16-Pin PDIP\*



Example



16-Pin SOICW\*



Example

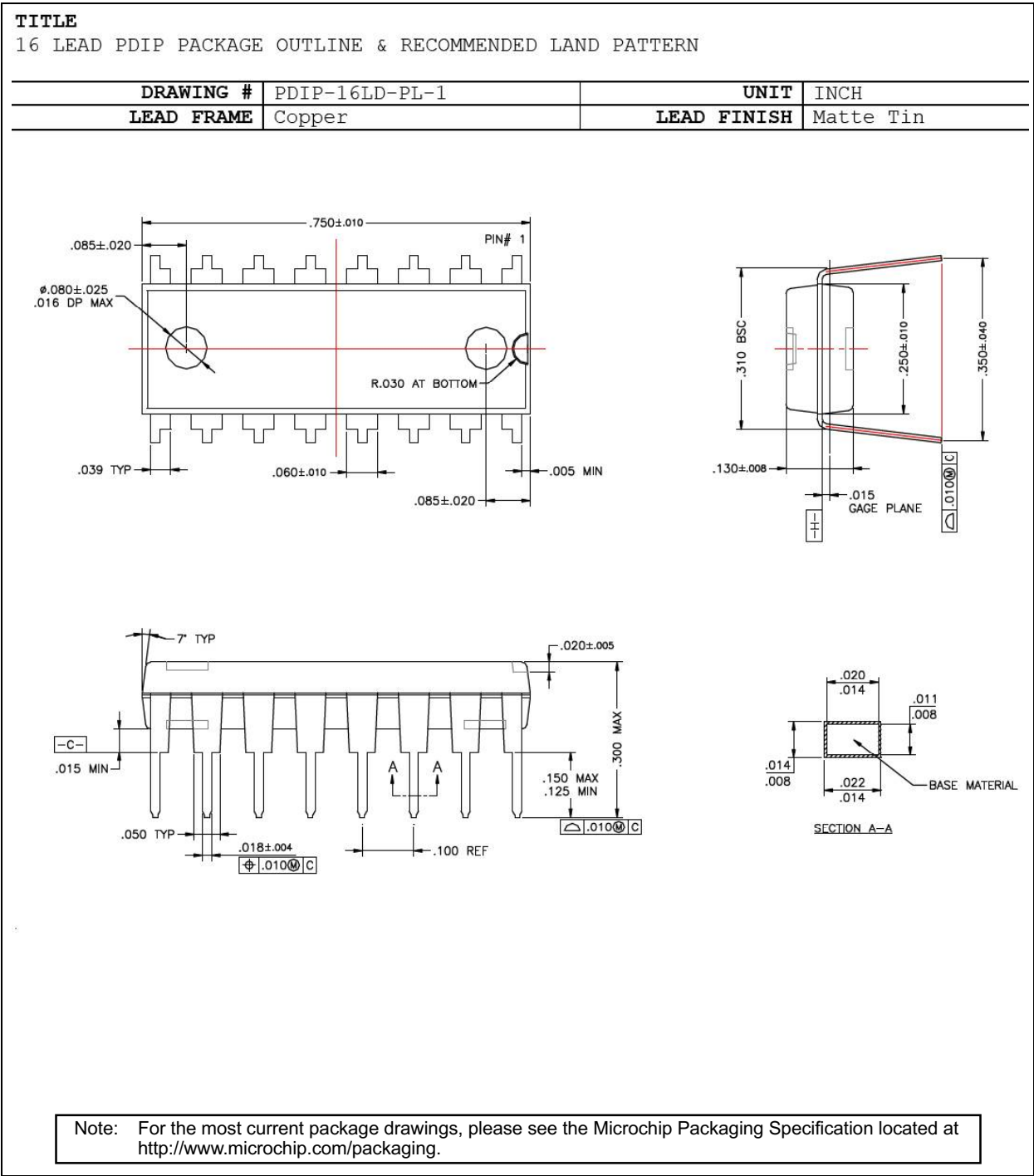


|                |  |  |
|----------------|--|--|
| <b>Legend:</b> | XX...X   | Product code or customer-specific information  |
|                | Y  | Year code (last digit of calendar year)  |
|                | YY   | Year code (last 2 digits of calendar year)   |
|                | WW   | Week code (week of January 1 is week '01')   |
|                | NNN  | Alphanumeric traceability code   |
|                | (e3)   | Pb-free JEDEC® designator for Matte Tin (Sn)   |
|                | *  | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |
|                | •, ▲, ▼  | Pin one index is identified by a dot, delta up, or delta down (triangle mark).                                     |
| <b>Note:</b>   | In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo. |  |
|                | Underbar ( _ ) and/or Overbar ( ¯ ) symbol may not be to scale.  |  |

**Note:** If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:  
 6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;  
 2 Characters = NN; 1 Character = N

# MIC5891

## 16-Lead PDIP Package Outline and Recommended Land Pattern



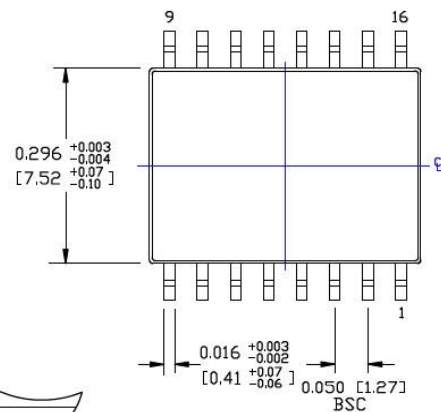
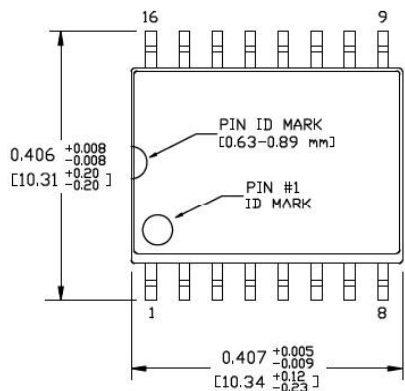
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

## 16-Lead SOICW Package Outline and Recommended Land Pattern

**TITLE**

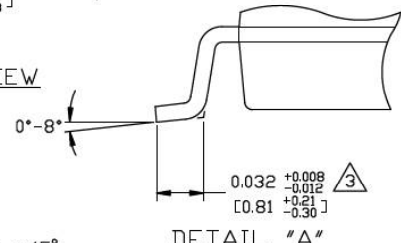
16 LEAD SOICW PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

| DRAWING # | SOICW-16LD-PL-1 | UNIT | INCH [MM] |
|-----------|-----------------|------|-----------|
|-----------|-----------------|------|-----------|

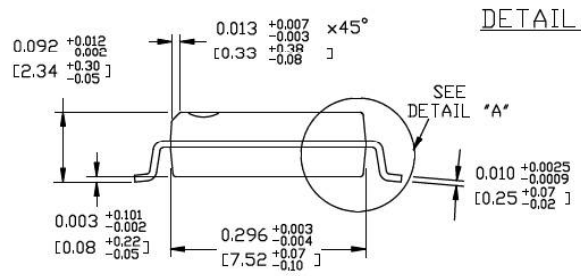


TOP VIEW  
NOTE 1, 2

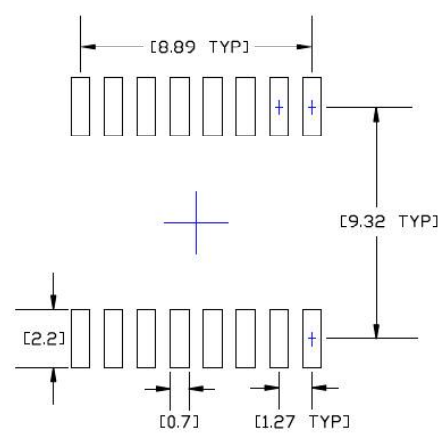
BOTTOM VIEW  
NOTE 1, 2



DETAIL "A"



END VIEW  
NOTE 1, 2, 3



RECOMMENDED LAND PATTERN

**NOTES:**

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.15] PER SIDE.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

## APPENDIX A: REVISION HISTORY

### Revision A (October 2016)

- Converted Micrel document MIC5891 to Microchip data sheet DS20005638B.
- Minor text changes throughout.
- Operating temperature range corrected in the [Temperature Specifications](#) section.
- Maximum Saturation Voltage values updated in [Table](#) .
- First Input Current maximum value updated in [Table](#) .

### Revision B (February 2022)

- Corrected the device marking specification in [Section 5.1, Package Marking Information](#).

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

| <u>PART NO.</u>             |                            | X  | XX         | - | XX |
|-----------------------------|----------------------------|--|------------|---|----|
| Device                      | Junction Temperature Range | Package                                  | Media Type |   |    |
| Device:                     | MIC5891:                   | 8-Bit Serial-Input Latched Source Driver |            |   |    |
| Junction Temperature Range: | Y =                        | -40°C to +85°C                           |            |   |    |
| Package:                    | N =                        | 16-Lead PDIP                             |            |   |    |
|                             | WM =                       | 16-Lead SOICW                            |            |   |    |
| Media Type:                 | TR =                       | 1,000/Reel for WM Package                |            |   |    |
|                             | (blank)=                   | 25/Tube for N Package                    |            |   |    |
|                             | (blank)=                   | 47/Tube for WM Package                   |            |   |    |

### Examples:

- a) MIC5891YN: 8-Bit Serial-Input Latched Source Driver, -40°C to +85°C Junction Temperature Range, 16-Lead PDIP, 25/Tube
- a) MIC5891YWM: 8-Bit Serial-Input Latched Source Driver, -40°C to +85°C Junction Temperature Range, 16-Lead SOICW, 47/Tube
- a) MIC5891YWM-TR: 8-Bit Serial-Input Latched Source Driver, -40°C to +85°C Junction Temperature Range, 16-Lead SOICW, 1,000/Reel

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