



Product Change Notification / SYST-28XOIJ180

Date:

02-Feb-2022

Product Category:

16-Bit - Microcontrollers and Digital Signal Controllers

PCN Type:

Document Change

Notification Subject:

ERRATA - dsPIC33CK512MP608 Family Silicon Errata and Data Sheet Clarification Document Revision

Affected CPNs:

[SYST-28XOIJ180_Affected_CPN_02022022.pdf](#)

[SYST-28XOIJ180_Affected_CPN_02022022.csv](#)

Notification Text:

SYST-28XOIJ180

Microchip has released a new Product Documents for the dsPIC33CK512MP608 Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at [dsPIC33CK512MP608 Family Silicon Errata and Data Sheet Clarification](#).

Notification Status: Final

Description of Change:

1) Updated data sheet references to current revision C.

Impacts to Data Sheet: None

Reason for Change: To Improve Manufacturability

Change Implementation Status: Complete

Date Document Changes Effective: 2 Feb 2022

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

[dsPIC33CK512MP608 Family Silicon Errata and Data Sheet Clarification](#)

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Affected Catalog Part Numbers (CPN)

DSPIC33CK256MP305-E/M7
DSPIC33CK256MP305-E/PT
DSPIC33CK256MP305-H/M7
DSPIC33CK256MP305-H/PT
DSPIC33CK256MP305-I/M7
DSPIC33CK256MP305-I/PT
DSPIC33CK256MP305T-E/M7
DSPIC33CK256MP305T-E/PT
DSPIC33CK256MP305T-I/M7
DSPIC33CK256MP305T-I/PT
DSPIC33CK256MP306-E/MR
DSPIC33CK256MP306-E/PT
DSPIC33CK256MP306-H/MR
DSPIC33CK256MP306-H/PT
DSPIC33CK256MP306-I/MR
DSPIC33CK256MP306-I/PT
DSPIC33CK256MP306T-E/MR
DSPIC33CK256MP306T-E/PT
DSPIC33CK256MP306T-I/MR
DSPIC33CK256MP306T-I/PT
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dsPIC33CK512MP608 Family Silicon Errata and Data Sheet Clarification

The dsPIC33CK512MP608 family devices that you have received conform functionally to the current Device Data Sheet (DS70005452C), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in [Table 1](#). The silicon issues are summarized in [Table 2](#).


The errata described in this document will be addressed in future revisions of the dsPIC33CK512MP608 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of [Table 2](#) apply to the current silicon revision (**A0**).

Data Sheet clarifications and corrections start on [page 5](#), following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
 - a) For MPLAB IDE 8, select *Programmer > Reconnect*.
 - b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ().
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various dsPIC33CK512MP608 silicon revisions are shown in [Table 1](#).

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID ⁽¹⁾	Revision ID for Silicon Revision	Number	Device ID ⁽¹⁾	Revision ID for Silicon Revision
		A0			A0
dsPIC33CK512MP608	0x9F54	0x0001	dsPIC33CK512MP308	0x9F14	0x0001
dsPIC33CK512MP606	0x9F53		dsPIC33CK512MP306	0x9F13	
dsPIC33CK512MP605	0x9F52		dsPIC33CK512MP305	0x9F12	
dsPIC33CK256MP608	0x9F44		dsPIC33CK256MP308	0x9F04	
dsPIC33CK256MP606	0x9F43		dsPIC33CK256MP306	0x9F03	
dsPIC33CK256MP605	0x9F42		dsPIC33CK256MP305	0x9F02	

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

dsPIC33CK512MP608

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions ⁽¹⁾
				A0
I ² C	Idle	1.	Address cannot be received in Idle mode.	X
CPU	DIV.SD Instruction	2.	Overflow bit is not getting set when an overflow occurs.	X
PWM	Time Base Capture	3.	PWM Capture Status (CAP) flag will not set again under certain conditions.	X
MCCP	Timer Interrupt	4.	Timer interrupt not working in Capture mode.	X
I ² C	Collision Detection	5.	Bus collision is not detected during Host reception if there is a Start/Stop condition.	X
I ² C	Client Mode	6.	Unexpected Client interrupt if there is a Stop bit in the 9th clock, followed by a Start bit.	X
I ² C	Client Mode	7.	When data hold is enabled and software sends a NACK, a Client interrupt is asserted if there are more bytes on the bus.	X
ADC	Differential-Mode	8.	Errors may occur when enabling Differential-mode when F _{SRC} is greater than 50 MHz.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A0**).

1. Module: I²C

In Client mode, an address cannot be received when the device is in Idle and the module is set for discontinue in Idle (I2CSIDL = 1).

Work around

None.

Affected Silicon Revisions

A0								
X								

2. Module: CPU

When using the Signed 32/16-bit Division instruction, DIV.SD, the Overflow bit may not always get set when an overflow occurs.

Work around

Test for, and handle, overflow conditions outside of the DIV.SD instruction.

Affected Silicon Revisions

A0								
X								

3. Module: PWM

When using a PWM Control Input (PCI) to trigger a time base capture, the Capture Status flag, CAP (PGxSTAT[5]), may not set again under certain conditions. When a subsequent PWM capture event occurs while, or just after, reading the current capture value from the PGxCAP register, the Capture Status flag, CAP, will not set again.

Work around

Read the PWM Generator Capture (PGxCAP, x = 1 to 8) register at a known time to avoid the condition. The timing of the PGxCAP read operation can be scheduled by using the PWM Generator x (1-8) interrupt or any of the six PWM Event (A-F) interrupts corresponding to the PCI event, which triggered the time base capture. Read the PGxCAP value after the CAP bit has set within the interrupt.

Affected Silicon Revisions

A0								
X								

4. Module: MCCP

The CCP Timer Interrupt, _CCTxInterrupt, may not occur in Capture mode (CCSEL = 1) with the timer time base prescale set to anything other than zero (TMRPS[1:0] ≠ 0).

Work around

None.

Affected Silicon Revisions

A0								
X								

dsPIC33CK512MP608

5. Module: I²C

Bus collision detection can fail during a Start/Stop condition when a Host is receiving data from a Client. This condition can occur in a noisy environment or hot swapping I²C.

Work around

None.

Affected Silicon Revisions

A0							
X							

6. Module: I²C

An unexpected Client interrupt will occur if the Host sends a NACK and a Stop bit, followed by a Start bit in the ACK phase (9th clock) during Client transmit.

Work around

Software should ignore the Client interrupt that is asserted after sending a NACK.

Affected Silicon Revisions

A0							
X							

7. Module: I²C

In Client mode with DHEN = 1 (Data Hold Enable), if software sends a NACK, the Client interrupt is asserted if there are any bytes on the bus.

Work around

Software should ignore the Client interrupt that is asserted after sending a NACK.

Affected Silicon Revisions

A0							
X							

8. Module: ADC

When operating ADC with an Input Frequency (F_{SRC}) above 50 MHz, conversion errors may occur when enabling Differential-mode (DIFFx = 1).

Work around

During initialization of the ADC to write the ADMODxL/H registers, use a slower input frequency of 50 MHz or less. After completion of the 1st conversion of each channel in Differential-mode, Input Frequency, F_{SRC}, can be increased to the maximum specified in the “**Electrical Characteristics**”.

Affected Silicon Revisions

A0							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70005452C):

<p>Note: Corrections are shown in bold. Where possible, the original bold text formatting has been removed for clarity.</p>

None.

dsPIC33CK512MP608

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (7/2021)

Initial version of this document; issued for revision A0.

Rev B Document (1/2022)

Updated data sheet references to current revision C.

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ISBN: 978-1-5224-9712-7



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