Information note

N° 10305AERRA

Dear customer,

With this Infineon Technologies AG information note, we would like to inform you about the following

Errata Advance Information 2021-12 affecting TC3xx Microcontrollers

On 16 April 2020, Infineon acquired Cypress.
We are now in the process of merging and consolidating our tools and processes for PCN, Information Notes, Errata and Product Discontinuance.
For further details, please visit our website:
https://www.infineon.com/cms/en/about-infineon/company/cypress-acquisition/

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Information note

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▶ **Products affected**	Please refer to attached affected product list 1_cip10305

▶ **Detailed change information**

Subject	Errata Advance Information: New/updated errata/ApHint text modules - Advance information 2021-12 for TC3xx Microcontrollers
Reason	Functional Problems, Application Hints, Documentation Updates

Description

Old	New
■ Not applicable (initial version)	■ Errata Advance Information TC3xx_Errata_Advance_Info_2021_12_v1_0_10305AERRA

▶ **Product identification**	Not applicable (no change of product)
▶ **Impact of change**	Assessment in Application required !
▶ **Attachments**	1_cip10305 affected product list 3_cip10305 TC3xx_Errata_Advance_Info_2021_12
▶ **Intended start of delivery**	Not applicable

If you have any questions, please do not hesitate to contact your local sales office.

Rel. 1.0, 2021-12-22

Device TC3xx

Marking/Step see Table 1

10305AERRA

Infineon is providing you with product information not previously addressed in the product data sheets or other documentation for the devices listed above. The enclosed information describes device behavior which may affect your current or prior use of the product. As our customers use these products in a number of different applications, Infineon is not in a position to assess the consequences of this device behavior in your specific application(s). Therefore, you should review the enclosed information and evaluate its effect, if any, on your current or prior use of the product in your application(s), including whether there are any safety concerns requiring further action and/or regulatory reporting.

New/updated errata/ApHint text modules - Advance information 2021-12

The following text modules have been compiled and internally reviewed by the Microcontroller Division of Infineon Technologies after the latest TC3xx errata sheet release cycle (2021-11-04). They are provided here as advance information, and shall be integrated into the TC3xx errata sheets in the next quarterly release cycle.

Table 1 New/updated TC3xx errata/ApHint text modules - 2021-12

Text module	Short description	Affected devices	Change	Page
ASCLIN_TC.012	Recover sequence after timeout in LIN master mode	All TC3xx	New	3
ASCLIN_TC.H006	Sample point position when using three samples per bit - Documentation update	All TC3xx	New	3
CCU_TC.005	ASC and CAN bootstrap loaders may not work if external clock is missing	All TC3xx	New	4

Table 1 New/updated TC3xx errata/ApHint text modules - 2021-12

Text module	Short description	Affected devices	Change	Page
GTM_AI.398	DPLL: Incorrect DPLL_THVAL calculation leading to a false direction decision in case tbu_ts0 wraps around	TC39x ..TC36x, TC3Ex[1)]	New	5
GTM_AI.400	MCS-RTL: Division instruction may produce unexpected memory overflow and wrong results	TC39x ..TC36x, TC3Ex[1)]	New	5
GTM_TC.025	Register DPLL_IRQ_NOTIFY - Documentation update for bits SORI and DCGI	TC39x ..TC36x, TC3Ex[1)]	New	6
GTM_TC.H026	Assignment of TOUTSEL Registers to TOUTy Outputs - Documentation correction to TC33x/TC32x Appendix	TC33x/32x	New	7
GTM_TC.H027	Register ODA (OCDS Debug Access) - Documentation update	TC3xx with GTM	New	7
I2C_TC.H009	Connections of Serial Clock Inputs	TC3xx with I2C[2)]	New	8
PMS_TC.016	VEXTMON - Update to table 3-31 of TC36x AA-Step Data Sheet V1.1	TC36x	New	8
PMS_TC.H011	Supply mode and topology selection - Allowed combinations of VEXT and VDDM - Documentation update	All TC3xx	New	9
SAFETY_TC.H019	SM[HW]:NVM.FSIRAM:REG_MONITOR_TEST should not be considered	All TC3xx	New	10
SAFETY_TC.H020	Test of SM[HW]:VMT:REG_MONITOR is missing - Documentation update	All TC3xx	New	10
SCR_TC.024	Field ADRES in register ADCOMP_RES - Documentation correction	All TC3xx	New	10
SCU_TC.033	TESTMODE pin shall be held at static level during LBIST	All TC3xx	New	11

1) TC3xx with GTM, except TC33x/32x (does not have DPLL and MCS)

2) TC39x..TC35x, TC3Ex (no I2C in TC33xEXT, TC33x/32x)

ASCLIN_TC.012 Recover sequence after timeout in LIN master mode

Due to an internal state machine problem, unexpected behavior will occur in the scenario described below.

Expected behavior

In the LIN master mode, the LIN state machine is supposed to abort its current processing and return to idle state when a header or response timeout occurs.

Observed behavior

If a timeout error occurred, no further LIN frames are transmitted.

Exception

In rare cases, when the timeout error occurs in the LIN state machine at the same time as a soft suspend request to the ASCLIN module, the LIN state machine returns to idle state and the recover sequence is as described in the User's Manual.

Workaround

After a header or response timeout has been detected, set field FRAMECON.MODE to INIT (00_B) and then to LIN mode (11_B), as described in section "Abort sequence" in the ASCLIN chapter of the User's Manual.

ASCLIN_TC.H006 Sample point position when using three samples per bit - Documentation update

As documented in the description of field BITCON.SAMPLEPOINT, "... if three sample points at position 7, 8, 9 are required, this bit field would contain 9".

In general, if three samples per bit are selected (BITCON.SM = 1_B), field BITCON.SAMPLEPOINT defines the position of the last sample point.

Documentation update

The text related to three sample points in figure “ASCLIN Bit Structure” in the ASCLIN chapter of the User’s Manual should be updated as follows:

- 16x Oversampling, 3 sample points, relevant sample position 7, 8, 9
  - instead of “16x Oversampling, 3 sample points, relevant sample position 8”
- 8x Oversampling, 3 sample points, relevant sample position 3, 4, 5
  - instead of “8x Oversampling, 3 sample points, relevant sample position 4”

CCU_TC.005 ASC and CAN bootstrap loaders may not work if external clock is missing

Description

When using the ASC or CAN bootstrap loader (BSL) with internal clocking (f_{BACK}), and no supply noise or other source of signal level transition is present on the XTAL1 input during device power-up, the device does not respond to the zero byte (ASC BSL) or initialization frame (CAN BSL).

Effects

No code download for initial device programming is started.

Note: This problem may only occur for initial start up of unprogrammed devices. If automatic start of the external crystal oscillation is programed in UCB DFLASH, the problem will not occur.

Workaround

Trigger reset and retry if bootstrap loader does not respond.

If connection to the device is possible via a debug tool, use the tool to reconfigure OSCCON.MODE = 00_B (when using an external crystal), and then trigger reset.

GTM_AI.398 DPLL: Incorrect DPLL_THVAL calculation leading to a false direction decision in case tbu_ts0 wraps around

When

- a) the inactive edge of TRIGGER input signal is used for detection of the direction (DPLL_CTRL_1.IDDS=1)

and

- b) the input delay information is used to correct time stamps (DPLL_CTRL_0.IDT=1)

and

- c) in between the active input signal edge and the inactive input signal edge on TRIGGER tbu_ts0 wraps around,

then the calculation of DPLL_THVAL.THVAL is incorrect incurring a false direction decision.

Scope

DPLL

Effects

Wrong value of DPLL_THVAL and false direction decision.

Workaround

Don't use DPLL_CTRL_0.IDT=1 when evaluating direction with DPLL_CTRL_1.IDDS=1.

GTM_AI.400 MCS-RTL: Division instruction may produce unexpected memory overflow and wrong results

Assume that a division instruction (DIVU or DIVS) is located in the MCS memory within the address range [MP1-4*6, ..., MP1-4]. If this instruction is executed with an Accelerated Scheduling mode or a Prioritized Scheduling mode the associated MCS channel potentially stops its execution and

signalizes a memory overflow. In this case the calculated results of the instruction are wrong.

Scope

MCS

Effects

An MCS channel stops with a memory overflow error and the calculated results of the division instruction are wrong.

Workaround

Re-order program sequence in a way that any division instruction is located outside the critical address range [MP1-4*6, ..., MP1-4] of the MCS memory.

GTM_TC.025 Register DPLL_IRQ_NOTIFY - Documentation update for bits SORI and DCGI

In the description of field SORI (State out of range interrupt) in register DPLL_IRQ_NOTIFY in the GTM chapter of the TC3xx User's Manual, the sentence "The interrupt occurs at line number 0" is incorrect.

Documentation update

In the description of register DPLL_IRQ_NOTIFY, the sentence "The interrupt occurs at line number 0" shall be moved from bit SORI to bit DCGI, as shown below.

Table 2 Register DPLL_IRQ_NOTIFY - Documentation update for bits SORI and DCGI

Field	Bits	Type	Description
SORI	26	rw	**STATE out of range** ~~The interrupt occurs at line number 0.~~
DCGI	27	rw	**Direction change interrupt** The interrupt occurs at line number 0.

The rest of the description for register DPLL_IRQ_NOTIFY remains unchanged.

Note: The assignment of DPLL interrupts to interrupt line numbers DPLL_IRQ[n] is correctly described in table "ICM Interrupt Signals" in the GTM chapter of the TC3xx User's Manual. According to this table, SORI is assigned to DPLL_IRQ[26].

GTM_TC.H026 Assignment of TOUTSEL Registers to TOUTy Outputs - Documentation correction to TC33x/TC32x Appendix

Note: This problem only affects TC33x/TC32x Appendix versions before V2.0.0. It has been corrected in V2.0.0.

The description in table "Assignment of TOUTSEL Registers to TOUTy Outputs" of the product specific TC33x/TC32x Appendix with respect to register TOUTSEL4 is partly incorrect: the connections TOUT35..TOUT37 in columns SEL3..SEL5 are not available.

Documentation correction

The corrected row for register TOUTSEL4 is shown in the following table.

Table 3 Assignment of TOUTSEL Registers to TOUTy Outputs - Correction for register TOUTSEL4

Register	SEL7	SEL6	SEL5	SEL4	SEL3	SEL2	SEL1	SEL0
TOUTSEL4	-	-	-	-	-	TOUT34 1)	TOUT33 1)	TOUT32

1) Not available in TQFP100/TQFP80 packages

GTM_TC.H027 Register ODA (OCDS Debug Access) - Documentation update

In the GTM chapter of the TC3xx User's Manual, the following note is located below the description of register ODA in section "OCDS Debug Access Register":

- 6. TIM[i]_CH[x]_GPR0/1: Reading these register will reset the ECNT counter.

Documentation update

Note 6. (see above) does not apply and shall be deleted.

I2C_TC.H009 Connections of Serial Clock Inputs

In tables “Connections of I2C0” and “Connections of I2C1” (for TC39x, TC38x TC3Ex only) in the respective product specific appendix to the TC3xx User’s Manual, only the serial clock output connections are shown. The serial clock input connections (located on the same port pins) are not shown.

Recommendation

See the corresponding TC3xy Data Sheet for the available I2C serial clock input connections (I2C0:SCLA/SCLB/SCLC, I2C1:SCLA/SCLB) on the respective port pins.

PMS_TC.016 VEXTMON - Update to table 3-31 of TC36x AA-Step Data Sheet V1.1

In table 3-31 (Supply Monitors) of TC36x AA-Step Data Sheet V1.1, the rows for the 5.0V (Typ.) values of V_{EXTMON} (VEXT, VDDM & VEVRSB secondary supply monitor accuracy after trimming) are corrupted by a page break.

Documentation update

The complete description of the rows for the 5.0V (Typ.) values of V_{EXTMON} is shown in the following table (see also TC36x AA-Step Data Sheet V1.0).

Table 4 Update to table 3-31 of TC36x AA-Step Data Sheet V1.1

Parameter	Symbol	Values			Unit	Note/Test Conditions
		Min.	Typ.	Max.		
V_{EXT}, V_{DDM} & V_{EVRSB} secondary supply monitor accuracy after trimming	V_{EXTMON}	4.9	5.0	5.1	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=5V=D9h(UV) / DAh(OV). For BGA packages: EVRMONFILT.SWDFIL=1
		4.9	5.0	5.1		SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=5V=D9h(UV) / DAh(OV). For QFP packages: EVRMONFILT.SWDFIL=2

PMS_TC.H011 Supply mode and topology selection - Allowed combinations of VEXT and VDDM - Documentation update

Tables “Allowed Combinations of Nominal External Supply Voltages between Voltage Rails” in the PMS and PMSLE chapters of the TC3xx User’s Manual define the allowed combinations of the external supply voltages for the target applications and verified use cases of the TC3xx family.

These tables do not include the combination VEXT = 5V and VDDM = 3.3V.

Documentation update

For consistency, in tables “Supply Mode and Topology selection” in the same chapters, for the configurations with “VEXT & VEVRSB = **5.0V** external supply” in column “Supply Pin Voltage/Level”, the term “VDDM = VAREFx = 5V **or 3.3V**” shall be replaced by

- VDDM = VAREFx = 5V

SAFETY_TC.H019 SM[HW]:NVM.FSIRAM:REG_MONITOR_TEST should not be considered

The SM[HW]:NVM.FSIRAM:REG_MONITOR_TEST is defined in the AURIX TC3xx Safety Manual as a self-test mechanism for the FSI.RAM SFFs.

Recommendation

The system integrator has to consider the FSI.RAM SFFs as not testable, as in fact there are no means to trigger this test.

Note: SM[HW]:NVM.FSIRAM:REG_MONITOR_TEST is not part of the FMEDA and will not impact the FIT rate.

SAFETY_TC.H020 Test of SM[HW]:VMT:REG_MONITOR is missing - Documentation update

In the AURIX™ TC3xx Safety Manual, the “Tests” field of SM[HW]:VMT:REG_MONITOR (section 6.500 in Safety Manual v2.0) is empty. Users may think that the safety flip-flops mechanism is not testable, which is not true.

Documentation update

SM[HW]:VMT:REG_MONITOR is testable through SMU by ESM[SW]:SMU:REG_MONITOR_TEST.

SCR_TC.024 Field ADRES in register ADCOMP_RES - Documentation correction

In chapter “ADC Comparator Unit (ADCOMP)” of the SCR chapter in the TC3xx User’s Manual, erroneously the term “ADCRES” is used instead of “ADRES” in the text and in figure “ADC Comparator Overview”.

Documentation correction

The term “ADCRES” shall be replaced by “ADRES” within the text of chapter “ADC Comparator Unit (ADCOMP)”, and in figure “ADC Comparator Overview”.

In addition, the text in column “Description” for field ADRES in the ADCOMP Result Register ADCOMP_RES shall be corrected as follows:

Table 5 Field ADRES in register ADCOMP_RES - correction

Field	Bits	Type	Description
ADRES	7:0	rh	**ADC Conversion Result**
			This register shows the current converted ADC result. Software should ensure that the result is read before starting the next conversion. • For ADRES > 1: – VIN = [LSB * (ADRES-1)]; LSB = 23.077 mV. Full Range: 5861.54 mV. • For ADRES ≤ 1: software shall assume VIN as 0 V.

SCU_TC.033 $\overline{\text{TESTMODE}}$ pin shall be held at static level during LBIST

The MISR signatures documented in the product specific TC3xy Appendix to the TC3xx User’s Manual are only valid if the $\overline{\text{TESTMODE}}$ pin (P20.2) is always kept at a static **high** level during LBIST execution. This is the recommended LBIST configuration.

For a stable MISR signature, the level on this pin must not change during LBIST execution.

Workaround

For application environments where pin $\overline{\text{TESTMODE}}$ is not held high, but a static **low** level is applied to $\overline{\text{TESTMODE}}$, a different MISR signature will be received in the LBISTCTRL3.SIGNATURE field, depending on bit LBISTCTRL1.BODY.

Table 6 Contents of LBISTCTRL3 if $\overline{\text{TESTMODE}}$ is low during LBIST

Device	Design step	LIBISTCTRL3	
		BODY = 0	BODY = 1
TC39x	BA..BC	0x07EC4205	0xFEA614D6
	BD	0x935E836A	0x6A14D5B9
TC38x	AA..AD	0x1E1CD10C	0xA7587528
	AE	0x3AD1859B	0x839521BF
TC37xEXT	AA, AB	0x01E51F27	0xEDB9BD01
TC37x	AA	0x62DD6AB1	0xA373D89F
TC36x	AA	0xD833B421	0xF53338B3
TC35x	AB	0xBA38B3CB	0x1CACD3CE
TC33xEXT	AA	0xD1298927	0x1A824479
TC33x/TC32x	AA	0xC12B66CB	0x3F84CD94
TC3Ex	AA	0x4D0F493B	0xE7764C81

Information note N°10305AERRA

Errata Advance Information 2021-12 affecting TC3xx Microcontrollers

Sales name	SP number	OPN	Package
SAK-TC323LP-16F160F AA	SP001724344	TC323LP16F160FAAKXUMA1	PG-TQFP-100-23
SAK-TC323LP-24F200F AA	SP005408909	TC323LP24F200FAAKXUMA1	PG-TQFP-100-23
SAK-TC332LP-32F200F AA	SP004264616	TC332LP32F200FAAKXUMA1	PG-TQFP-80-7
SAK-TC332LP-32F300F AA	SP004974864	TC332LP32F300FAAKXUMA1	PG-TQFP-80-7
SAK-TC333LP-32F200F AA	SP001724318	TC333LP32F200FAAKXUMA1	PG-TQFP-100-23
SAK-TC333LP-32F300F AA	SP004974874	TC333LP32F300FAAKXUMA1	PG-TQFP-100-23
SAK-TC334LP-32F200F AA	SP001724294	TC334LP32F200FAAKXUMA1	PG-TQFP-144-27
SAK-TC334LP-32F300F AA	SP004974878	TC334LP32F300FAAKXUMA1	PG-TQFP-144-27
SAK-TC336LP-32F300S AA	SP004974908	TC336LP32F300SAAKXUMA1	PG-LFBGA-180-1
SAK-TC337DA-32F300S AA	SP004974938	TC337DA32F300SAAKXUMA1	PG-LFBGA-292-13
SAK-TC337DZ-32F200S AA	SP002268356	TC337DZ32F200SAAKXUMA1	PG-LFBGA-292-13
SAK-TC337LP-32F300S AA	SP004974944	TC337LP32F300SAAKXUMA1	PG-LFBGA-292-11
SAK-TC356TA-64F300S AB	SP003833202	TC356TA64F300SABKXUMA1	PG-LFBGA-180-1
SAK-TC356TD-48F300S AB	SP005424938	TC356TD48F300SABKXUMA1	PG-LFBGA-180-1
SAK-TC356TH-64F300S AB	SP004818890	TC356TH64F300SABKXUMA1	PG-LFBGA-180-1
SAK-TC357TA-64F300S AB	SP003803252	TC357TA64F300SABKXUMA1	PG-LFBGA-292-13
SAK-TC357TH-64F300S AB	SP003803258	TC357TH64F300SABKXUMA1	PG-LFBGA-292-13
SAK-TC364DP-48F300F AA	SP004577254	TC364DP48F300FAAKXUMA1	PG-TQFP-144-27
SAK-TC364DP-64F200F AA	SP005578089	TC364DP64F200FAAKXUMA1	PG-TQFP-144-27
SAK-TC364DP-64F300F AA	SP001713956	TC364DP64F300FAAKXUMA1	PG-TQFP-144-27
SAK-TC364DP-64F300W AA	SP001714740	TC364DP64F300WAAKXUMA1	PG-LQFP-144-25
SAK-TC365DP-64F200W AA	SP005351242	TC365DP64F200WAAKXUMA1	PG-LQFP-176-22
SAK-TC365DP-64F300W AA	SP001724126	TC365DP64F300WAAKXUMA1	PG-LQFP-176-22
SAK-TC367DP-64F300S AA	SP001694656	TC367DP64F300SAAKXUMA1	PG-LFBGA-292-11
SAK-TC367V0-64F300S AA	SP005411327	TC367V064F300SAAKXUMA1	PG-LFBGA-292-11
SAK-TC375TP-96F300W AA	SP001724106	TC375TP96F300WAAKXUMA1	PG-LQFP-176-22
SAK-TC377DP-96F300S AA	SP004987108	TC377DP96F300SAAKXUMA1	PG-LFBGA-292-11
SAK-TC377TP-96F300S AA	SP001694648	TC377TP96F300SAAKXUMA1	PG-LFBGA-292-11
SAK-TC377TX-96F300S AB	SP004950416	TC377TX96F300SABKXUMA1	PG-LFBGA-292-13
SAK-TC377VS-96F300S AA	SP005546304	TC377VS96F300SAAKXUMA1	PG-LFBGA-292-11
SAK-TC387QP-160F300S AD	SP002921224	TC387QP160F300SADKXUMA1	PG-LFBGA-292-11
SAK-TC387QP-160F300S AE	SP005351247	TC387QP160F300SAEKXUMA1	PG-LFBGA-292-11
SAK-TC387TP-128F300S AD	SP002921230	TC387TP128F300SADKXUMA1	PG-LFBGA-292-11
SAK-TC387TP-128F300S AE	SP005351248	TC387TP128F300SAEKXUMA1	PG-LFBGA-292-11
SAK-TC387TP-128F300S AE	SP005425390	TC387TP128F300SAEKXQMA1	PG-LFBGA-292-11
SAK-TC389QP-160F300S AD	SP002921222	TC389QP160F300SADKXUMA1	PG-FBGA-516-1
SAK-TC389QP-160F300S AE	SP005351252	TC389QP160F300SAEKXUMA1	PG-FBGA-516-1
SAK-TC397QA-160F300S BC	SP002739588	TC397QA160F300SBCKXUMA1	PG-LFBGA-292-12
SAK-TC397QA-160F300S BD	SP005351257	TC397QA160F300SBDKXUMA1	PG-LFBGA-292-12
SAK-TC397XA-256F300S BC	SP002739594	TC397XA256F300SBCKXUMA1	PG-LFBGA-292-12
SAK-TC397XA-256F300S BD	SP005351382	TC397XA256F300SBDKXUMA1	PG-LFBGA-292-12

Information note N°10305AERRA

Errata Advance Information 2021-12 affecting TC3xx Microcontrollers

Sales name	SP number	OPN	Package
SAK-TC397XP-256F300S BC	SP002739600	TC397XP256F300SBCKXUMA1	PG-LFBGA-292-10
SAK-TC397XP-256F300S BD	SP005351385	TC397XP256F300SBDKXUMA1	PG-LFBGA-292-10
SAK-TC397XP-256F300S BD	SP005433583	TC397XP256F300SBDKXQMA1	PG-LFBGA-292-10
SAK-TC397XX-256F300S BC	SP002725526	TC397XX256F300SBCKXUMA1	PG-LFBGA-292-10
SAK-TC397XX-256F300S BD	SP005351387	TC397XX256F300SBDKXUMA1	PG-LFBGA-292-10
SAK-TC399XP-256F300S BC	SP002725524	TC399XP256F300SBCKXUMA1	PG-LFBGA-516-10
SAK-TC399XP-256F300S BD	SP005351394	TC399XP256F300SBDKXUMA1	PG-LFBGA-516-10
SAK-TC399XX-256F300S BC	SP002725518	TC399XX256F300SBCKXUMA1	PG-LFBGA-516-10
SAK-TC399XX-256F300S BD	SP005351395	TC399XX256F300SBDKXUMA1	PG-LFBGA-516-10
SAK-TC3E7QF-192F300S AA	SP005345769	TC3E7QF192F300SAAKXUMA1	PG-LFBGA-292-11
SAK-TC3E7QG-160F300S AA	SP005345771	TC3E7QG160F300SAAKXUMA1	PG-LFBGA-292-11
SAL-TC333LP-32F200F AA	SP001724322	TC333LP32F200FAALXUMA1	PG-TQFP-100-23
SAL-TC364DP-64F300F AA	SP001724134	TC364DP64F300FAALXUMA1	PG-TQFP-144-27
SAL-TC367DP-64F300S AA	SP001724120	TC367DP64F300SAALXUMA1	PG-LFBGA-292-11
SAL-TC375TI-96F300W AA	SP005428963	TC375TI96F300WAALXUMA1	PG-LQFP-176-22
SAL-TC375TI-96F300W AA	SP005572121	TC375TI96F300WAALXUMA2	PG-LQFP-176-22
SAL-TC375TP-96F300W AA	SP001724110	TC375TP96F300WAALXUMA1	PG-LQFP-176-22
SAL-TC377DP-96F300S AA	SP004987116	TC377DP96F300SAALXUMA1	PG-LFBGA-292-11
SAL-TC377TP-96F300S AA	SP001724092	TC377TP96F300SAALXUMA1	PG-LFBGA-292-11
SAL-TC377TX-96F300S AB	SP004950414	TC377TX96F300SABLXUMA1	PG-LFBGA-292-13
SAL-TC387QP-160F300S AD	SP002921220	TC387QP160F300SADLXUMA1	PG-LFBGA-292-11
SAL-TC387QP-160F300S AE	SP005351250	TC387QP160F300SAELXUMA1	PG-LFBGA-292-11
SAL-TC387TP-128F300S AD	SP003021930	TC387TP128F300SADLXUMA1	PG-LFBGA-292-11
SAL-TC387TP-128F300S AE	SP005398494	TC387TP128F300SAELXUMA1	PG-LFBGA-292-11
SAL-TC389QP-160F300S AD	SP002921216	TC389QP160F300SADLXUMA1	PG-FBGA-516-1
SAL-TC389QP-160F300S AE	SP005351253	TC389QP160F300SAELXUMA1	PG-FBGA-516-1
SAL-TC397XP-256F300S BC	SP002725522	TC397XP256F300SBCLXUMA1	PG-LFBGA-292-10
SAL-TC397XP-256F300S BD	SP005351392	TC397XP256F300SBDLXUMA1	PG-LFBGA-292-10
SAL-TC399XP-256F300S BC	SP002725520	TC399XP256F300SBCLXUMA1	PG-LFBGA-516-10
SAL-TC399XP-256F300S BD	SP005351397	TC399XP256F300SBDLXUMA1	PG-LFBGA-516-10
SAL-TC399XX-256F300S BD	SP005351398	TC399XX256F300SBDLXUMA1	PG-LFBGA-516-10