Product Change Notification / SYST-26XAVG660

Date:

29-Oct-2021

Product Category:

PoE PSE

PCN Type:

Document Change

Notification Subject:

ERRATA - PD69104B1 Errata Sheet

Affected CPNs:

SYST-26XAVG660_Affected_CPN_10292021.pdf
SYST-26XAVG660_Affected_CPN_10292021.csv

Notification Text:

SYST-26XAVG660

Microchip has released a new Product Documents for the PD69104B1 Errata Sheet of devices. If you are using one of these devices please read the document located at PD69104B1 Errata Sheet.

Notification Status: Final

Description of Change: Initial Revision

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 29 Oct 2021

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

PD69104B1 Errata Sheet

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Affected Catalog Part Numbers (CPN)

PD69104B1FILQ-TR
PD69104B1ILQ-TR

PD69104

PD69104B1 and PD69104B1-F Errata

About this document

This document captures all the known erratas for PD69104B1 and PD69104B1-F device versions.

Table of Contents

1. Errata for PD69104B1 and PD69104B1-F Devices

This section lists the errata items and available solutions.

1.1 LED Behavior Due to Overload (OVL) or Short at Auto Mode

Description

The port LED stays **ON**, although ports are **OFF** due to disconnect. This scenario was detected at Auto Mode only. This behavior occurs:

- Sometimes when two ports are connected.
- Always when three or four ports are connected.

The sequence that causes the issue is:

1. OVL on all ports at the same time or Short on all ports at the same time.
2. Remove OVL or Short back to normal load on all ports at the same time, start-up, and then disconnect the ports in any order.
3. After disconnecting ports, some of the LEDs will stay ON although there is no load.

Workaround

Currently, there is no workaround for this issue.

1.2 LED Behavior Due to OVL or Short while Punishment at Auto Mode

Description

The port LED stays **ON**, although port is **OFF** due to disconnect. This scenario was detected at Auto Mode only. This behavior occurs always:

- OVL or Short on one port, then two seconds punishment timer starts and disables this port from starting up, which causes this issue.
- During this punishment time, disconnect the port.
- After disconnecting the port, the LED will stay ON; although there is no load.

Workaround

Currently, there is no workaround for this issue.

1.3 Host Communication

Description

- During UART communication, the PD69104B1 device writes zeros once the host starts to transmit the packet (starting from the first bit). The PD69104B1 device must wait until the host finishes the transmission and then starts to transmit another packet.

Workaround

The host must ignore any data containing 0 before receiving the header.

1.4 UART and I^2C Communications

For UART communications, operation of registers 0x2-0x3, 0x4-0x5, 0x6-0x7, 0x8-0x9, and 0xA-0xB is reversed from operation published in the PD69104B1 - Generic Registers Map.

For I^2C communication, operation is as described in the PD69104B1 - Generic Registers Map.

Registers Mapping and Description for UART Operation
Notes:
R/W Access Key:

- COR - Clear on Read. Register clears when read. Writing to these registers has no effect.
- R/W - Read/Write. Register can be read or written.
- RO - Read Only. Register can be read-only. Writing to these registers has no effect.
- SO - Set Only. Writing **1** - set the bit, Writing **0** – bit is unchanged (Data read from these registers has no effect).
- / - Bit (or Byte) default value – depends on IC I/O configuration (pull-up or pull-down).

Table 1-1. Registers Mapping and Description for UART Operation

Address (HEX)	Register Name	Width	Bits	Detailed Description	General/Equation	Reset Value (HEX)	Read/ Write
2	PWREVN_COR	8	[0:3]	Ports 1 to 4 power status change (occurs when a port is turned ON or OFF).	Power Event register. Identical to PWREVN register (03h), except that reading this register clears both power status and PWREVN_COR registers.	0	COR
			[4:7]	Ports 1 to 4 power good change (when power good status of the port changes).		0	COR
3	PWREVN	8	[0:3]	Ports 1 to 4 power status change (occurs when a port is turned ON or OFF).	Power Event register. Lower 4 bits indicate Power Enable events, which occur when a port is turned ON or OFF. Upper 4 bits are set when Power Good status of the applicable port(s) change. See STATPWR Register (10h) in the Register Map User Guide.	0	RO
			[4:7]	Ports 1 to 4 power good change (when power good status of the port changes).		0	RO
4	DETEVN_COR	8	[0:3]	Ports 1 to 4 detection cycle completed.	Detect and Classification Event register. Identical to DETEVN register (05h), except that reading this register clears both DETEVN and DETEVN_COR registers.	0	COR
			[4:7]	Ports 1 to 4 classifications completed.		0	COR
5	DETEVN	8	[0:3]	Ports 1 to 4 detection cycle completed.	Detection and Classification Event register. Lower 4 bits indicate that port has completed a detection cycle. upper 4 bits indicate port has completed classifying the PD. Detection's/Classification's results are available in ports' STATP register (0 Ch to 0 Fh). See Register Map User Guide.	0	RO
			[4:7]	Ports 1 to 4 classifications completed.			

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Address (HEX)	Register Name	Width	Bits	Detailed Description	General/Equation	Reset Value (HEX)	Read/ Write
6	FLTEVN_COR	8	[0:3]	Ports 1 to 4 over current time-out (t_{CUT}).	Overload and Underload Time Out register. Identical to FLTEVN Register (07h) except that reading this register clears both FLTEVN and FLTEVN_COR registers.	0	COR
			[4:7]	Ports 1 to 4 disconnect time-out (t_{DIS}).		0	COR
7	FLTEVN	8	[0:3]	Ports 1 to 4 over current time-out (t_{CUT}).	Overload and Underload Time Out register. Lower 4 bits indicate port is turned OFF because load current was above ICUT or ILIM lasted for longer than t_{CUT}. Upper 4 bits indicate when port is turned OFF because PD was disconnected.	0	RO
8	TSEVN_COR	8	[0:3]	Ports 1 to 4 over current during start-up time-out (t_{START}).	Overload during Start Up Time Out register. Identical to TSEVN register (09h) except that the reading this register clears both TSEVN and TSEVN_COR registers.	0	COR
			[4:7]	Ports 1 to 4 current limit time-out (t_{LIM}).		0	COR
9	TSEVN	8	[0:3]	Ports 1 to 4 over current during start-up time-out (t_{START}). A set bit indicates port is turned OFF due to over current during start-up for period longer than t_{START}.	Overload during Start Up Time Out register. Lower 4 bits indicate port is turned OFF because of an unsuccessful start-up. Upper 4 bits indicate port is turned OFF because it was in current limit for longer than t_{LIM}.	0	RO
			[4:7]	Ports 1 to 4 current limit time-out (t_{LIM}). A set bit indicates port is turned OFF, since after start-up it was forced to limit the current for a period longer than t_{LIM}.			
A	SUPEVN_COR	8	[0:7]	Register 0Ah Clear On Read	Supply Event register. Identical to SUPEVN register (0Bh) except that reading of this register clears both SUPEVN and SUPEVN_COR registers.	0	COR

.....continued

Address (HEX)	Register Name	Width	Bits	Detailed Description	General/Equation	Reset Value (HEX)	Read/ Write
B	SUPEVN	8	[0]	IC power is externally supplied from one of the ports – Microchip proprietary	Supply Event register. Bits in this register indicate problems with power supplies, temperature, or MOSFET failures.	0	RO
			[1]	Reserved		1	RO
			[2]	Chip temperature is over the temperature alarm threshold (9Dh) – Microchip proprietary		0	RO
			[3]	Over Voltage Lock Out (OVLO) on main supply (V_{MAIN}) – Microchip proprietary		0	RO
			[4]	Under Voltage Lock Out (UVLO) on main supply (V_{MAIN}).		1	RO
			[5]	One port or more were denied to power-up due to power management – Microchip proprietary		1	RO
			[6]	If this bit is set, one or more MOSFETs may have failed. To determine which ports may have bad FETs, read the HPSTAT registers (49h, 4Eh, 53h, and 58h).		0	RO
			[7]	This bit is set in case of a thermal shutdown. All ports are turned OFF. This bit can be cleared by reading SUPEVN_COR but TSD bit in WDOG register (42h) will remain set as long as temperature remains above the threshold value.		0	RO

2. Revision History

Revision	Date	Description
A	10/2021	Initial Revision

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