Information note

N° 10287AERRA

Dear customer,

With this Infineon Technologies AG information note, we would like to inform you about the following

Errata Advance Information 2021-09 affecting TC3xx Microcontrollers

On 16 April 2020, Infineon acquired Cypress.
We are now in the process of merging and consolidating our tools and processes for PCN, Information Notes, Errata and Product Discontinuance.
For further details, please visit our website:
https://www.infineon.com/cms/en/about-infineon/company/cypress-acquisition/

Infineon Technologies AG
Postal Address Headquarters: Am Campeon 1-15, D-85579 Neubiberg, Phone +49 (0)89 234-0
Chairman of the Supervisory Board: Dr. Wolfgang Eder
Management Board: Dr. Reinhard Ploss (CEO), Dr. Helmut Gassel, Jochen Hanebeck, Constanze Hufenbecher, Dr. Sven Schneider
Registered Office: Neubiberg
Commercial Register: München HRB 126492

Information note

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▶ **Products affected**	Please refer to attached affected product list 1_cip10287

▶ **Detailed change information**

Subject	Errata Advance Information: New/updated errata/ApHint text modules - Advance information 2021-09 for TC3xx Microcontrollers
Reason	Functional Problems, Application Hints, Documentation Updates

Description

Old	New
■ Not applicable (initial version)	■ Errata Advance Information TC3xx_Errata_Advance_Info_2021_09_v1_0_10287AERRA

▶ **Product identification**	Not applicable (no change of product)
▶ **Impact of change**	Assessment in Application required !
▶ **Attachments**	1_cip10287 affected product list 3_cip10287 TC3xx_Errata_Advance_Info_2021_09
▶ **Intended start of delivery**	Not applicable

If you have any questions, please do not hesitate to contact your local sales office.

Errata Advance Information

Rel. 1.0, 2021-09-30

Device **TC3xx**

Marking/Step **see Table 1**

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Infineon is providing you with product information not previously addressed in the product data sheets or other documentation for the devices listed above. The enclosed information describes device behavior which may affect your current or prior use of the product. As our customers use these products in a number of different applications, Infineon is not in a position to assess the consequences of this device behavior in your specific application(s). Therefore, you should review the enclosed information and evaluate its effect, if any, on your current or prior use of the product in your application(s), including whether there are any safety concerns requiring further action and/or regulatory reporting.

New/updated errata/ApHint text modules - Advance information 2021-09

The following text modules have been compiled and internally reviewed by the Microcontroller Division of Infineon Technologies after the latest TC3xx errata sheet release cycle (2021-07-23). They are provided here as advance information, and shall be integrated into the TC3xx errata sheets in the next quarterly release cycle.

Table 1 New/updated TC3xx errata/ApHint text modules - 2021-09

Text module	Short description	Affected devices	Change	Page
FLASH_TC.056	Reset value for register HF_ECCC is 0x0000 0000 - Documentation correction	All TC3xx	New	3
GTM_AI.358	TOM/ATOM: Synchronous update of working register for RST_CCU0=1 and UDMODE=0b01 not correct	TC3xx with GTM[1)]	Update	3

Table 1 New/updated TC3xx errata/ApHint text modules - 2021-09

Text module	Short description	Affected devices	Change	Page
GTM_AI.387	DPLL: Wrong calculation of pulse generator frequency for DPLL_CTRL_0.AMT/S=1 and DPLL_CTRL_11.ADT/S=1 when number of pulses (DPLL_CTRL_0.MLT or DPLL_MLS1/2.MLS1/2) is too small	TC3xx with GTM except TC33x/32x	New [2]	5
MCMCAN_AI.023	Incomplete description in section *.5.2 “Dedicated Tx Buffers” and *.5.4 “Tx Queue” of the M_CAN documentation in the User’s Manual related to transmission from multiple buffers configured with the same Message ID	All TC3xx	New	5
MEMMAP_TC.001	Size of PFLASH and DFLASH - Correction to TC33xEXT and TC33x/TC32x Appendix	TC33xEXT and TC33x/32x	New	7
PADS_TC.H007	Connection of HWCFG[6] pad in QFP-80 and QFP-100 packages – Explanation to Data Sheet history	TC33x/32x	New	8
RESET_TC.H006	Certain registers may have different reset values than documented in TC3xx User’s Manual - Documentation update	All TC3xx[3]	New	9
SAFETY_TC.023	MCU infrastructure Safety Related Function - Documentation Update	TC3xx with Safety Manual v2.0	New	11
SAFETY_TC.024	Clock alive monitor for f_{SPB} - Documentation update	All TC3xx	New	12

1) TC35x and TC33xEXT have no GTM, therefore not affected in general. GTM in TC33x/TC32x has no DPLL, therefore DPLL issues do not apply to TC33x/TC32x.

2) GTM_AI.387 replaces GTM_AI.H004 previously published in TC3xx errata sheets 2021-07-23
3) TC33x*/TC32x in analysis

FLASH_TC.056 Reset value for register HF_ECCC is 0x0000 0000 - Documentation correction

In the register description for register HF_ECCC (DF0 ECC Control Register) in the TC3xx User's Manual, the application reset value is documented as 0xC000 0000.

However, this register is cleared by the startup software SSW, and the user software will read the reset value of 0x0000 0000.

Documentation correction

- The application reset value for register HF_ECCC is 0x0000 0000.

Note: The user must consider that field HF_ECCC.TRAPDIS is 00_B after reset, which means a bus error trap is generated if an uncorrectable ECC error occurs upon read from DF0, or read from DF1 when DF1 is configured as not HSM_exclusive..

GTM_AI.358 TOM/ATOM: Synchronous update of working register for RST_CCU0=1 and UDMODE=0b01 not correct

TOM/ATOM is configured in SOMP mode with ATOM[i]_CH[x]_CTRL.MODE="10" (only for ATOM) and up-down counter mode is enabled by setting of (A)TOM[i]_CH[x]_CTRL.UDMODE=0b01. With the additional configuration of (A)TOM[i]_CH[x]_CTRL.RST_CCU0=1, the counter direction from up to down is changed with the trigger signal from a preceding channel TRIGIN[x] or with the TIM_EXT_CAPTURE signal from TIM module.

Expected behaviour:

The synchronous update of the working registers (A)TOM[i]_CH[x]_CM0 and (A)TOM[i]_CH[x]_CM1 in this configuration shall be done only when the channel counter (A)TOM[i]_CH[x]_CN0 reaches zero.

Observed behaviour:

Additionally to the update of the working registers (A)TOM[i]_CH[x]_CM0 and (A)TOM[i]_CH[x]_CM1 when the channel counter (A)TOM[i]_CH[x]_CN0 reaches zero, the update is executed with the selected trigger signal TRIGIN[x] or TIM_EXT_CAPTURE(x). This is not expected in this configuration with (A)TOM[i]_CH[x]_CTRL.UDMODE=0b01.

Scope

TOM, ATOM

Effects

The synchronous update of the working register (A)TOM[i]_CH[x]_CM0 and (A)TOM[i]_CH[x]_CM1 is done unintendedly with the selected trigger signal TRIGIN[x] or TIM_EXT_CAPTURE.

Workaround

For settings where the PWM phases are longer than the register access times on target system: Ensure to deliver new data to the associated shadow registers (A)TOM[i]_CH[x]_SR0 and (A)TOM[i]_CH[x]_SR1 only when the channel counter ATOM[i]_CH[x]_CN0 is in down counting phase. The down counting phase is reported by the according interrupt.

The described workaround is only possible for ATOM as long as the ARU interface is disabled and the new shadow register values are delivered by configuration interface and not by ARU interface.

GTM_AI.387 DPLL: Wrong calculation of pulse generator frequency for DPLL_CTRL_0.AMT/S=1 and DPLL_CTRL_11.ADT/S=1 when number of pulses (DPLL_CTRL_0.MLT or DPLL_MLS1/2.MLS1/2) is too small

When the number of pulses per increment DPLL_CTRL_0.MLT is smaller than 127, or DPLL_MLS1/2.MLS1/2 is smaller than 128 and the correction of physical deviations is used (DPLL_CTRL_0.AMT/AMS=1 and DPLL_CTRL_11.ADT/ADS=1), the calculation of internal values such as DPLL_DT_T/S_ACT.DT_T/S_ACT, DPLL_RDT_T/S_ACT.RDT_T/S_ACT, and DPLL_ADD_IN_CAL1/2.ADD_IN_CAL_1/2 is wrong. The resulting frequency of the generated sub increment pulses of the DPLL is too small.

Scope

DPLL

Effects

The frequency of the generated sub increment pulses of the DPLL is too small. This leads to an unbalanced generation of micro ticks.

Workaround

1. Don`t use pulse numbers DPLL_CTRL_0.MLT < 127 and/or DPLL_MLS1/2.MLS1/2 < 128, when using correction of physical deviation (DPLL_CTRL_11.ADT/ADS=1 when DPLL_CTRL_0.AMT/AMS=1).
2. When 1.) cannot be applied use configuration DPLL_CTRL_11.ADT/ADS=0 when DPLL_CTRL_0.AMT/AMS=1 is used.

MCMCAN_AI.023 Incomplete description in section *.5.2 “Dedicated Tx Buffers” and *.5.4 “Tx Queue” of the M_CAN documentation in the User’s Manual related to transmission from multiple buffers configured with the same Message ID

*Note: The absolute chapter number * depends on the version of the User’s Manual.*

Section *.5.2 Dedicated Tx Buffers

Wording User's Manual

In case that multiple dedicated Tx Buffers are configured with the same Message ID, the Tx Buffer with the lowest buffer number is transmitted first.

Enhancement - additional text

These Tx buffers shall be requested in ascending order with lowest buffer number first.

Alternatively all Tx buffers configured with the same Message ID can be requested simultaneously by a single write access to **TXBARi**.

Section *.5.4 Tx Queue

Wording User's Manual - to be deleted

In case that multiple Queue Buffers are configured with the same Message ID, the Queue Buffer with the lowest buffer number is transmitted first.

Replacement

In case that multiple Tx Queue buffers are configured with the same Message ID, the transmission order depends on numbers of the buffers where the messages were stored for transmission. As these buffer numbers depend on the then current states of the PUT index, a prediction of the transmission order is not possible.

Wording User's Manual - to be deleted

An Add Request cyclically increments the Put Index to the next free Tx Buffer.

Replacement

The Put Index always points to that free buffer of the Tx Queue with the lowest buffer number.

Scope

Use of multiple dedicated Tx Buffers or Tx Queue buffers configured with same Message ID.

Effects

In case the dedicated Tx buffers with the same Message ID are not requested in ascending order or at the same time or in case of multiple Tx Queue buffers with the same Message ID, it cannot be guaranteed, that these messages are transmitted in ascending order with lowest buffer number first.

Workaround

In case a defined order of transmission is required the Tx FIFO shall be used for transmission of messages with the same Message ID. Alternatively dedicated Tx buffers with same Message ID shall be requested in ascending order with lowest buffer number first or by a single write access to **TXBARi**. Alternatively a single Tx Buffer can be used to transmit those messages one after the other.

MEMMAP_TC.001 Size of PFLASH and DFLASH - Correction to TC33xEXT and TC33x/TC32x Appendix

Note: This issue only affects V1.6.0 and V2.0.0 of the TC33xEXT and the TC33x/TC32x Appendix.

Versions V1.6.0 and V2.0.0 include incorrect sizes and address ranges for PFLASH (3 Mbyte instead of 2 Mbyte) and DFLASH DF0 (1 Mbyte instead of 128 Kbyte) in table “Address Map as seen by Bus Masters on Bus SRI” in the MEMMAP chapter of the TC33xEXT and TC33x/TC32x Appendix.

Earlier versions (V1.2.0 .. V1.5.0) of the TC33xEXT and TC33x/TC32x Appendix correctly specify the sizes and address ranges for PFLASH (2 Mbyte) and DFLASH DF0 (128 Kbyte).

Documentation correction

The sizes and address ranges for PFLASH and DFLASH DF0 in table “Address Map as seen by Bus Masters on Bus SRI” in the MEMMAP chapter of the

TC33xEXT and TC33x/TC32x Appendix V1.6.0 and V2.0.0 shall be corrected as shown in the following table.

Table 2 Address Map as seen by Bus Masters on Bus SRI - Corrections

Address Range		Size	Unit
from	to		
80000000_H	$801FFFFF_H$	2 Mbyte	Program Flash (PFI0)
80200000_H	$8FDFFFFF_H$	-	Reserved
$A0000000_H$	$A01FFFFF_H$	2 Mbyte	Program Flash (PFI0_NC)
$A0200000_H$	$A7FFFFFF_H$	-	Reserved
$AF000000_H$	$AF01FFFF_H$	128 Kbyte	Data Flash 0 EEPROM (DF0) and Host Command
$AF020000_H$	$AF3FFFFF_H$	-	Reserved

PADS_TC.H007 Connection of HWCFG[6] pad in QFP-80 and QFP-100 packages – Explanation to Data Sheet history

In QFP80 and QFP100 packages, HWCFG[2] and HWCFG[6] pins are not available. Internally, the corresponding pads are handled as follows:

- HWCFG[2] is tied to 1 (via internal pull-up) to ensure EVRC is enabled;
- HWCFG[6] is tied to 0 (connected to V_{SS} via E-PAD) to ensure pins are in tristate.

This is also documented in Note 2.) in figure “Hardware Configuration (HWCFG) pins” in the PMSLE chapter of the TC3xx User’s Manual in version V1.3.0 and later versions.

In V0.6 of the TC33x/TC32x Data Sheet, the E-PAD was listed as VSS pin 81 for QFP-80, pin 101 for QFP-100, and pin 145 for QFP-144 packages, respectively. The E-PAD is explicitly listed in the supply tables in TC33x/TC32x Data Sheet V0.7 and following (see also chapter “History” in corresponding Data Sheets).

RESET_TC.H006 Certain registers may have different reset values than documented in TC3xx User's Manual - Documentation update

The following registers may show different reset values compared to those documented in the TC3xx User's Manual or TC3xy appendix. During device start-up, the initial hardware reset values of certain registers may be updated. Consequently, user software may read different values. Please refer to the table below for further details.

Note: The TC3xx User's Manual chapters and/or register bitfield descriptions may contain information in addition to reset values/tables.

*Note: The registers listed in the table apply to TC39x..TC35x and TC3Ex. Presence of CPU*_PCON1 registers depends on number of available CPUs.*

Table 3 TC3xx registers that may have different reset values than documented in TC3xx User's Manual

Register	Initial reset value	Reset value defined in User's Manual	Remark
P20_IOCR0	0x0010 0000	0x0000 0000 (HWCFG6 = tri-state)	TESTMODE pin is PU (input pull-up), even with HWCFG6 = tri-state, as described in Data Sheet.
EMEM_TILECONFIG	0x0000 0000	0x5555 5555	This is a write-only ("w") register. For tile mode information do not read EMEM_TILECONFIG; instead, read EMEM_TILESTATE.
SBCU_DBCNTL	0x0000 7002	0x0000 7003	Bit EO is "Status of BCU Debug Support Enable" and only set after reset when OCDS is enabled. This bit is controlled by Cerberus.

Table 3 TC3xx registers that may have different reset values than documented in TC3xx User's Manual (cont'd)

Register	Initial reset value	Reset value defined in User's Manual	Remark
CPU1_PCON1	0x0000 0001	0x0000 0000	Bit PCINV of PCON1 is set when CPU is in boot halt mode, it is cleared when CPU starts execution
CPU2_PCON1	0x0000 0001	0x0000 0000	
CPU3_PCON1	0x0000 0001	0x0000 0000	
CPU4_PCON1	0x0000 0001	0x0000 0000	
CPU5_PCON1	0x0000 0001	0x0000 0000	
HSSL0_MFLAGS	0xA000 0000	0x8000 0000	Bit TEI indicates the state of CTS (Clear To Send) signal from HSCT module. The default state of this bit is 1.
HF_OPERATION	0x0000 0X00	0x0000 0000	RES bits shall be ignored.
PMS_EVRSDCTRL0	0x3039 0001	0xF039 0001	LCK and UP bits are cleared.
PMS_EVRSDCTRL1	0x0669 0708	0x8669 0708	LCK bit is cleared.
PMS_EVRSDCTRL6	0x0023 1C94	0x8023 1C94	LCK bit is cleared.
PMS_EVRSDCTRL7	0x0000 00FE	0x8000 00FE	LCK bit is cleared.
PMS_EVRSDCTRL8	0x1121 048E	0x9121 048E	LCK bit is cleared.
PMS_EVRSDCTRL9	0x0000 0434	0x8000 0434	LCK bit is cleared.
PMS_EVRSDCTRL11	0x1207 0909	0x9207 0909	LCK bit is cleared.
PMS_EVRSDCOEFF0	0x3508 73B6	0xB508 73B6	LCK bit is cleared.

Table 3 TC3xx registers that may have different reset values than documented in TC3xx User's Manual (cont'd)

Register	Initial reset value	Reset value defined in User's Manual	Remark
PMS_EVRSDCOEFF1	0x2294 6C46	0xA294 6C46	LCK bit is cleared.
PMS_EVRSDCOEFF6	0x0097 1802	0x8097 1802	LCK bit is cleared.
PMS_EVRSDCOEFF7	0x0000 D8F7	0x8000 D8F7	LCK bit is cleared.
PMS_EVRSDCOEFF8	0x0017 1002	0x8017 1002	LCK bit is cleared.
PMS_EVRSDCOEFF9	0x0000 A0AF	0x8000 A0AF	LCK bit is cleared.
SCU_OSCCON	0x0000 0258 for UCB_DFLASH.OSCCFG = 0;0x0XX0 XXXX otherwise	0x0000 0X1X	SCU_OSCCFG setting is recovered from UCB_DFLASH

SAFETY_TC.023 MCU infrastructure Safety Related Function - Documentation Update

Note: This issue applies to AURIX™ TC3xx Safety Manual version v2.0.

Section 4.3.1 (Introduction) of chapter "Safety Related Functions" in the AURIX™ TC3xx Safety Manual v2.0 mentions in the last bullet point below the table that Safety Related Functions 10, 11 and 12 shall always be correctly implemented in order to reach the ASIL level of the listed Safety Related Functions.

The listed absolute numbers 10, 11, 12 are not correct in this context.

Documentation Update

The MCU infrastructure Safety Related functions **12, 13 and 14** are assumed to be always correctly implemented.

SAFETY_TC.024 Clock alive monitor for f_{SPB} - Documentation update

The AURIX™ TC3xx Safety Manual states in section 6.37 SM[HW]:CLOCK:ALIVE_MONITOR that the clock alive monitor for f_{SPB} is only visible to HSM.

This statement is not correct.

Documentation update

The clock alive monitor for f_{SPB} is visible to all interfaces in the SMU.

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Errata Advance Information 2021-09 affecting TC3xx Microcontrollers

Sales name	SP number	OPN	Package
SAK-TC322LS-24F160F AA	SP005424932	TC322LS24F160FAAKXUMA1	PG-TQFP-80-7
SAK-TC332LP-32F200F AA	SP004264616	TC332LP32F200FAAKXUMA1	PG-TQFP-80-7
SAK-TC332LP-32F300F AA	SP004974864	TC332LP32F300FAAKXUMA1	PG-TQFP-80-7
SAK-TC333LP-32F300F AA	SP004974874	TC333LP32F300FAAKXUMA1	PG-TQFP-100-23
SAK-TC334LP-32F200F AA	SP001724294	TC334LP32F200FAAKXUMA1	PG-TQFP-144-27
SAK-TC334LP-32F300F AA	SP004974878	TC334LP32F300FAAKXUMA1	PG-TQFP-144-27
SAK-TC336LP-32F300S AA	SP004974908	TC336LP32F300SAAKXUMA1	PG-LFBGA-180-1
SAK-TC337DA-32F300S AA	SP004974938	TC337DA32F300SAAKXUMA1	PG-LFBGA-292-13
SAK-TC337DZ-32F200S AA	SP002268356	TC337DZ32F200SAAKXUMA1	PG-LFBGA-292-13
SAK-TC337LP-32F300S AA	SP004974944	TC337LP32F300SAAKXUMA1	PG-LFBGA-292-11
SAK-TC356TA-64F300S AB	SP003833202	TC356TA64F300SABKXUMA1	PG-LFBGA-180-1
SAK-TC356TD-48F300S AB	SP005424938	TC356TD48F300SABKXUMA1	PG-LFBGA-180-1
SAK-TC356TH-64F300S AB	SP004818890	TC356TH64F300SABKXUMA1	PG-LFBGA-180-1
SAK-TC357TA-64F300S AB	SP003803252	TC357TA64F300SABKXUMA1	PG-LFBGA-292-13
SAK-TC357TH-64F300S AB	SP003803258	TC357TH64F300SABKXUMA1	PG-LFBGA-292-13
SAK-TC364DP-48F300F AA	SP004577254	TC364DP48F300FAAKXUMA1	PG-TQFP-144-27
SAK-TC364DP-64F300F AA	SP001713956	TC364DP64F300FAAKXUMA1	PG-TQFP-144-27
SAK-TC364DP-64F300W AA	SP001714740	TC364DP64F300WAAKXUMA1	PG-LQFP-144-25
SAK-TC365DP-64F300W AA	SP001724126	TC365DP64F300WAAKXUMA1	PG-LQFP-176-22
SAK-TC367DP-64F300S AA	SP001694656	TC367DP64F300SAAKXUMA1	PG-LFBGA-292-11
SAK-TC367V0-64F300S AA	SP005411327	TC367V064F300SAAKXUMA1	PG-LFBGA-292-11
SAK-TC375TP-96F300W AA	SP001724106	TC375TP96F300WAAKXUMA1	PG-LQFP-176-22
SAK-TC377DP-96F300S AA	SP004987108	TC377DP96F300SAAKXUMA1	PG-LFBGA-292-11
SAK-TC377TP-96F300S AA	SP001694648	TC377TP96F300SAAKXUMA1	PG-LFBGA-292-11
SAK-TC377TX-96F300S AB	SP004950416	TC377TX96F300SABKXUMA1	PG-LFBGA-292-13
SAK-TC377VS-96F300S AA	SP005546304	TC377VS96F300SAAKXUMA1	PG-LFBGA-292-11
SAK-TC387QP-160F300S AD	SP002921224	TC387QP160F300SADKXUMA1	PG-LFBGA-292-11
SAK-TC387QP-160F300S AE	SP005351247	TC387QP160F300SAEKXUMA1	PG-LFBGA-292-11
SAK-TC387TP-128F300S AD	SP002921230	TC387TP128F300SADKXUMA1	PG-LFBGA-292-11
SAK-TC387TP-128F300S AE	SP005351248	TC387TP128F300SAEKXUMA1	PG-LFBGA-292-11
SAK-TC387TP-128F300S AE	SP005425390	TC387TP128F300SAEKXQMA1	PG-LFBGA-292-11
SAK-TC389QP-160F300S AD	SP002921222	TC389QP160F300SADKXUMA1	PG-FBGA-516-1
SAK-TC389QP-160F300S AE	SP005351252	TC389QP160F300SAEKXUMA1	PG-FBGA-516-1
SAK-TC397QA-160F300S BC	SP002739588	TC397QA160F300SBCKXUMA1	PG-LFBGA-292-12
SAK-TC397QA-160F300S BD	SP005351257	TC397QA160F300SBDKXUMA1	PG-LFBGA-292-12
SAK-TC397XA-256F300S BC	SP002739594	TC397XA256F300SBCKXUMA1	PG-LFBGA-292-12
SAK-TC397XA-256F300S BD	SP005351382	TC397XA256F300SBDKXUMA1	PG-LFBGA-292-12
SAK-TC397XP-256F300S BC	SP002739600	TC397XP256F300SBCKXUMA1	PG-LFBGA-292-10
SAK-TC397XP-256F300S BD	SP005351385	TC397XP256F300SBDKXUMA1	PG-LFBGA-292-10
SAK-TC397XP-256F300S BD	SP005433583	TC397XP256F300SBDKXQMA1	PG-LFBGA-292-10
SAK-TC397XX-256F300S BC	SP002725526	TC397XX256F300SBCKXUMA1	PG-LFBGA-292-10

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Sales name	SP number	OPN	Package
SAK-TC397XX-256F300S BD	SP005351387	TC397XX256F300SBDKXUMA1	PG-LFBGA-292-10
SAK-TC399XP-256F300S BC	SP002725524	TC399XP256F300SBCKXUMA1	PG-LFBGA-516-10
SAK-TC399XP-256F300S BD	SP005351394	TC399XP256F300SBDKXUMA1	PG-LFBGA-516-10
SAK-TC399XX-256F300S BC	SP002725518	TC399XX256F300SBCKXUMA1	PG-LFBGA-516-10
SAK-TC399XX-256F300S BD	SP005351395	TC399XX256F300SBDKXUMA1	PG-LFBGA-516-10
SAK-TC3E7QF-192F300S AA	SP005345769	TC3E7QF192F300SAAKXUMA1	PG-LFBGA-292-11
SAK-TC3E7QG-160F300S AA	SP005345771	TC3E7QG160F300SAAKXUMA1	PG-LFBGA-292-11
SAL-TC364DP-64F300F AA	SP001724134	TC364DP64F300FAALXUMA1	PG-TQFP-144-27
SAL-TC375TI-96F300W AA	SP005428963	TC375TI96F300WAALXUMA1	PG-LQFP-176-22
SAL-TC375TI-96F300W AA	SP005572121	TC375TI96F300WAALXUMA2	PG-LQFP-176-22
SAL-TC375TP-96F300W AA	SP001724110	TC375TP96F300WAALXUMA1	PG-LQFP-176-22
SAL-TC377DP-96F300S AA	SP004987116	TC377DP96F300SAALXUMA1	PG-LFBGA-292-11
SAL-TC377TP-96F300S AA	SP001724092	TC377TP96F300SAALXUMA1	PG-LFBGA-292-11
SAL-TC387QP-160F300S AD	SP002921220	TC387QP160F300SADLXUMA1	PG-LFBGA-292-11
SAL-TC387QP-160F300S AE	SP005351250	TC387QP160F300SAELXUMA1	PG-LFBGA-292-11
SAL-TC387TP-128F300S AD	SP003021930	TC387TP128F300SADLXUMA1	PG-LFBGA-292-11
SAL-TC387TP-128F300S AE	SP005398494	TC387TP128F300SAELXUMA1	PG-LFBGA-292-11
SAL-TC389QP-160F300S AD	SP002921216	TC389QP160F300SADLXUMA1	PG-FBGA-516-1
SAL-TC389QP-160F300S AE	SP005351253	TC389QP160F300SAELXUMA1	PG-FBGA-516-1
SAL-TC397XP-256F300S BC	SP002725522	TC397XP256F300SBCLXUMA1	PG-LFBGA-292-10
SAL-TC397XP-256F300S BD	SP005351392	TC397XP256F300SBDLXUMA1	PG-LFBGA-292-10
SAL-TC399XP-256F300S BC	SP002725520	TC399XP256F300SBCLXUMA1	PG-LFBGA-516-10
SAL-TC399XP-256F300S BD	SP005351397	TC399XP256F300SBDLXUMA1	PG-LFBGA-516-10
SAL-TC399XX-256F300S BD	SP005351398	TC399XX256F300SBDLXUMA1	PG-LFBGA-516-10