Product Change Notification / CYER-05NWLS164

Date:

26-Aug-2021

Product Category:

FPGA Kits and Boards, General Purpose FPGAs

PCN Type:

Document Change

Notification Subject:

Memolog# ML082021003U Final Notice: Release of revised timing data in Libero SoC v2021.2 for selected products in the PolarFire FPGA device family, including selected CPSOM-MPFxxx, MPF100Txxx, MPF200Txxx, MPF300Txxx and MPF500Txxx device families.

Affected CPNs:

CYER-05NWLS164_Affected_CPN_08262021.pdf
CYER-05NWLS164_Affected_CPN_08262021.csv

Notification Text:

PCN Status: Final notification.

PCN Type: Manufacturing Change
Microchip Parts Affected: Please open one of the files found in the Affected CPNs section.

NOTE: For your convenience Microchip includes identical files in two formats (.pdf and .xls).

Description of Change: Release of revised timing data in Libero SoC v2021.2 for selected products in the PolarFire FPGA device family, including selected CPSOM-MPFxxx, MPF100Txxx, MPF200Txxx, MPF300Txxx and MPF500Txxx device families.
Customer notification details.

Note: Once released, Libero SoC v2021.2 will be available for download on the webpage below.

https://www.microsemi.com/product-directory/design-resources/1750-libero-soc#downloads

Pre and Post Change Summary:

	Pre Change	Post Change
Firmware	All Libero SoC releases supporting PolarFire FPGAs up to and including Libero SoC v2021.1.	Libero SoC v2021.2 and later.

Impacts to Data Sheet: None

Change Impact: None

Reason for Change: Release updated PolarFire FPGA timing data along with Libero SoC v2021.2 to improve the accuracy of Static Timing Analysis (STA) performed on PolarFire designs, as described in the attached Customer Notice.

Change Implementation Status: In Progress

Estimated Implementation Date:
August 25, 2021 (date code: 2134)

Time Table Summary:

	August 2021				
Workweek	32	33	34	35	36
Final PCN Issue Date				X	
Estimated Implementation Date			X		

Method to Identify Change: Not applicable. New firmware will be made available as defined above

Qualification Report: Not applicable

Revision History:
August 25, 2021: Issued final notification to reveal the appropriate firmware release.

The change described in this PCN does not alter Microchip's current regulatory compliance regarding the material content of the applicable products.

Attachments:

CN-PolarFire_FPGA_Timing_Data_Update_Libero_2021p2.pdf

Please contact your local Microchip sales office with questions or concerns regarding this notification.

Terms and Conditions:

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If you wish to change your PCN profile, including opt out, please go to the PCN home page select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.

Customer Notification (CN)

Subject: PolarFire FPGA Timing Data Update in Libero SoC v2021.2

Aug 16, 2021

Description:

This customer notification applies to FPGA Static Timing Analysis (STA) data used with Microchip's PolarFire FPGAs and the Libero SoC design tool suite. As part of continuous improvement efforts, Libero SoC v2021.2 has been updated to improve the accuracy of the PolarFire timing data in two specific cases, described in the following section.

Reason for Change:

Prior to Libero SoC v2021.2, STA of the two PolarFire timing paths below used delay values that were slightly underestimated:

1) Unused IP Interface Logic Elements used as regular combinatorial logic elements have LUT4 B input to Y output delay that was underestimated by up to 35 ps worst-case.
   - IP Interface Logic Elements are used to connect hard IP blocks in the FPGA fabric, such as RAM blocks and Mathblocks, to user logic. When the associated hard IP blocks are unused in a design, Libero SoC can re-use the IP Interface LUTs and SLEs for user fabric logic. In this scenario, the 4-input LUT input B to output Y path can be used for user logic.

2) MathBlock input registers have enable pin setup time that was underestimated by up to 77 ps worst-case.
   - Example Mathblock input register enable pins are: A_EN, B_EN, C_EN, and D_EN.

Application Impact:

During internal analysis on Microchip's suite of PolarFire regression test designs, there were zero new violations uncovered after re-running STA with the updated timing data. Although the statistical analysis shows that these timing data updates have a minor impact, there is a theoretical corner case design where multiple cascaded IP interface logic element LUT4 input to output paths could exist on the critical path. Therefore, Microchip recommends performing the actions described in the section below.

Required Action:

New and ongoing designs:

Microchip recommends upgrading to Libero SoC v2021.2 or later and re-running STA to ensure the updated timing data is used when performing STA.

Designs completed prior to the release of Libero SoC v2021.2:

No further actions are listed if the design has successfully completed full system functional hardware testing on every production unit over the entire operating conditions range.

For completed designs that don't meet the criteria above, Microchip has created a Tcl detection script that can be run on a completed design to report whether the design's critical paths are impacted by this timing data update. If there are no new timing violations reported after running the Tcl script, then no further actions are recommended. If the updated timing violation reports generated by the Tcl script lists new violations, Microchip recommends opening the completed design in Libero SoC v2021.2 and running an incremental Timing Driven Place and Route (TDPR) with Minimum Delay Repair (MDR) enabled to see if the violations can be resolved, and if not try running a full TDPR with MDR enabled.

The Tcl detection script can be downloaded at the link below:
http://soc.microsemi.com/download/rsc/?f=CN-2021.2-PolarFire-Timing-Data

Contact Information:

If you have any questions about this subject, contact Microchip FPGA-BU Technical Support at the web portal below:
http://www.microchip.com/support

Regards,

Microsemi Corporation, a wholly owned subsidiary of Microchip Technology Inc.

CYER-05NWLS164 - Memolog# ML including s MPF100Tx MPF200Tx MPF300Txxx and MPF500Txxx de

Affected Catalog Part Numbers(CPN)

MPF200TS-FCSG536I
MPF200TS-FCVG484I
MPF200TS-WAFER
MPF300T-1FCG1152E
MPF300T-1FCG1152EX3
MPF300T-1FCG1152I
MPF300T-1FCG1152IX45
MPF300T-1FCG484E
MPF300T-1FCG484I
MPF300T-1FCG784E
MPF300T-1FCG784I
MPF300T-1FCG784NE
MPF300T-1FCG784NI
MPF300T-1FCSG536E
MPF300T-1FCSG536I
MPF300T-1FCVG484E
MPF300T-1FCVG484I
MPF300T-FCG1152E
MPF300T-FCG1152I
MPF300T-FCG484E
MPF300T-FCG484EX52
MPF300T-FCG484I
MPF300T-FCG784E
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MPF300T-FCG784NE
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MPF300TS-FCSG536I
MPF300TS-FCV484M
MPF300TS-FCVG484I
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MPF500TS-FC1152MX167
MPF500TS-FC784M
MPF500TS-FCG1152I
MPF500TS-FCG784I
MPF500TS-WAFER
CPSOM-MPF100T-FCSG325
CPSOM-MPF200T-FCSG536
CPSOM-MPF300T-FCG484
MPF100T-1FCG484E
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MPF100T-1FCSG325E
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