Product Change Notification / SYST-11EZTD257

Date:

12-Aug-2021

Product Category:

Broadband Gateway

PCN Type:

Document Change

Notification Subject:

Data Sheet - Le9643 Datasheet

Affected CPNs:

SYST-11EZTD257_Affected_CPN_08122021.pdf
SYST-11EZTD257_Affected_CPN_08122021.csv

Notification Text:

SYST-11EZTD257

Microchip has released a new Product Documents for the Le9643 Datasheet of devices. If you are using one of these devices please read the document located at Le9643 Datasheet.

Notification Status: Final

Description of Change: Converted the legacy document to the Microchip format and updated the following sections:
1) Package Outline
2) Related Collateral

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 12 Aug 2021

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

Le9643 Datasheet

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

LE9643AQC
LE9643AQCT

Le9643 Subscriber Line Interface Circuit miSLIC™ Series

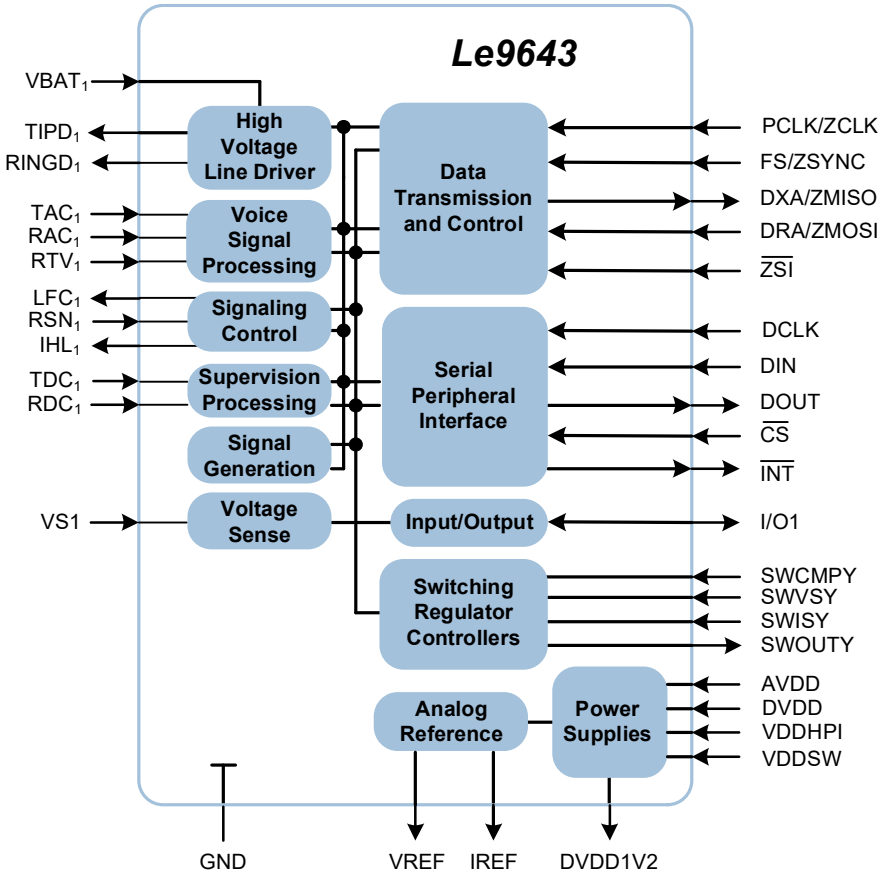
Introduction

The miSLIC™ Series Line Circuits together with a VoIP processor or SoC, provides an economical turn-key solution for derived voice applications. The versatile Le9643 miSLIC can be controlled via a PCM/SPI or ZSI interface.

The Le9643 miSLIC 1 FXS Tracking device is a cost optimized FXS solution. The Le9643 uses energy efficient power supply topologies for reduced BOM cost. The Le9643 can be configured to operate a Buck-Boost fixed tracking supply or an Inverting-Boost supply. Ringing and system power management are supported to limit the peak power requirements of the telephone line FXS port. The Le9643 features wideband clarity and complete BORSCHT functionality.

Manufacturing self test and subscriber line diagnostics are available features. All AC, DC, and power parameters are programmable making the Le9643 device suitable for any short loop application requiring SLIC functionality.

Figure 1. Le9643 Block Diagram



Features

- Cost Optimized Single Channel FXS Solution
  - Smaller, 36-pin 4x6 mm QFN package
  - Low cost, 2-Layer PCB Reference Designs
- Software compatible with equivalent features to the Le9641
- Pin-Selectable PCM/SPI or ZSI Interfaces
  - Single port 4-wire ZSI control simplifies board routing
  - Compatible with numerous VoIP processors and SoC solutions
- 95V Peak Battery Designs
  - Up to 60-VRMS with up to 3 REN load
  - Up to 50-VRMS with up to 5 REN load
- Energy Efficient Switching Regulator Architectures
  - Consistent with Code of Conduct on Energy Consumption of Broadband Equipment
- VoicePath SDK and VP-API-II Software available to implement FXS functions
- VeriVoice Professional Test Suite Software
  - Comprehensive subscriber loop testing, including *Telcordia GR-909-CORE / TIA-1063*
- VeriVoice Manufacturing Test Package (VVMT)
  - Facilitates factory testing of assembled boards
- Complete Wideband BORSCHT functionality
- Worldwide Programmability
- Narrowband or Wideband operation

Applications

- Fixed Wireless (LTE) Gateways
- DSL Residential Gateways and Integrated Access Devices (IADs)
- Cable Embedded Multimedia Terminal Adapters (eMTAs)
- PON Single Family Units (SFU)
- Fiber-to-the-premise (FTTX) solutions
- Analog Telephone Adapters (ATAs)

Table of Contents

1. miSLIC™ Series Solution Overview

The sixth-generation *miSLIC* line interface solution consists of *a miSLIC* device, *VoicePath API-II (VP-API-II)* Software, and *Profiles* Data Structures. To support the *miSLIC* device, Microchip offers comprehensive software and hardware collateral packages, including 2-layer printed circuit board reference designs.

The *VoicePath API-II (VP-API-II)* software initializes the FXS port coefficient data containing application or country- specific AC and DC parameters, ringing and other signaling characteristics, and configures the switching power supply. *VP-API-II* resides on the customer's VoIP processor or SoC and provides high-level control over the telephony functions. *VP-API-II* offers a seamless migration between products utilizing its common software architecture and interfaces with the Microchip *VeriVoice Professional Test Suite Software*.

A *Microsoft® Windows®* GUI (Graphical User Interface) application, *VoicePath Profile Wizard (VP Profile Wizard)*, allows the user to select the operating parameters of the FXS channels and to automatically generate the sets of data structures, called *Profiles*, that are required by the *VP-API-II* for integration with the VoIP host software.

1.1 Le9643 Tracking Battery miSLIC Device

The Le9643 miSLIC device implements a universal telephone line interface with pin-selectable PCM and SPI or ZSI serial digital interfaces. All AC, DC, and signaling parameters are fully programmable via the PCM and SPI or reduced pin-count ZSI interfaces.

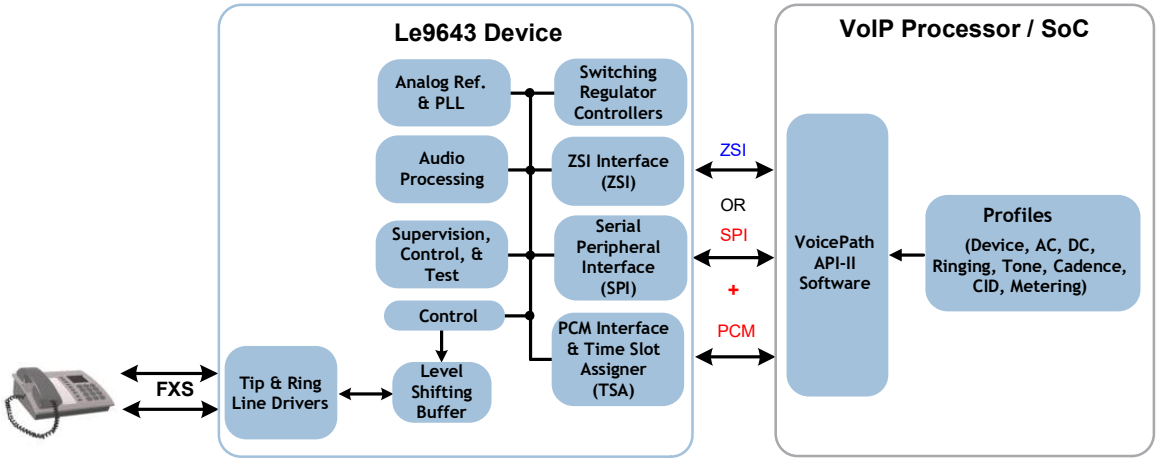
The switching regulator controller generates the high voltage needed for efficiently powering and ringing analog telephones. The Le9643 supports two switching regulator architectures, both are capable of ringing 85-VPK; a Buck-Boost fixed tracking switching regulator architecture which uses a fixed voltage for ringing signals, or an Inverting-Boost switcher circuit which tracks the ringing voltage during ringing. The battery tracks the DC feed with both architectures. The switching regulators provide high efficiency in all operating states and corresponding low power consumption. See the Switching Regulator Controller section for more information.

The Le9643 utilizes the *VeriVoice Professional Test Suite Software* to resolve line circuit faults and to provide line diagnostics. The integrated digital access to line information such as AC and DC line voltages and Metallic or Longitudinal currents is crucial for remote applications where dedicated test hardware is not cost effective.

Additionally, the *VeriVoice Manufacturing Software (VVMT)* package provides test functions intended to facilitate factory testing, eliminating the need for expensive external test equipment.

The figure below shows a high-level solution diagram with a *Le9643* device, *VP-API-II* and *Profiles*.

Figure 1-1. Le9643 Solution Diagram



2. Device Overview

- Buck Boost Power Supply with 95 V peak battery designs
  - Up to $60V_{RMS}$ with up to 3 REN Load
  - Up to $50V_{RMS}$ with up to 5 REN Load
- Cost Optimized Single chip solution provides high voltage line driving, digital signal processing, and high voltage power generation for one line
- Wideband 150 Hz – 6.8 kHz and Narrowband 200 Hz – 3.4 kHz Codec modes
  - Compliant with Cable Labs *PacketCable High Definition Voice Specification PKT-SP-HDV-104-120823*
- Exceeds *Telcordia® GR-909-CORE* transmission requirements
- Single hardware design meets worldwide requirements through software programming of:
  - Ringing waveform, frequency and amplitude
  - DC loop-feed characteristics and current limit
  - Loop-supervision detection thresholds
  - Off-hook debounce circuit
  - Ground-key and ring trip filters
  - Two-wire AC impedance
  - Transhybrid balance impedance
  - Transmit and receive gains and equalization
  - A-law/µ-law and linear coding selection
  - Switching power supply
- Supports loop-start and ground-start signaling
- On-hook transmission
- Power/service denial mode
- Smooth polarity reversal
- Supports wink function
- Internal Test Termination
- Compatible with inexpensive protection networks
- Self-contained ringing generation and control
  - Programmable ringing cadencing
  - Internal battery-backed balanced sinusoidal or trapezoidal
  - Integrated ring trip filter and software, manual or automatic ring trip mode
- Flexible tone generation
  - Call progress tone generation
  - Howler tone generation with *VP-API-II*
  - Integrated switching regulator controller
    - Generates battery voltage for the line
    - Energy efficient in all states
    - Low idle-power
    - Line-feed characteristics independent of battery voltage
  - *VeriVoice Professional Test Suite Software*
    - Monitors two-wire interface voltages and currents for subscriber line diagnostics
    - Integrated self-test features
- *VeriVoice Manufacturing Test Package*
- Supported by *VoicePath SDK* and *VP-API-II*
- Monitors and drives Tip & Ring independently
- Built-in voice-path test modes
- Small physical size in 4x6 mm, 36-pin QFN
- -40°C to +85°C operation

- Low-Power Idle Mode (LPIM)
  - Voltage-based off-hook detection
- Supervision ADC for advanced testing
  - Monitors up to 5 signals in multiplexed mode, such as V_{TIP}, V_{RING}, I_M, I_L, & VBAT
- Simultaneous ground key / DC fault detection
- Over current monitoring and blanking
- Hook and ground key detection with hysteresis and calibrated thresholds
- On-chip timer functions
- Tone generators with frequency modulation capability for compliance with *BT*, *NTT*, and *Austel* special Howler tone requirements
- ZSI interface voltage
  - Supports communication with host processors at 3.3 V
- Low BOM cost:
  - Compatible with 2-layer PCB designs
  - Small value/size/cost switcher output and SLIC capacitors
  - No external diodes for protecting SLIC against negative surges
- Comprehensive device calibration capabilities
  - Short calibration time
  - No need to generate voltages to the Tip/Ring interface
  - Programmable loop current dependent overhead

3. Functional Description

3.1 Host Port Interface

The Le9643 device features a flexible host port interface which is hardware-selectable for communicating with VoIP processors and SoCs using standard PCM and SPI or the reduced pin-count ZSI interfaces. The host port interface mode is selected using the ZSI pin.

The host port interface voltage level (VDDHPI) can be set for 1.8 V, 2.5 V, or 3.3 V for maximum system-level compatibility. The host port interface supports PCM clock (PCLK) rates of 1.024 MHz, 1.536 MHz, 2.048 MHz,

3.072 MHz, 4.096 MHz, 6.144 MHz, and 8.192 MHz with a Frame Sync (FS) of 8 kHz (or 16 kHz in Wideband mode).

PCM and SPI modes are discussed in Section 3.1.1 and Section 3.1.2 respectively. ZSI mode is discussed in Section 3.1.3.

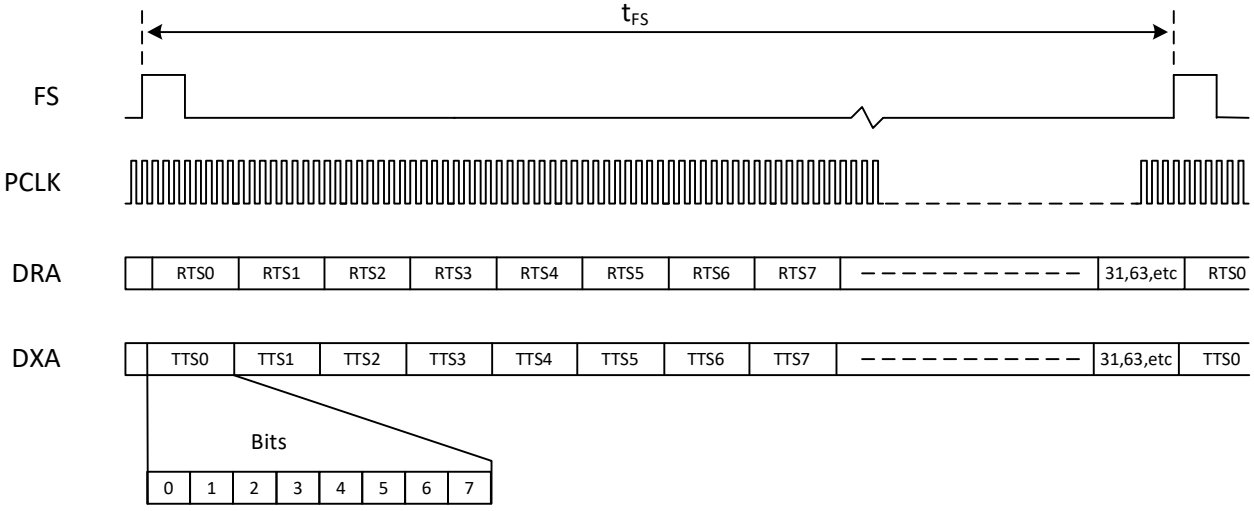
3.1.1 PCM Interface and Time Slot Assigner

The PCM Interface and Time Slot Assigner (PCM block) is a synchronized serial mode of communication between the system and the Le9643 device. In PCM mode, voice data is transmitted/received on a serial PCM highway with FS and PCLK used as references. The host port interface operates in this mode if the ZSI pin is pulled high.

Data is transmitted out of the DXA pin and received on the DRA pin. The Le9643 device transmits/receives single 8-bit time slot (A-law/µ-law) compressed voice data or 16-bit two's complement linear voice data in two contiguous time slots. The PCLK is a data clock supplied to the device that determines the rate at which the data is shifted in/out of the PCM ports. The FS pulse identifies the beginning of a transmit/receive frame and all time slots are referenced to it. For the Le9643 device, the frequency of the FS signal can be 8 kHz (Narrowband or 8 kHz Wideband modes) or 16 kHz (Wideband mode). In Wideband mode, two evenly spaced sets of time slots are exchanged in each frame. The PCLK frequency can be a number of fixed frequencies as defined by the *VP-API-II*. Refer to the Figure 10-2. Profile Wizard – Device Profile Configuration section for an example setting of the Transmit and Receive Clock Slots, PCM Transmit Edge, and PCLK Frequency.

The *VP-API-II* allows the time slots to be offset to eliminate any clock skew in the system. The Transmit Clock Slot and Receive Clock Slot fields are each three bits wide to offset the time slot assignment by 0 to 7 PCLK periods. The Transmit and Receive Clock Slot is a global command that is applied at the device level. Thus, for each channel, two time slots must be assigned: one for transmitting voice data and the other for receiving voice data. The figure below shows the PCM highway time slot structure. The t_{FS} timing is either 125 µs or 62.5 µs depending on the frequency of FS.

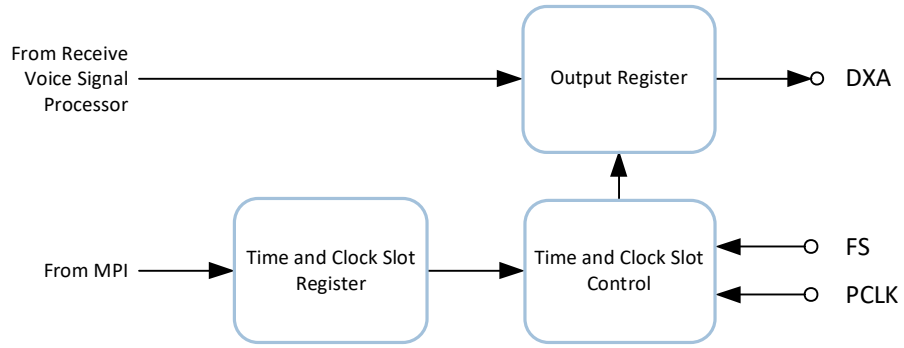
Figure 3-1. PCM Highway Structure



3.1.1.1 Transmit PCM Interface

The Transmit PCM interface receives an 8-bit compressed code (A-law/μ-law) or a 16-bit two's complement linear code from the voice signal processor (compressor). The transmit PCM interface logic, as shown in the figure below, controls the transmission of the data onto the PCM highway through the output port selection circuitry and the time and clock slot control block. The data can be transmitted on either edge of the PCLK, as selected in the *Device Profile*.

Figure 3-2. Transmit PCM Interface



The *VP-API-II* allows the time slot of the selected channel to be programmed. The Transmit Time Slot Register is 7 bits wide and allows up to 128 8-bit time slots in each frame, depending on the value of the PCLK frequency, the encoding scheme, and whether Narrowband or Wideband modes are selected. Refer to the table below for the maximum number of available time slots. Please note that linear mode requires two back-to-back time slots to transmit one voice channel. The data is transmitted in bytes with the most significant bit first. Wideband mode requires twice the number of transmit time slots as Narrowband linear mode.

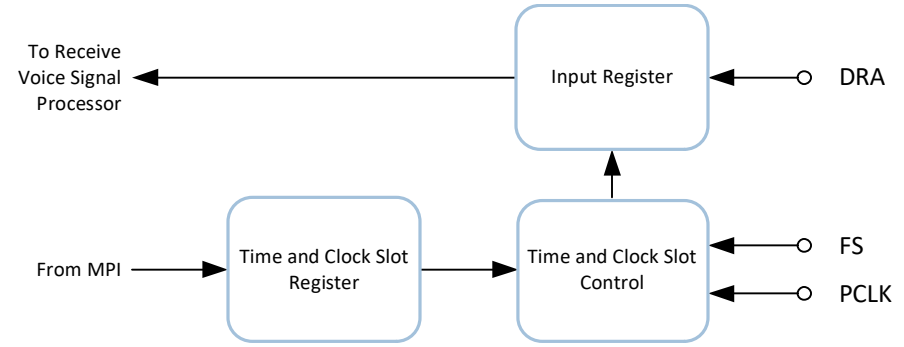
Table 3-1. Maximum Number of Transmit or Receive Time Slots

Audio Mode	FS Freq	Encoding	1.024 MHz	2.048 MHz	4.096 MHz	8.192 MHz
Narrowband (8 kHz sampling)	8 kHz	8-bit compressed, A-law/μ-law companding	16	32	64	128
	8 kHz	16-bit linear	8	16	32	64
Wideband (16 kHz sampling)	8 kHz or 16 kHz	8-bit compressed	8	16	32	64
	8 kHz or 16 kHz	16-bit linear	4	8	16	32

3.1.1.2 Receive PCM Interface

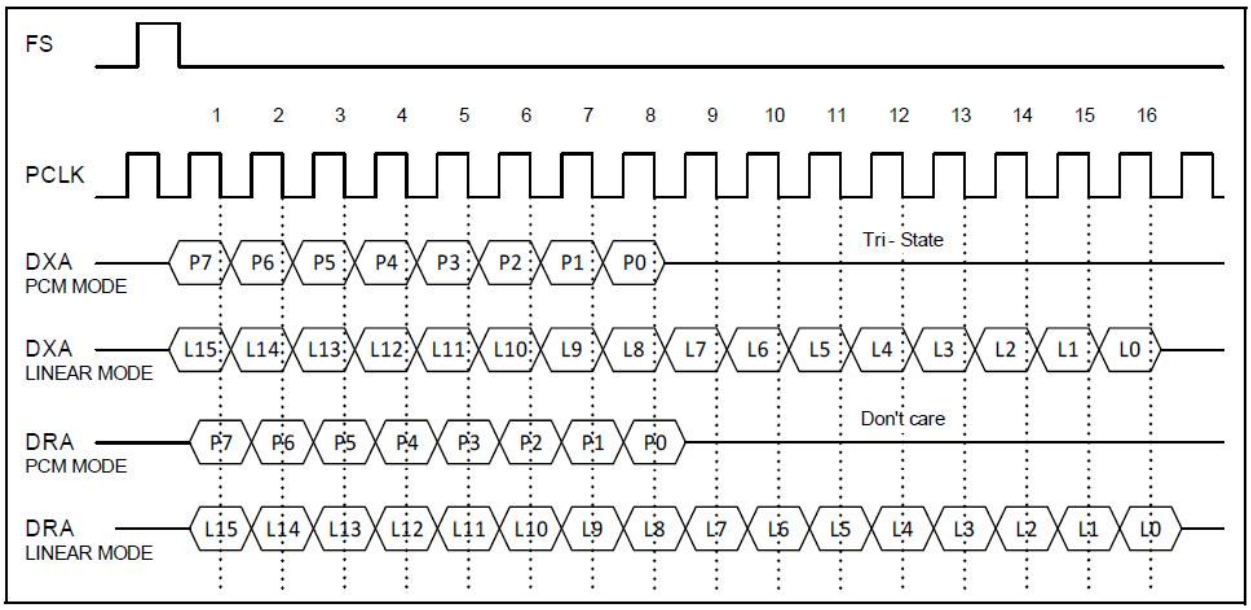
The receive PCM interface logic, as shown in the figure below, controls the reception of data bytes from the PCM highway. 8-bit compressed (A-law/μ-law) or 16-bit two's complement linear data is formatted and passed to the voice signal processor (expander).

Figure 3-3. Receive PCM Interface



The *VP-API-II* allows the time slot of the selected channel to be programmed. The Receive Time Slot Register is 7 bits wide and allows up to 128 8-bit time slots in each frame. Refer to the table above for the maximum number of available channels. Please note that linear mode requires two back-to-back time slots to receive one voice channel. The data is transmitted in bytes with the most significant bit first. Wideband mode requires twice the numbers of receive time slots as Narrowband linear mode. Please refer to the VP-API-II Functions for Speech Coding table for more details about setting the Codec mode and transmit and receive time slots. The following figure illustrates data flow on the PCM highway with data transmitted on the negative PCLK edge.

Figure 3-4. PCM Data Flow Transmit and Receive Data (Transmit Data on Negative PCLK Edge)



3.1.2 Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) block communicates with external VoIP processors over a flexible half-duplex synchronous serial interface. This port is always a peripheral to the host processor's SPI port which provides clocking, chip select and initiates transactions.

3.1.2.1 SPI Signals

The SPI port physically consists of a serial data input (DIN) serial data output (DOUT), a data clock (DCLK), and a chip select (CS).

Table 3-2. SPI Interface Signals

Signal Name	Type	Description
DCLK	Input	Serial Clock
$\overline{CS}$	Input	Chip Select, active low
DOUT	Output	Host Input Peripheral Output
DIN	Input	Host Output Peripheral Input

3.1.2.2 Interrupt Signal

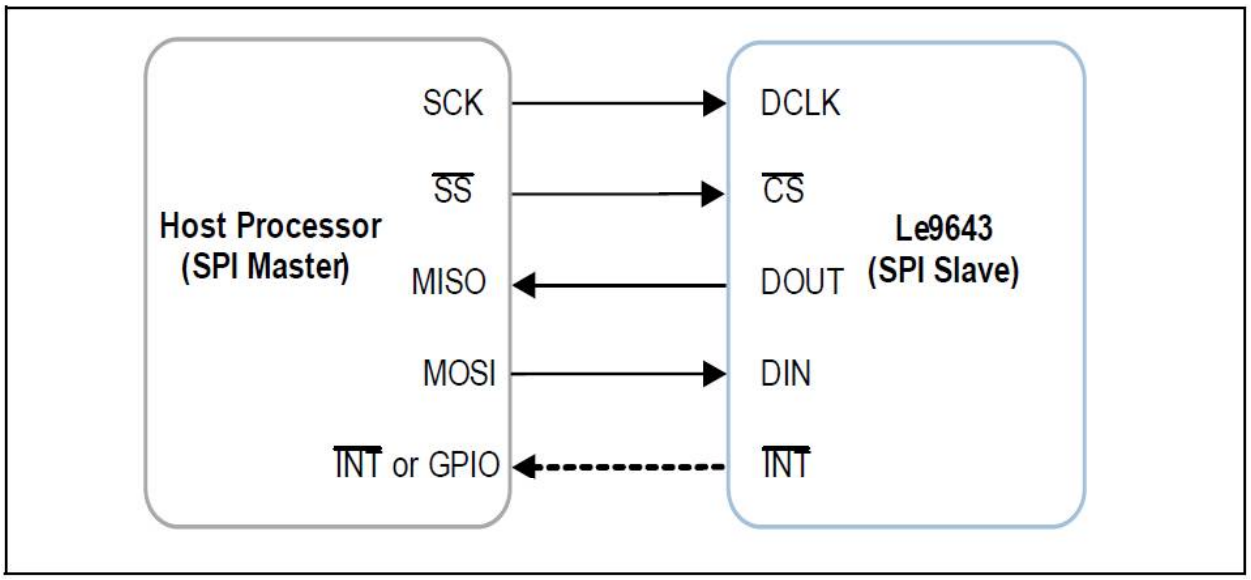
An optional interrupt signal ($\overline{INT}$) is available to alert the host processor that the device has status information. It is recommended that the $\overline{INT}$ signal be tied to an interrupt-generating pin on the host processor. If the interrupt signal is not used, the host processor will need to regularly poll the device.

The signal on the $\overline{INT}$ pin is available even in ZSI mode. This supports a system wake up even if the ZSI interface is powered down.

3.1.2.3 SPI Connection Diagram

The figure below shows the standard 4-Wire SPI connection to the host processor. The optional INT signal is also shown here.

Figure 3-5. SPI Connection to Host Processor



The Le9643 device also supports 2- and 3-Wire variants of the SPI interface in case of limitations on the host's serial port. Contact *Microchip* for more information.

3.1.2.4 Chip Select Settings

Three chip select settings are supported:

1. Low for each Byte or Word: $\overline{CS}$ goes inactive between bytes or words. This mode is compatible with the legacy MPI mode.
2. Command Framing: $\overline{CS}$ goes inactive on some command boundaries. Commands cannot be aborted in this mode. All required bytes are expected even if $\overline{CS}$ is de-asserted in the middle.
3. CS Hard-Wired Low: This can be used when the Le9643 device is the only device on the SPI bus, but additional measures are required to acquire synchronization if it is ever lost.

Whenever $\overline{CS}$ goes inactive the bit state machine is reset. Also, if $\overline{CS}$ has not been active for *exactly* a multiple of 8 bit times, any byte which was partially received when $\overline{CS}$ goes inactive is ignored.

3.1.2.5 DCLK Polarity and Phase Settings

The SPI standards include four modes, defined by the polarity of DCLK and the phase relationship between data and DCLK. The clock polarity (CPOL) is determined by the idle state of DCLK. If the idle state is low, CPOL is 0. If the idle state is high, CPOL is 1. The clock phase (CPHA) is determined by which edge that data is valid. If the data is valid on the first edge of DCLK, CPHA is 0. If the data is valid on the second edge of DCLK, CPHA is 1.

The Le9643 device supports SPI Modes 0 (CPOL =0 and CPHA = 0) and 3 (CPOL =1 and CPHA = 1) and contains a logic block to automatically conform to the selected Mode. SPI Modes 1 (CPOL =0 and CPHA = 1) and 2

(CPOL =1 and CPHA = 0) are not supported.

Since the host processor is the controller, it must place DCLK in the proper idle state before $\overline{CS}$ is asserted.

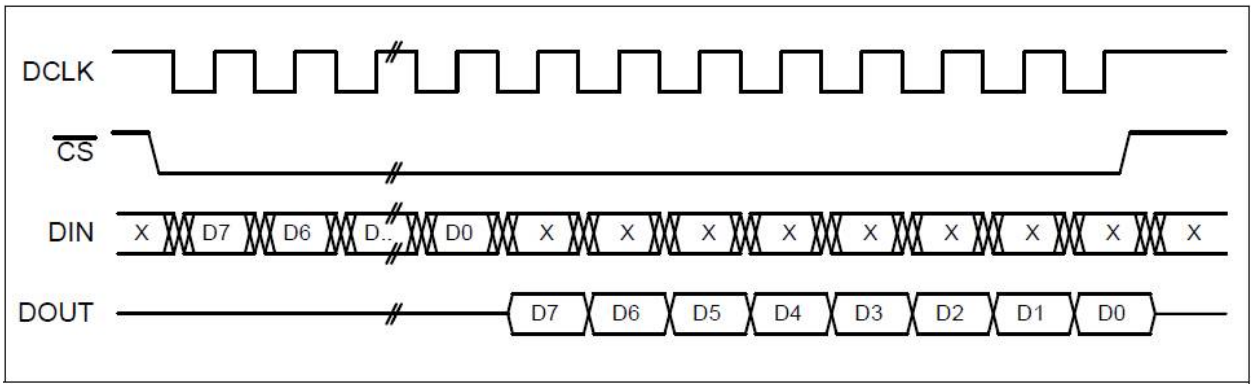
3.1.2.6 Length of Data Transactions

The SPI port on the Le9643 device supports 8-bit (byte-wide) transactions. 16-bit transactions are not supported.

3.1.2.7 SPI Interface Timing

The figure below shows a typical timing interface diagram for SPI Mode 3.

Figure 3-6. SPI Mode 3 Interface Timing



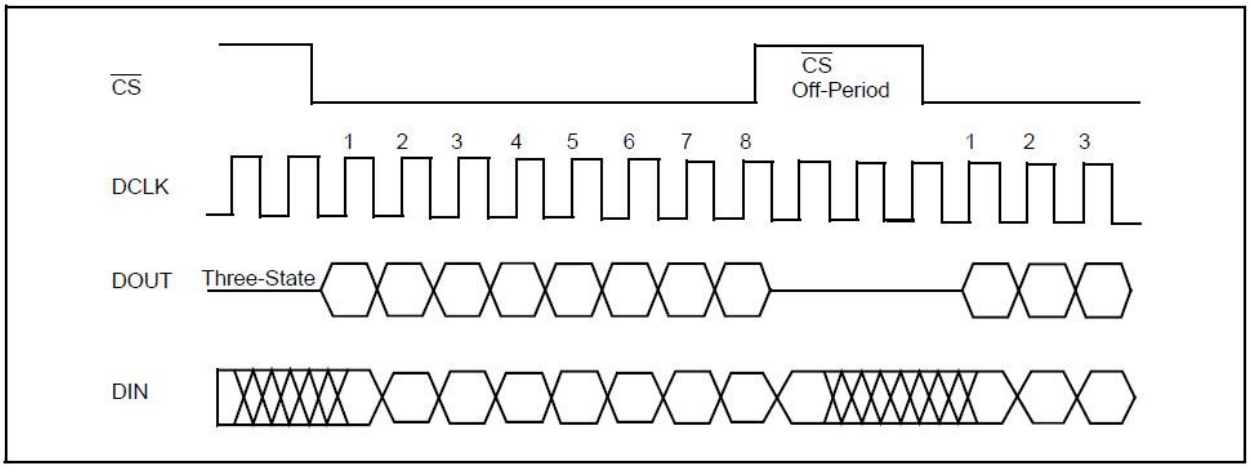
3.1.2.8 MPI Interface

The Microprocessor Interface (MPI) is essentially a 4-Wire SPI Mode 3, with $\overline{CS}$ low for each byte and 8-bit data transactions. With the MPI interface, 8-bit commands can be followed with additional bytes of input data, or can be followed by the Le9643 device sending out bytes of data. All data input and output is MSB (D7) first and LSB (D0) last. All data bytes are read or written one at a time, with $\overline{CS}$ going high for at least a minimum off period before the next byte is read or written. Only a single channel should be enabled during read commands.

All commands that require additional input data to the device must have the input data as the next N words written into the device (for example, framed by the next N transitions of $\overline{CS}$). All unused bits must be programmed to 0 to ensure compatibility with future parts. All commands that are followed by output data will cause the device to output data for the next N transitions of $\overline{CS}$ going low. The Le9643 device will not accept any commands until all the data has been shifted in or out. The output values of unused bits are not specified.

The figure below shows an example MPI mode interface timing, with DOUT changing on the negative edge of DCLK. DIN is sampled on the rising edge of DCLK.

Figure 3-7. MPI Interface Timing



An MPI cycle is defined by transitions of $\overline{CS}$ and DCLK. If the $\overline{CS}$ lines are held in the high state between accesses, the DCLK may run continuously with no change to the internal control data. Using this method, the same DCLK can be run to a number of Le9643 devices and the individual $\overline{CS}$ lines will select the appropriate device to access. Between command sequences, DCLK can stay in a static state indefinitely with no loss of internal control information regardless of any transitions on the $\overline{CS}$ lines. Between bytes of a multi byte read or write command sequence, DCLK can also stay in a static high state indefinitely. If the host controller has a single bidirectional serial data pin, the DOUT pin of the Le9643 device can be connected to its DIN pin.

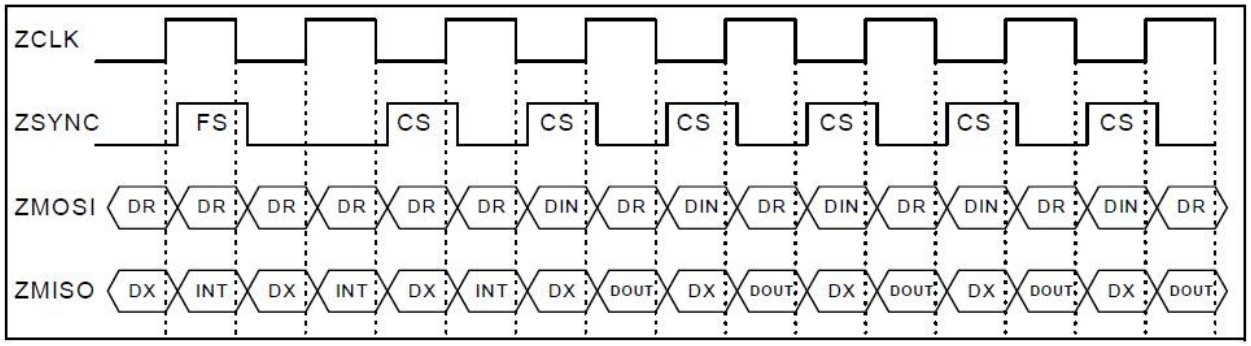
If a low period of $\overline{CS}$ contains less than 8 positive DCLK transitions, it is ignored. If it contains 8 or more positive transitions, the first 8 transitions will be interpreted as the first byte and the next 8 transitions will be treated as the second byte, etc. This allows the chip select input to be tied low permanently if desired.

3.1.3 ZSI Timing

The figure below shows the protocol for multiplexing PCM and control signals onto the ZSI.

Note: The chip select must be de-asserted at least one clock between bytes or a reset will be generated after 16 clocks.

Figure 3-8. ZSI Timing Protocol

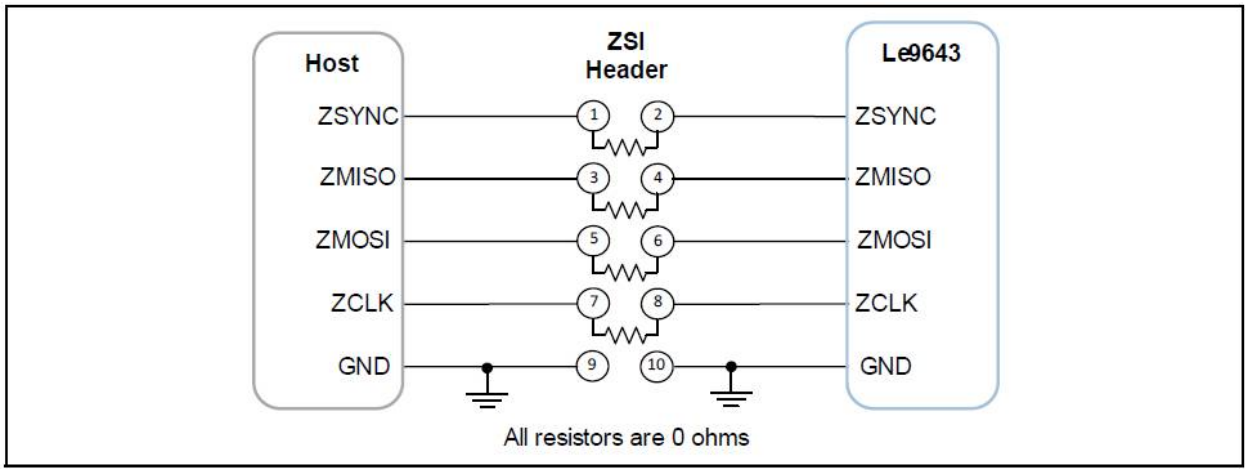


3.2 ZSI Header

The ZSI port consists of the ZSYNC, ZMISO, ZMOSI, and ZCLK pins. Microchip can provide a ZSI Snooper board that can demux and provide access to the ZSI interface. If access to this port is desired, a header footprint should be added to the system board.

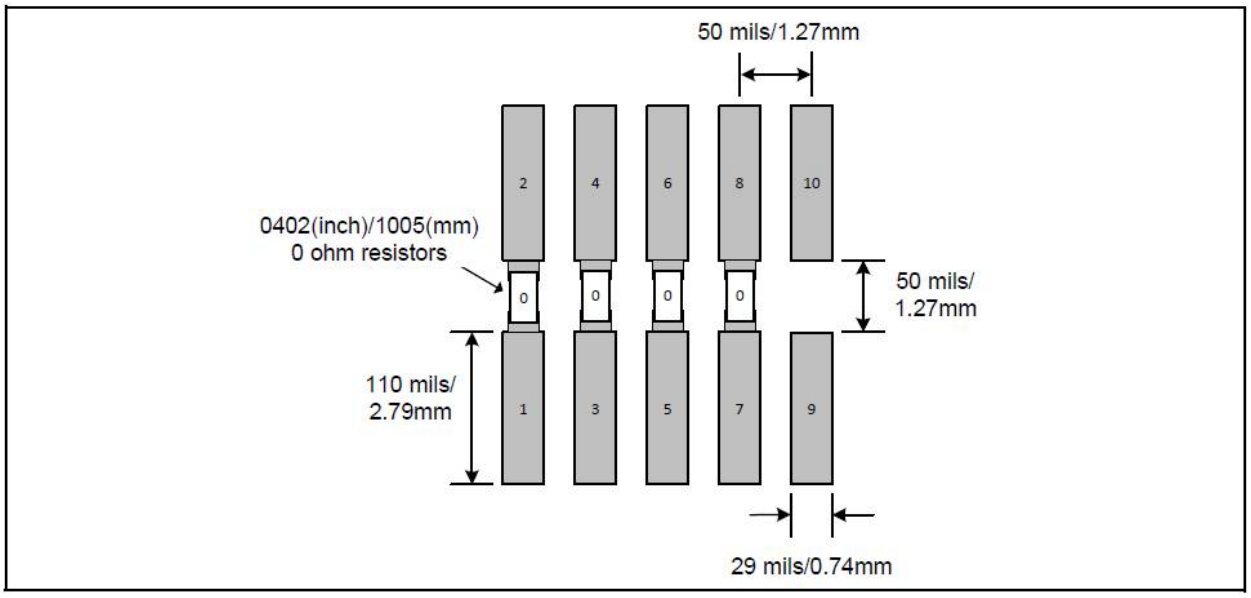
The following figure shows the pin out for the ZSI header. For normal operation the 0 ohm resistors short the header. If the header is to be used, the 0 ohm resistors must be removed and replaced with the header.

Figure 3-9. ZSI Header



The following figure depicts the ZSI header land pattern that needs to be added to the circuit board. The land pattern is designed for a Samtec FTSH-105-01-L-DV-K vertical 10-position, surface mount micro header. The 10-pin header mating pins are spaced 1.27 mm row to row and 1.27 mm column to column. Four 0 ohm resistors are shown shorting the header. A 0402 inch / 1005 mm resistor will fit between the surface mount land pattern pads as illustrated in the figure.

Figure 3-10. ZSI Header Land Pattern with 0 Ohm Resistors



3.3 Input/Output Block

The Le9643 device features a general purpose input/output pin. VS/IO can be configured as a general purpose digital; input or output (I/O) or as a voltage sense pin (VS).

3.3.1 Voltage Sense

The voltage sense block allows the measurement of analog voltage at pin VS, when the pin is configured as an analog input. This makes it possible, for example, to monitor VSW in real time and make switcher optimizations based on its level. An external 1.0MΩ 1% resistor needs to be connected between this pin and the voltage to be measured.

3.4 Voice Signal Processor

This block, as shown in the figure below, performs digital signal processing for the transmission and reception of voice. It includes *G.711* compression/decompression, impedance matching, filtering, gain scaling, DTMF generation and general-purpose tone generators. Additionally Caller ID (FSK and DTMF) and metering generation are provided.

This block performs the codec and filter functions associated with the four-wire section of the subscriber line circuitry in a digital switch. These functions involve converting an analog voice signal into digital PCM samples and converting digital PCM samples back into an analog signal. During conversion, digital filters are used to band-limit the voice signals.

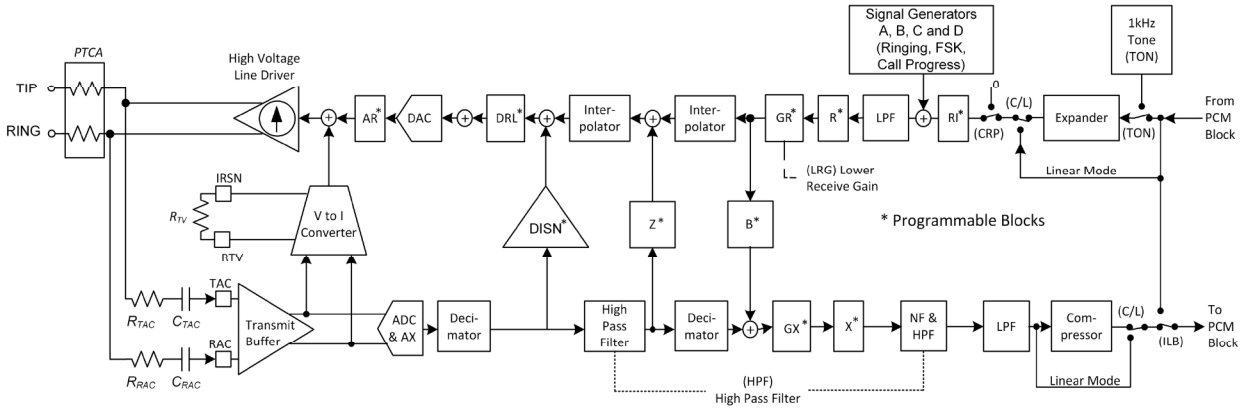
The user-programmable filters perform the following functions:

- Sets the receive and transmit gain
- Performs the transhybrid balancing function
- Permits adjustment of the two-wire termination impedance
- Provides frequency attenuation adjustment (equalization) of the receive and transmit paths

Country-specific and standards-specific *Profiles* are available from Microchip with pre-computed digital filter coefficients.

The Le9643 device is architected in such a way as to reduce the real time demands on the host processor. An integrated cadencer/sequencer controls ringing and call progress tone generation. This feature can also generate timed interrupts and substantially reduces the user's need to implement time critical functions.

Figure 3-11. Voice Signal Processing Block Diagram



3.4.1 Impedance Synthesis

The analog impedance synthesis loop is comprised of the SLIC block, the AC sense path components, the transmit amplifier, and a voltage to current converter. An external resistor, R_{TV}, synthesizes the nominal impedance in the analog domain. Additional refinement of the impedance is done in the DSP via the Digital Impedance Scaling Network (DISN) and Z-blocks.

The DISN path is comprised of the voice A/D and its first stage of decimation, a DISN, and the voice DAC. The 8-bit DISN synthesizes a portion of the AC impedance which appears in parallel with R_{TV} and is used to modify the impedance set by the external analog network.

The Z Filter is a programmable digital filter providing an additional path and programming flexibility over the DISN in modifying the transfer function of the synthesis loop. Together R_{T1}, DISN, and the Z Filter enable the user to synthesize virtually all required telephony device input impedances.

3.4.2 Frequency Response Correction and Equalization

The voice signal processor contains programmable filters in the receive (R) and transmit (X) directions that may be programmed for line equalization and to correct any attenuation distortion caused by the Z Filter.

3.4.3 Transhybrid Balancing

The voice signal processor's programmable B Filter is used to adjust transhybrid balance. The filter has a single pole Infinite Impulse Response (IIR) section and an eight-tap Finite Impulse Response (FIR) section, both operating at twice the sampling rate.

3.4.4 Gain Adjustment

The transmit path of the FXS has two programmable gain blocks. Gain block AX is an analog gain of 0 dB or 6.02 dB (unity gain or gain of 2.0), located immediately before the A/D converter. GX is a digital gain block that is programmable from 0 dB to +12 dB, with a worst-case step size of 0.1 dB for gain settings below +10 dB, and a worst-case step size of 0.3 dB for gain settings above +10 dB. The filters provide a net gain in the range of 0 dB to 18 dB. The receive voice path has three programmable gain blocks. GR is a digital loss block that is programmable from 0 dB to 12 dB, with a worst-case step size of 0.1 dB. DRL is a digital loss block of 0 dB or 6.02 dB. AR is an analog gain of 0 dB or 6.02 dB (unity gain or gain of 2) or a loss of 6.02 dB (gain of 0.5), located immediately after the D/A converter. This provides an attenuation in the range of 0 dB to 18 dB.

The gain adjustment block can also be accessed by a *VP-API-II* function directly, without using an *AC FXS Profile*.

Table 3-3. VP-API-II Functions for Gain Adjustment

Function Name	Description
`VpSetRelGain()`	Adjusts transmit and/or receive gain up to +/-6 dB. Relative gain of 1 (0 dB) defined as initial value programmed by *AC FXS Profile*. Note that the supplied *AC FXS Profiles* have initial gains of -6 dBr receive and 0 dBr transmit.

.....continued	
Function Name	**Description**
VpSetOption()	VP_OPTION_ID_ABS_GAIN -- Programs absolute gain.

3.4.5 Transmit Signal Processing

In the transmit path (A/D) of the FXS, the AC Tip - Ring analog input signal is sensed by the TAC and RAC pins, buffered, amplified by the analog AX gain and sampled by the A/D converter, filtered, companded (for A-law or µ-law), and made available to the PCM blocks. If linear format is selected, the 16-bit data will be transmitted in two consecutive time slots starting at the programmed time slot. The B, X, and GX digital filter blocks are user-programmable digital filter sections. The first high-pass filter is for DC rejection, and the second high pass and notch filters reject low frequencies such as 50 Hz or 60 Hz.

3.4.6 Receive Signal Processing

In the receive path (D/A) of the FXS port, the digital signal is expanded (for A-law or µ-law), filtered, interpolated, converted to analog, and driven onto TIP and RING by the SLIC block. The AR, DRL, DISN, Z, R, and GR blocks are user-programmable filter sections.

3.4.7 Speech Coding

The A/D and D/A conversion follows either the A-law or the µ-law standard as defined in *ITU-T Recommendation G.711*. Alternate bit inversion is performed as part of the A-law coding. Linear code is an option on both the transmit and receive sides of the device. Two successive time slots are used for linear code operation. The linear code is a 16-bit two's-complement number with sign bit first.

3.4.8 Wideband Operation

The Le9643 device can be set to operate in either Narrowband or Wideband mode under *VP-API-II* software control. In the Wideband mode, the nominal voice bandwidth is expanded to provide better voice quality. The 50/60 Hz notch filter can be disabled to support the full wideband range of 150 Hz to 6800 Hz. The *AC FXS Profiles* must be programmed with wideband coefficients. In the Wideband mode, the increased data rate is processed by accessing a second set of timeslots equally spaced in the frame.

Table 3-4. VP-API-II Functions for Speech Coding

Function Name	Description
VpSetOption()	VP_OPTION_ID_TIMESLOT -- Programs transmit and receive timeslot. VP_OPTION_ID_CODEC -- Programs speech coding mode.
VpGetOption()	VP_OPTION_ID_TIMESLOT -- Retrieves current values of transmit and receive timeslot. VP_OPTION_ID_CODEC -- Retrieves current speech coding mode.

3.5 Signal Generation

Up to four programmable digital signal generators are available for the FXS channel. These signal generators can be programmed for multi-tone generation, amplitude and frequency modulation, and or the generation of complex sine, triangular or trapezoidal signals.

3.5.1 Multi-Tone Generation

In this configuration, up to four tone generators are summed into the output path, as shown in the following figure. The Bias generator produces a DC bias that can be used to provide DC offset during ringing or DC test signals during diagnostics. This generator is automatically enabled when entering the VP_LINE_RINGING state.

Figure 3-12. Multi-Tone Generation

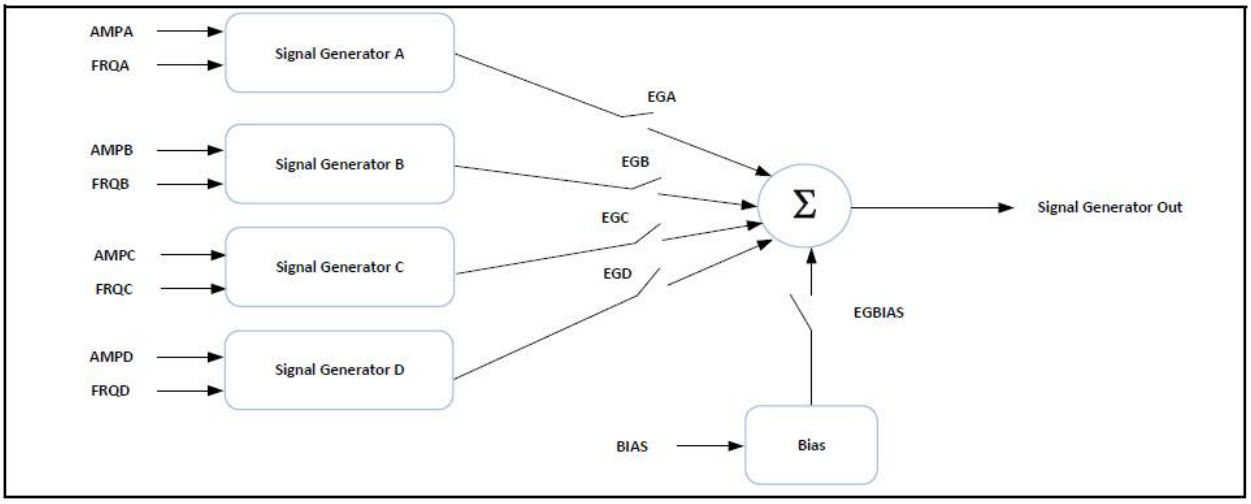


Table 3-5. VP-API-II Functions Using Signal Generators

Function Name	Description
`VpSetLineTone()`	Provides simultaneous generation of up to four tones. Note that with Tone Cadencing, tones can be enabled/disabled individually to provide Special Indication Tone (SIT).
`VpSetLineState()`	`VP_LINE_RINGING` and `VP_LINE_RINGING_POLREV` -- Uses Signal Generator A (and B for trapezoidal type ringing) with user selected frequency, offset, amplitude, and type.
`VpSendSignal()`	`VP_SENDSIG_DTMF_DIGIT` -- Generates a DTMF digit on the line.
`VpInitCid()`	Sending Caller ID (FSK and DTMF message data supported) on an FXS line. Providing Type 2 CID Alerting tone.
`VpSendCid()`	
`VpContinueCid()`	

Signal Generator A is also used by the Microchip *VeriVoice* test suites to produce slow ramps. This allows a complex sequence of diagnostic test voltages to be generated in a controlled manner without generating unwanted transients on the line.

Each generator has independent frequency and amplitude parameters. The frequency accuracy is basically the same as the crystal accuracy of the system.

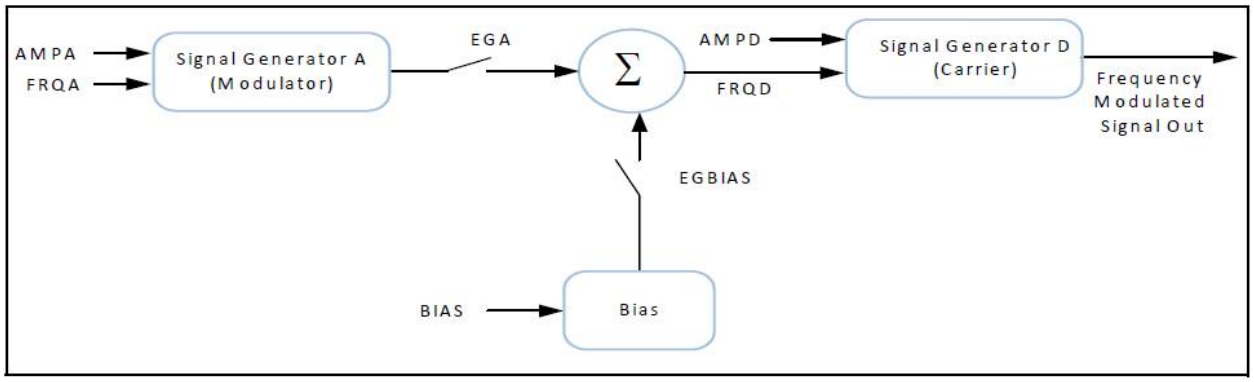
The EGA/B/C/D bits are controlled by the *VP-API-II* Cadencing engine.

3.5.2 Frequency and Amplitude Modulation

The signal generators can also be used to generate frequency-modulated and/or amplitude-modulated tones in conformance with worldwide Howler (receiver off-hook) and call progress tone requirements. Frequency modulation is performed in a dedicated hardware block, while amplitude modulation is performed in software by *VP-API-II*.

To generate frequency-modulated tones, Signal Generator A is configured as a modulator, while Signal Generator D is configured as a carrier. The output of Signal Generator A is the frequency input to Signal Generator D. Note that Signal Generator A needs a positive DC bias so that its output is always positive. Caller ID generation is not available while frequency modulation is taking place. The following figure shows the configuration for modulation. Note that Signal Generators B and C are available to be summed to the frequency-modulated signal, if necessary.

Figure 3-13. Frequency Tone Modulation



Frequency and amplitude modulation allow the Le9643 device to meet exacting Howler tone requirements such as those specified in *BTNR 1080 Version 15* and *Draft 960-G*, *NTT Edition 5* and *Austel AUS002:2001*.

The table below lists the *VP-API-II* functions that are used for Howler tone generation.

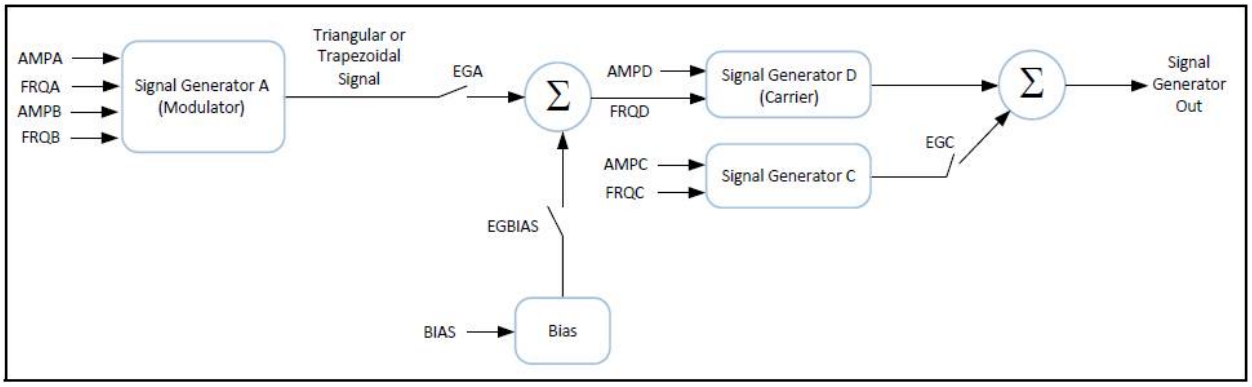
Table 3-6. VP-API-II Functions for Howler Tone Generation

Function Name	Description
`VpSetLineState()`	`VP_LINE_HOWLER` -- Places the device in a high gain state for Howler tone generation.
`VpSetLineTone()`	Provides simultaneous generation of up to four tones. Note that with Tone Cadencing, tones can be enabled/disabled individually or modulated in order to generate Howler tones.

3.5.3 Triangular and Trapezoidal Signal Generation

The signal generators can also be used to generate trapezoidal waveforms for ringing. The following figure shows a configuration that is typically used to generate trapezoidal waveforms. Triangular waveforms can also be generated.

Figure 3-14. Trapezoidal Signal Generation



3.6 Low Power DC Feed

The Le9643 device supports *Low Power Idle Mode (LPIM)*, which reduces the system power consumption during idle (On-Hook) state. *LPIM* provides a weak DC feed capable of at least 5 mA to the line and reacts to a change in the line voltage to create an off-hook indication when a telephone goes off-hook.

3.7 Normal DC Feed

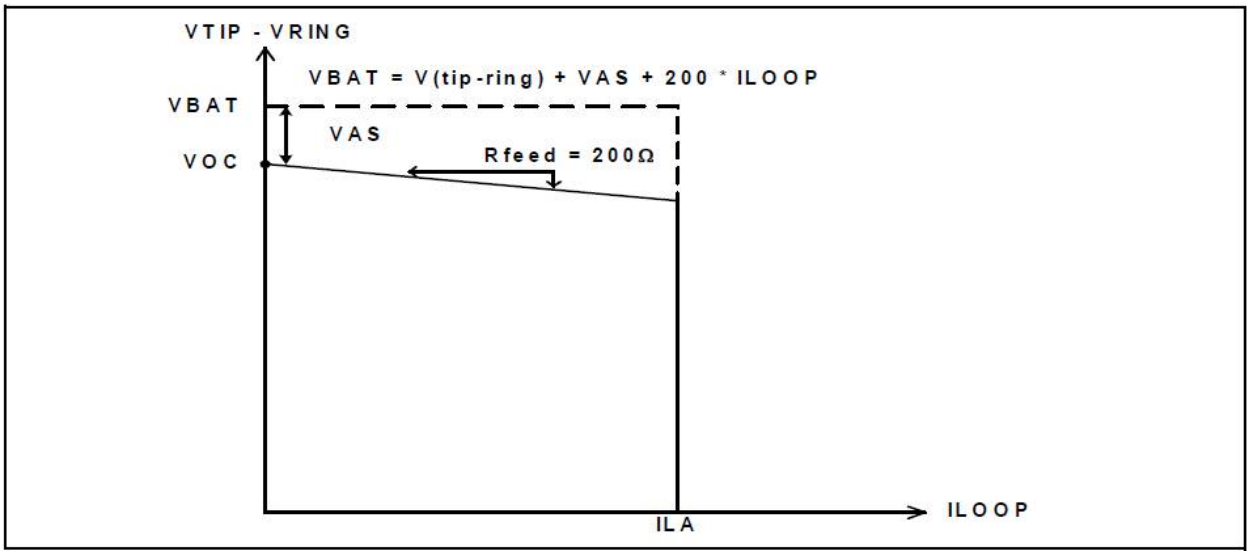
DC feed is active in normal idle, talk and ringing states and the programmed characteristics appear between Tip and Ring. VAS is chosen to ensure that sufficient headroom is available for the amplifiers when on-hook to support on-hook transmission with the programmed open circuit (VOC) voltage. Values programmed in device for VAS, VOC, and ILA are determined during `VpCalLine()` to ensure circuit performance. Please refer to the Active State I / V Characteristic figure for the Active state I/V characteristic feed curve for Rfeed = 200 Ω.

The *DC Profile* produces a DC feed curve at Tip and Ring when the fuse resistors are inside the feedback loop formed by the RTDC and RRDC feedback network. Note that the value of the combined Tip and Ring feed resistors Rfeed is programmable to 0, 50, 100, or 200 Ω to correspond to the choice of PTCs or fuse resistors that are used. Refer to the Figure 10-3. Profile Wizard – DC Profile Configuration Example for more details.

3.8 Tip Open Feed

The Tip Open test state presents the DC feed characteristic between the Ring lead and ground as shown the figure below.

Figure 3-15. Active State I / V Characteristic



3.9 Ringing

In this state, the voice DAC is used to apply the ringing signal and bias to the high voltage line driver. Internal feedback maintains a low system output impedance during ringing and the current limit is increased in the Ringing state. In order to minimize line transients, entry and exit from the Ringing states are intelligently managed by the Le9643 device. The Le9643 supports balanced ringing.

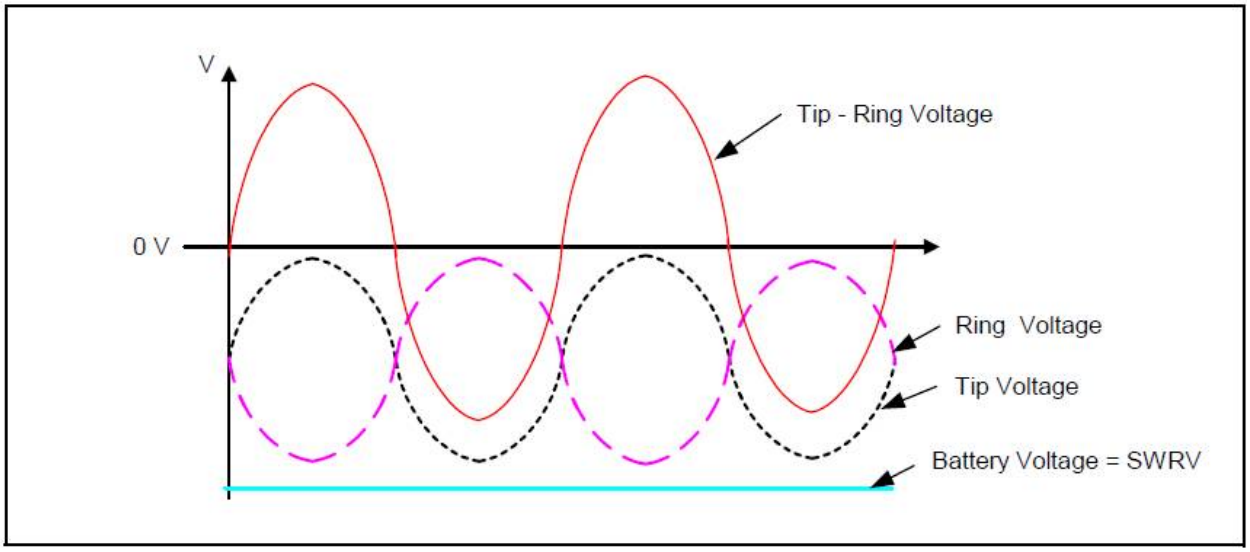
3.9.1 Balanced Ringing

Internal balanced ringing drives the subscriber line with balanced ringing voltage waveforms.

The Buck-Boost supply uses a fixed supply with ringing as shown in the following figure. The Inverting-Boost switcher circuit can also be operated with a fixed voltage during ringing.

The Le9643 device can be programmed to output either sinusoidal or trapezoidal ringing waveforms. The ringing signal is driven differentially, thus maximizing the ringing signal swing. In this mode, the SLIC appears to the subscriber line as a voltage source with an output impedance of 200 Ω.

Figure 3-16. Balanced Ringing with Fixed Supply



3.9.2 Adaptive Ringing Amplitude

The Le9643 device supports adaptive ringing amplitude. Adaptive ringing amplitude limits the maximum power that is generated during ringing at or below a specified level.

3.9.3 Switch Hook Detection

The FXS supervision circuits of the Le9643 device provide debounced off-hook indications to an external processor via the host port interface. The supervision circuit compares a scaled version of the Tip-Ring current to a programmed off-hook threshold, TSH. The output of the comparator is debounced by a programmable debounce timer, DSH. A debounced off-hook indication generates an interrupt to the host processor.

3.9.4 Ring Trip Detection

Ring trip is the process of sensing a subscriber's off-hook event during ringing. This is accomplished by sensing the rise in loop current which occurs when a phone goes off-hook. The Le9643 device can detect ring trip when the ringing signal is purely AC and/or when the ringing signal has a DC bias on it. To do so, the ring trip algorithm is automatically altered internally by the Le9643 device based on the user-programmed parameters.

The ring trip detector uses the Tip-Ring current as an input. This current is rectified so that AC + DC ring trip can be detected. The output of the rectified signal is compared to a programmable ring trip threshold and the output is digitally debounced. The output is blanked upon ring entry to avoid false ring trips.

The ring trip detection circuit provides debounced ring trip indications to an external processor via the host port interface. The ring trip circuit compares a scaled version of the Tip-Ring current to a programmed Ring Trip Threshold (RTTH). The output of the comparator is processed by the ring trip algorithm on a cycle by cycle basis to provide immunity to false ring trips. In addition, spending more than 50% of the time in ringing current limit will generate a trip indication. A positive ring trip occurs if a trip indication is present for one (optional) or two (default) complete ring cycles, and an interrupt can be raised to the host processor. For AC-only ringing, the signal is half- wave rectified.

The Ring Trip Threshold (RTTH), integration method (positive half-wave for AC only or full-wave for AC+DC), the number of cycles (1 or 2), and Ringing Current Limit (ILR) are programmed in the *Ringing Profile*. Microchip provides a number of example *Ringing Profiles* for most common ringing requirements incorporating the ringing signal parameters and corresponding ring trip settings.

The following equations can be used to select new ring trip settings when using different ringing waveforms and different loads. They allow the ratio of the open circuit ringing voltage to the ringing threshold current to vary by +/-20%, which is conservative.

Table 3-7. Ring Trip Parameters

Name	Description
AMPA	Amplitude of signal generator A which is used for ringing.
FREQA	Frequency of signal generator A which is used for ringing.
BIAS	DC bias for ringing.
RTDCAC	Ringing trip based on AC only or Battery Backed (DC) Ringing.
RTTH	Ringing trip threshold in 0.5 mA steps from 0 to 63.5 mA.
ILR	Ringing current limit programmed in 2 mA steps. ILR=0 represents 50 mA. ILR = 31 represents 112 mA.
HOOK	Interruption in signaling register indicating a ring trip occurrence.

For AC only ringing, RTDCAC is 1 and the ringing current is half-wave rectified and averaged over a ringing cycle. If this result exceeds the RTTH threshold for two successive cycles, the HOOK bit will be set. This method limits the supported loop length x depending on the minimum must not trip ringing impedance (Rmnt in Ohms) and allowing for errors in the applied ringing voltage and trip level. The maximum loop resistance is given by:

$$\mathbf{RLOOP(max) = 0.67xRmnt - Rphone - 66\Omega}$$

RLOOP (max) excludes the DC resistance of the phone (Rphone, typically 430 Ω in the U.S.), and the fuse resistance if DC line sensing is behind the fuse resistors.

For a sinusoidal ringing waveform of VRING (RMS) volts, and Rmnt impedance, the following ring trip settings should be used:

$$RTTH = \frac{0.54xVRING}{Rmnt + 200\Omega}$$

$$ILR = \frac{1.4xVRING}{Rmnt + 200\Omega}$$

In general for short loop applications, it is recommended to use AC ring trip even in the presence of a DC bias that could allow a DC based ring trip, and the above equations still apply. Note that the ringing source impedance is nominally 200 Ω.

3.10 Subscriber Line Testing

The Le9643 device provides the ability for the user to perform the *Telcordia GR-909-CORE / TIA-1063* diagnostic testing for the voice ports. In Test mode, a variety of input signals can be read from the voice ADC converter. These signals include the switching regulator voltage and the line DC and AC voltages.

3.10.1 VeriVoice Professional Test Suite Software

VeriVoice Professional Test Suite Software is an advanced test suite featuring the following tests as described in the table below.

Table 3-8. VeriVoice Professional Test Suite list of Tests

Test	Description
Line Voltage	Checks for hazardous and foreign AC and DC voltages.
Receiver Off-Hook	Checks for longitudinal fault, off-hook resistive fault and receiver off-hook.
Regular REN	Tests the impedance of the line and returns a fail if the Ringer Equivalence Number (REN) is too low or high.
Electronic REN	Provides REN Tip to Ring, Tip to ground and Ring to ground based on capacitance.
Resistive Fault	Measures three-element resistance.
GR-909-CORE / TIA-1063	Performs all of the GR-909-CORE outward tests in the correct sequence.
Capacitance	Measures three element capacitance.
Master Socket	Detects master socket terminations.
Cross Connect	Detects cross connected FXS.
Loop back	Enables receive-to-transmit signal loop-back using two different methods.
Read Loop Conditions	Measures DC voltages between Tip and Ring, Tip to ground, Ring to ground, and VBAT to ground. Also measures metallic and longitudinal DC line currents in supported States.
Read Battery Conditions	Reads the battery voltages connected to the line circuit.
DC Voltage Self-Test	Verifies that the line circuit has the ability to drive the voltage ranges required for the normal operation of the line circuit.
DC Feed Self-Test	Measures the voltage and current across a known internal test termination using the DC Profile that has been programmed.
Ringing Self-Test	Verifies ring signal generation, drive capability, and ring trip.
On/Off-Hook Self-Test	Creates on-hook and off-hook conditions on the line using the internal test termination and verifies that they are properly reported.
Draw and Break Dial Tone	Verifies the capability of the line circuit to detect off-hook and on-hook as well as the voice path to/from the host.
Read Loop Conditions - Extended	Reads the loop conditions of the current state of the line without disturbing the T/R feed conditions. Measures AC and DC voltages Tip and Ring, Tip to ground and Ring to ground. Measures VBAT to ground. Also measures metallic and longitudinal AC and DC line currents in supported States.

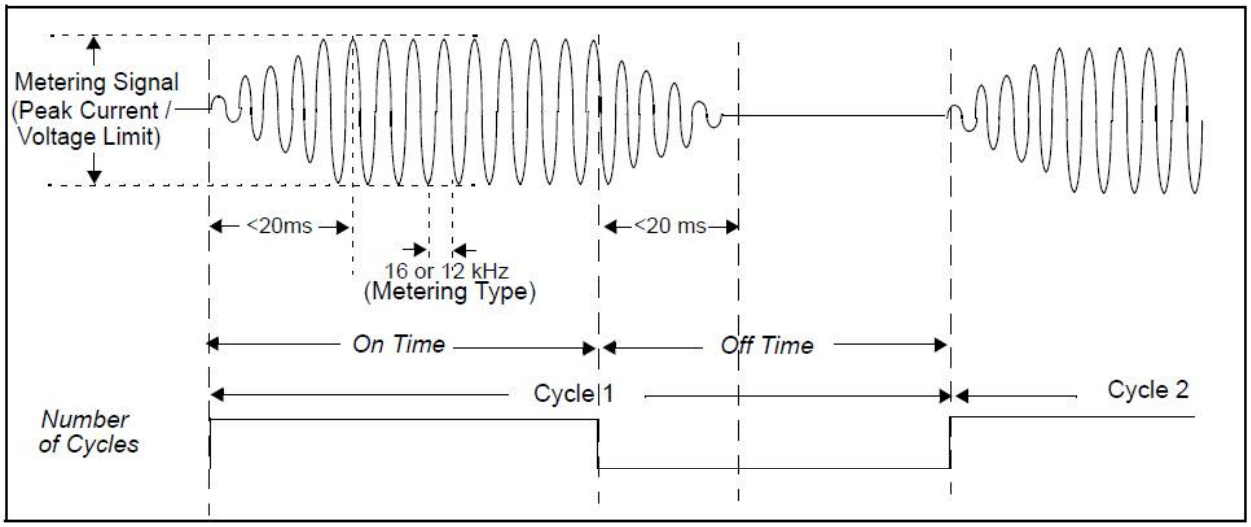
3.11 Manufacturing Testing

The Le9643 is supported by the *VeriVoice Manufacturing Test Package (VVMT),* a platform independent source code module which facilitates factory testing and calibration of assembled boards.

3.12 Metering

The Le9643 device can produce 0.5 V_{RMS} metering into a 200 Ω metering load at either 12 kHz or 16 kHz. Smooth and abrupt metering applications are supported. A typical metering sequence is shown in the figure below.

Figure 3-17. Metering Pulse Definitions



The metering on time, off-time, and number of cycles are programmed in the *VP-API-II* function `VpStartMeter()`. This off-loads much of the timing from the host processor. Note that a ramp up / ramp down period of up to 20 ms is possible. The metering type (12 or 16 kHz), peak current and voltage limit are set in the *Metering Profile* and are used by the *VP-API-II* function `VpInitMeter()`. Note that in a normal configuration, some of the metering current flows into the CTD and CRD capacitors, so that the current sourced into an external load will be less than that programmed peak current parameter even when the metering voltage limit is not reached. The metering voltage at the load is also dependent on the total fuse resistance and the minimum load resistance (typically 200 Ω).

3.13 Switching Regulator Controller

The switching regulator controller and the external power train circuitry provide a flexible switching regulator that automatically produces the negative supply voltage required to drive the line.

A Buck-Boost fixed tracker switching regulator circuit capable of up to 85-VPK ringing is shown in the Buck-Boost Switching Regulator Circuit section. An Inverting-Boost switching regulator circuit also capable of up to 85-VPK ringing is shown in the Inverting-Boost Switching Regulator Circuit section. The Inverting-Boost switching regulator circuit has a lower BOM cost. Both topologies operate at similar efficiency levels.

The tracking switching regulator has a variable output for DC feed. An offset voltage (set by the VAS DC feed parameter) is added to the measured Tip-Ring voltage when on-hook and the resulting signal controls the output of the switching regulator. When loop current is drawn in the Active or Ringing states, an additional offset defined as Rfeed * Iloop is added, to ensure overhead is maintained with up to 160 Ohms of total fuse resistance present in the DC feed loop. This architecture enables the switching regulator output voltage to generate the required voltage to feed the line whether in the on-hook, off-hook or ringing states. The result is maximum power efficiency and minimum power consumption in all DC feed states because the regulator output is always optimum for the current state.

Three baseline levels need to be set for switching regulator operation. The first is the Battery Floor Voltage, this limits how low the power supply will drop when driving very short loops. Typically this is set to -25 V for US applications to ensure compatibility with Call Waiting Caller ID (CWCID) equipment that performs a momentary extension check (MEC). International applications typical have a lower floor voltage, such as -20 V. The second is the Open Circuit Voltage (VOC) which is used for Low Power Idle Mode -48 V. The third sets a fixed ringing voltage mode. In this case the power supply ramps up to a pre-programmed voltage that is sufficient to support the programmed ringing waveform just before entering the ringing state. The Battery Floor Voltage and the Open Circuit Voltage are set in the *DC Profile*, while the ringing voltage is set in the *Ringing Profile*. These voltages should be calibrated by the *VP-API-II* software `VpCalLine()` function.

The switching regulator has three modes of operation: Low, Medium, and High, which roughly correspond with On-Hook, Off-Hook, and Ringing states. These modes of operation provide for increased efficiency over a wide load range. Each mode is frequency and duty cycle programmable. Switching regulator parameters are set in the *Device*

Profile. In addition, the controller detects over current events and terminates the output pulse on a cycle by cycle basis.

For Buck-Boost operation the VDDSW pin needs to be tied to DVDD (+3.3 V). For Inverting-Boost operation the VDDSW pin needs to be tied to +5.0 V.

The Le9643 has built-in undervoltage lock-out circuitry on VDDSW and VDD supply inputs. This circuitry provides stable on/off operating voltages for the switching regulator circuitry so that the circuitry can properly drive and control an external transistor.

4. Electrical Specifications

4.1 Absolute Maximum Ratings

Stresses above those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 4-1. Stress Parameters and Thresholds

Stress Parameter	Threshold Level
Storage Temperature	-55°C < T_A < +125°C
Ambient temperature, under Bias	-40°C < T_A < +85°C
Ambient relative humidity (non condensing)	5 to 95%
$VBAT_1$ voltage with respect to GND	-100 V_{DC} to +0.5 V_{DC}
AVDD, DVDD, voltages with respect to GND	-0.4 V_{DC} to +4.0 V_{DC}
AVDD voltage with respect to DVDD	-0.4 V_{DC} to +0.4 V_{DC}
VDDSW voltage	-0.4 V_{DC} to +5.5 V_{DC}
IDDSW current	200 mA
$TIPD_1$ or $RINGD_1$ voltage with respect to GND (continuous)	$VBAT_1$ – 1 V_{DC} to + 1 V_{DC}
$TIPD_1$ or $RINGD_1$ voltage with respect to GND (10 ms, F = 0.1Hz)	$VBAT_1$ – 5 V_{DC} to + 5 V_{DC}
$TIPD_1$ or $RINGD_1$ voltage with respect to GND (1 µs, F = 0.1Hz)	$VBAT_1$ – 10 V_{DC} to + 10 V_{DC}
$TIPD_1$ or $RINGD_1$ voltage with respect to GND (250 ns, F = 0.1Hz)	$VBAT_1$ – 15 V_{DC} to + 15 V_{DC}
$TIPD_1$ or $RINGD_1$ current (continuous)	±150 mA
$TIPD_1$ or $RINGD_1$ current (1 µs)	±400 mA
Latch up immunity (any pin)	±100 mA
Maximum device junction temperature	+145°C
Maximum device power dissipation, continuous (1) - TA = 85°C, PD	1.5 W
Junction to ambient thermal resistance (1), Θ_{JA}	29.3°C/W
Junction to board thermal resistance (1), Θ_{JB}	13.6°C/W
Junction to case thermal resistance (1), Θ_{JC}	15.5°C/W
Junction-to-top characterization parameter (1,2), Ψ_{JT}	0.9°C/W
Reflow temperature, 10 sec., MSL3, per *JEDEC J-STD-020*	260°C
ESD immunity (Human Body Model)	*JESD22 Class 1C* compliant

Notes:

1. Refer to the next section “Thermal Performance”.
2. Above SLIC.

4.2 Thermal Performance

The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Specified performance requires that the exposed thermal pad be soldered to an equally sized exposed copper surface, which, in turn, conducts heat through multiple vias to a large internal copper plane. Thermal performance depends on the number of PCB layers and the size of the copper area. Please refer to Microchip’s application note *QFN Package (Document ID#: 080791)* and also the *Two Layer PCB Design Application Note* available on the website for general design and layout guidelines.

The thermal specifications in the Absolute Maximum Ratings section assume that the device is mounted on a highly effective thermal conductivity test board (4 layers, 2s2p) per *JEDEC JESD51-7* and *JESD51-5*, and featuring the recommended 3x5 array of thermal vias shown in the Recommended Land Pattern (36-Pin QFN) – Top View figure.

4.3 Operating Ranges

Microchip guarantees the performance of this device over industrial (-40ºC to 85ºC) temperature range by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with the *Telcordia GR-357-CORE Generic Requirements for Assuring the Reliability of Components Used in Telecommunications Equipment.*

4.3.1 Recommended Operating Conditions

Table 4-2. Operating Conditions and Valid Values

Operating Condition Parameter	Valid Values
Ambient temperature	-40°C < T_A < +85°C
Ambient relative humidity	15% to 85%
GND	0 V_{DC}
AVDD	+3.3 V_{DC} ± 5%
DVDD with respect to AVDD	±50 mV_{DC}
VDDHPI	+1.71 V_{DC} to DVDD
VDDSW Buck-Boost operation	 +3.3 V_{DC} ± 5%
Inverting-Boost operation	+3.7 V_{DC} to +5.25 V_{DC}
$VBAT_1$ with respect to GND, in Disconnect or Shutdown states	-95 V_{DC} to +0.4 V_{DC}
$VBAT_1$ with respect to GND, in other states	-95 V_{DC} to -12 V_{DC}
Digital pins	GND to VDDHPI
I/O1	GND to DVDD
Analog pins	GND – 0.3 V_{DC} to AVDD + 0.3 V_{DC}

5. Electrical Characteristics

Unless otherwise noted, test conditions are:

- Typical values are for T_A = 25ºC and nominal supply voltages. Minimum and maximum values are over the temperature and supply voltage ranges shown in the previous Recommended Operating Conditions section, except where noted.
- Default (unity) gain in X, R, DRL, AX and AR blocks; default coefficients in DISN, Z and B filters.DC feed programmed and calibrated to:
  - ILA = 25 mA, ILA CoC = 20mA, VOC = 48.0 V, V_{FLOOR}= 20V, VAS = 8.76 V and VSW = 12V
- AC load resistance = 600 Ω unless otherwise noted.
- Fuse resistors for device tests are R_F = 14 Ω
- 0 dBm0 = 0 dBm (600 Ω) = 0.775 V_{RMS}. Digital gains GX0 and GR0 to achieve 0 dBr relative levels are GX0 = +6.797 dB (7A20h) A-law or linear and GX0 = +6.737 dB (2A20h) µ-law to set A/D transmit gain to 0dB GR0 = -1.793 dB (6AA0h) A-law or linear and GR0 = -1.720 dB (3AA0h) µ-law to set D/A receive gain to 0dB
- Ringing tests were performed with the following conditions: C1 and C2 with ILR = 50 mA and RTTH = 19.0 mA AC.
  - C1 programmed ringing 71 V_{PK} (50 V_{RMS}), 0 V_{DC} offset and 1 REN (7000 Ω + 8-µF) load
  - C2 programmed ringing 85 V_{PK} (60 V_{RMS}), 0 V_{DC} offset and 3 REN (2333 Ω + 24-µF) load

5.1 Supply Currents and Power Dissipation

5.1.1 Buck Boost Switcher Circuit

Power supply currents and device power dissipation using the Buck Boost Switcher Circuit as shown in the Buck-Boost Switching Regulator Circuit and Buck-Boost Switching Regulator Circuit Bill of Materials sections with input voltage VSW = 12 VDC.

Table 5-1. Supply Currents and Power Dissipation Parameters

Operational State	Condition	IDD mA *(Note 2)*	IVSW mA *(Note 3)*	IVBAT mA *(Note 4)*	Device Power mW	Notes
		Typ	Typ	Typ	Typ	
Shutdown	Disconnect, switcher off	2.1	0.0	0.0	7	
Disconnect	VBAT=-20V	7.2	0.2	0.02	24	
Low Power Idle	VBAT=-50V	10.8	1.6	0.2	45	
Idle	On-Hook	15.1	5.8	0.7	90	
Active (normal or reverse polarity)	Off-Hook, 300 Ω	24.1	64.1	26.8	364	1
Code of Conduct (CoC)	Off-Hook, 200 Ω	24.3	51.8	21.5	392	1

.....continued

Operational State	Condition	IDD mA (Note 2)	IVSW mA (Note 3)	IVBAT mA (Note 4)	Device Power mW	Notes
		Typ	Typ	Typ	Typ	
Ringing	C1	26.2	91.0	8.8	379	1
	C2	25.3	268.0	23.8	892	1

Note:

1. Not Tested in Production. Parameter is guaranteed by characterization or correlation to other tests.
2. I_{DD} supply current is the sum of I_{AVDD}, I_{DVDD}, I_{VDDSW} and I_{VDDHPI} for the device.
3. I_{VSW} is not tested in production.
4. Measured output of switching regulator feeding into device's $VBAT_1$ pin.

5.1.2 90V Inverting Boost Switcher Circuit

Power supply currents and device power dissipation using the 90V Inverting Boost Switcher Circuit as shown in the sections Figure 8-3. 90V Inverting-Boost Switching Regulator Circuit and 90V Inverting-Boost Switching Regulator Circuit Bill of Materials1.

Table 5-2. 90V Inverting Boost Switcher Circuit Parameters

Operational State	Condition	IDD mA (Note 2)	IVSW mA (Note 3)	IVDDSW mA	IVBAT mA (Note 4)	Device Power mW	Notes
		Typ	Typ	Typ	Typ	Typ	
Shutdown	Disconnect, switcher off	2.0	0.0	0.15	0.0	7	1
Disconnect	VBAT=-20V	7.1	0.2	0.26	0.02	25	1
Low Power Idle	On-Hook, F_{SW}=24kHz	10.6	2.0	0.21	0.2	45	1
Idle	On-Hook	14.3	7.8	0.27	0.7	88	1
Active (normal or reverse polarity)	Off-Hook, 300 Ω	19.3	59.8	0.83	26.9	352	1
Code of Conduct (CoC)	Off-Hook, 200 Ω	19.1	49.2	0.83	21.6	382	1
Ringing	C1	21.8	92.0	0.86	9.3	265	1
	C2	22.0	232.0	0.90	24.9	362	1

Note:

1. Not Tested in Production. Parameter is guaranteed by characterization or correlation to other tests.
2. I_{DD} supply current is the sum of I_{AVDD}, I_{DVDD} and I_{VDDHPI} for the device.
3. I_{VSW} is not tested in production.
4. Measured output of switching regulator feeding into device's $VBAT_1$ pin.

5.2 DC Characteristics[1]

Table 5-3. DC Parameters

Symbol	Parameter Descriptions	Min	Typ	Max	Unit	Note
VIL	Digital input low voltage			0.8	V	
VIH	Digital input high voltage	2.0				
VIL	Digital input low voltage VDDHPI = 2.5V			0.7		2
VIH	Digital input high voltage VDDHPI = 2.5V	1.7				2
VIL	Digital input low voltage VDDHPI = 1.8V			0.63		2
VIH	Digital input high voltage VDDHPI = 1.8V	1.17				2
IIL	Digital input leakage current	-7		+7	µA	
IAIL	Analog input leakage current	-1		+1		
VHYS	Digital input hysteresis		250		mV	2
VHYS	Digital input hysteresis VDDHPI = 2.5V		235			
VHYS	Digital input hysteresis VDDHPI = 1.8V		220			
VOL	Digital output low voltage (I_{OL} = 2 mA)			0.4	V	3
VOH	Digital output high voltage (I_{OH} = 400 µA)	2.4				
IOL	Digital output leakage current (Hi-Z state, 0 < V < DVDD)	-7		+7	µA	
VREF	VREF output open circuit voltage (IVREF = +/-100 µA)	1.43	1.5	1.57	V	
CIREF	IREF pin maximum load capacitance			20	pF	2
CI	Digital input capacitance			4		
CO	Digital output capacitance			4		
PSRR1	AVDD, DVDD power supply rejection ratio (1.02 kHz, 100 mV_{RMS}, either path, GX = GR = 0 dB)	32	38		dB	
PSRR2	$VBAT_1$ power supply rejection ratio (1.02 kHz, 100 mV_{RMS}, either path, GX = GR = 0 dB)	40				2

Note:

1. Unless otherwise specified VDDHPI = 3.3V
2. This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.
3. VS/IO output is resistive for less than a 0.8 V drop. Total DC current must not exceed absolute maximum ratings.

5.3 DC Feed and Signaling – All States Except Low Power Idle Mode

Table 5-4. All States Except Low Power Idle Mode Test Conditions

Description	Test Conditions	Min	Typ	Max	Unit	Note
ILA programmable range, Active state		18		30	mA	1
I_L, Loop current accuracy, Active state	I_L in constant-current region after ILA calibration	-10		+10	%	
I_{RINGD}, RINGD leakage, Ring Open state	$VBAT_1$ = -80 V R_L = 0 to GND or $VBAT_1$			1000	µA	1
I_{TIPD}, TIPD leakage, Tip Open state	$VBAT_1$ = -80 V R_L = 0 to GND or $VBAT_1$			1000		
TIPD, RINGD leakage, Disconnect state	$VBAT_1$ = -80 V R_L = 0 to GND or $VBAT_1$			10		
I_{RINGD}, RINGD current accuracy, Tip Open state	RINGD to ground	-10		+10	%	1
V_{TIPD}, ground-start signaling	TIPD to -48 V = 7 kΩ, RINGD to ground = 100 Ω	-7.5	-5		V	
TDC, RDC input offset current		1.35	1.5	1.65	µA	1, 2
Ground key accuracy	After calibration	-1 mA - 15%		+1 mA + 15%		
Switch hook accuracy	After calibration	-20		+20	%	
Open circuit voltage, $V_{TIPD} - V_{RINGD}$	VOC = 48 V, after VOC calibration	-7		+7		
V_{RINGD}, open circuit	VOC = 48 V, after VOC calibration	-56.5		-49.0	V	

Note:

1. This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.
2. Analog input pad leakage can add to this value. Refer to the specifications in the DC Characteristics1 section.

5.4 DC Feed and Signaling - Low Power Idle Mode State

Table 5-5. Low Power Idle Mode State Test Conditions

Description	Test Conditions	Min	Typ	Max	Unit	Note
$V_{TIPD} - V_{RINGD}$ voltage	$VBAT_1$ = -52 V, I_{LOAD} = 3 mA	44			V	Refer to note.
	R_{LOAD} = 3.5 KΩ	23	28	33		
	$VBAT_1$ = -52 V, R_{LOAD} = open	44	48	51		
I_{TIPD} current limit	TIPD sourcing current	9	31	70	mA	Refer to note.
I_{RINGD} current limit	RINGD sinking current, R_{LOAD} = 600 Ω	7.1	8.0	9.3		
Off-hook current settling time	R_{LOAD} = 200 Ω		150	800	µs	Refer to note.
DC feed resistance	I_{LOAD} < current limit		200		Ω	
	I_{LOAD} > current limit		230k			

Note: This parameter is guaranteed by characterization or correlation to other tests. Typical values not tested in production.

5.5 Metering

Table 5-6. Metering Test Conditions

Description	Test Conditions	Min	Typ	Max	Unit	Note
Level accuracy	0.5 VRMS, 12 or 16 kHz, 200 or 3000 Ω AC load	-5		+10	%	Refer to note.
Frequency accuracy	12 or 16 kHz	-0.1		+0.1	%	

Note: This parameter is guaranteed by characterization or correlation to other tests. Typical values not tested in production.

5.6 Ringing

Table 5-7. Ringing Test Conditions

Description	Test Conditions	Min	Typ	Max	Unit	Note
Ringing Voltage Accuracy	52.5 V_{PK} into a 3 REN load	-7		+7	%	1
Normal Polarity Ringing DC offset, $V_{TIPD} - V_{RINGD}$	R_L = open circuit, programmed rInging = 0 V_{PK}	-5	0	+2	V	2, 3
Harmonic distortion	52.5 V_{PK} into a 3 REN load		3	5	%	
Ringing current limit accuracy	R_L = 600 Ω	-10		10		
Ringing source impedance			200		Ω	2
DC ring trip accuracy	EGBIAS = 1	-15		+15	%	2, 4
AC ring trip accuracy	EGBIAS = 0	-15		+15		
Ring trip delay	Periods of ringing	1		3	cycles	

Note:

1. This production test is performed without calibration. After calibration, typical accuracy is within +/-4%.
2. This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.
3. After calibration.
4. If the ringing current in the loop is near the current limit more than 50% of the time, a ring trip will occur regardless of the average current.

5.7 Switching Regulator Controller Y

The following specifications apply to the switching regulator controller Y.

Table 5-8. Switching Regulator Controller Test Conditions

Description	Test Conditions	Min	Typ	Max	Unit	Note
SWISY shutdown threshold	Referenced to GND	85	100	115	mV	
SWISY hysteresis			25			1
SWISY input bias current		-10		10	µA	
SWISY shutdown delay	V_{SWISx} > 115 mV	12		88	ns	1, 2
SWCMPY output current		-200		200	µA	1
SWCMPY operating range		0.4		2.6	V	
SWVSY to SWCMPY gain		0.4		40	V/nA	
SWVSY to SWCMPY bandwidth		100			kHz	
SWVSY input offset current	R_{VSx} = 1.0 MΩ	1.3	1.5	1.7	µA	
LFC1 output impedance			12		kΩ	
Output voltage accuracy	Calibrated -95 V fixed ringing voltage	-100		-90	V	3

Note:

1. This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.
2. Time from SWISY exceeding threshold to SWOUTY voltage passing through DVDD/2.
3. Accuracy following battery calibration depends on the battery voltage sense accuracy (+/-4%) plus the calibration resolution of +/- 0.625 V.

5.8 MOSFET Driver – Inverting-Boost Operation (VDDSW = +5 V)

The following specifications apply to Inverting-Boost operation when driving the switching regulator N-channel MOSFET device.

Table 5-9. MOSFET Driver – Inverting-Boost Operation Test Conditions

Description	Test Conditions	Min	Typ	Max	Unit	Note
VDDSW undervoltage lockout range		3.80	4.0	4.15	V	Refer to note.
VDDSW undervoltage lockout accuracy		-100		100	mV	
SWOUTY peak source current	V_{SWOUTx} = 2.5 V, C_{LOAD} = 1.5 nF	100			mA	
SWOUTY peak sink current	V_{SWOUTx} = 2.5 V, C_{LOAD} = 1.5 nF	200				

Note: This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.

5.9 Voice ADC Signal Sense Accuracy

Table 5-10. Voice ADC Signal Sense Accuracy Parameters

Description	Code	Full Scale	Useful Range	Min	Typ	Max	Unit	Note
Metallic AC coupled voltage (Tip/Ring voice)	00h	-3.44 to +3.44	-3.44 to +3.44	-4%		+4%	V	1, 2
Voice DAC analog loop back	0Ah	-2.0 to +2.0	-1.0 to +1.0	-12%		+12%		

Note:

1. All specifications assume calibration.
2. The% limits are defined as the% of programmed threshold value or the% of the actual voltage or current on Tip / Ring. The offset and percentage errors are independent and combine as RMS errors.

5.10 Supervision ADC Signal Sense Accuracy

Table 5-11. Supervision ADC Signal Sense Accuracy Parameters

Description	Code	Full Scale	Useful Range	Min	Typ	Max	Unit	Note
Sense at SWVSY	01h	-240 to +240	-180 to 0	-0.5 V – 4 %		+0.5 V + 4 %	V	1, 2, 3, 6
				-0.5 V – 4 %		+0.5 V + 4 %		
Sense at VS1	03h		-180 to +60	-0.5 V – 4 %		+0.5 V + 4 %		
Tip voltage to ground	04h		-225 to +225	-2.0 V – 4 %		+1.0 V + 4 %		
Ring voltage to ground	05h			-2.0 V – 4 %		+1.0 V + 4 %		
Metallic DC line voltage (Tip to Ring)	06h		-160 to +160	-0.5 V – 5 %		+0.5 V + 5 %		
Longitudinal DC line voltage (Tip to ground + Ring to ground)	0Ah			-1.0 V – 5 %		+1.0 V + 5 %		1, 2, 6
MOSFET drive supply, VDDSW	10h	+2 to +10	+2.5 to +5.5	-0.08 V – 0.5%		+0.08V + 0.5%		
Metallic loop current, IM (Tip to Ring) in Normal Mode	07h	-59.5 to +59.5(4)	-51 to +51(4)	-1.0 mA – 5 %		+1.0 mA + 5%	mA	
Longitudinal loop current, IL (total) in Normal Mode	08h	-59.5 to +59.5	-42 to +42	-1.0 mA – 5 %		+1.0 mA + 5%		
Ring current, IB (IM+IL)	0Eh			-2.0 mA – 5 %		+2.0 mA + 5%		
Tip current, IA (IM-IL)	0Fh			-2.0 mA – 5 %		+2.0 mA + 5%		
Metallic loop current (IM) in Low Gain Mode	08h	-297.5 to +297.5	-100 to +100	-5.0 µA – 5 %		+5.0 µA + 5%	µA	
Longitudinal loop current per wire (IL) in Low Gain Mode	07h		-250 to +250	-5.0 µA – 5 %		+5.0 µA + 5%		

.....continued

Description	Code	Full Scale	Useful Range	Min	Typ	Max	Unit	Note
Tip voltage to Longitudinal current ratio	N/A	N/A	N/A	-6.5		+6.5	%	1, 5, 6, 7
Ring voltage to Longitudinal current ratio				-6.5		+6.5		
Metallic voltage to Metallic current ratio				-6.5		+6.5		
Temperature sense	0Dh	-50 to +150	-50 to +150	-15		+15	ºC	1, 6

Note:

1. All specifications assume calibration.
2. The% limits are defined as the% of programmed threshold value or the% of the actual voltage or current. The offset and percentage errors are independent and combine as RMS errors.
3. This is measured in production by calibrating offset voltage and applying -26 V for voltage to ground and 20 V Metallic. Accurately measuring smaller voltage requires care in offset calibration.
4. The Metallic loop current scale and range during ringing are -119 mA to +119 mA.
5. These are ratios of voltage to current measurements in Low Gain state. Not tested in production.
6. Full scale is defined as a digital output code of ±32768.
7. Not tested in production

5.11 Transmission Characteristics - Narrowband Codec Mode

Table 5-12. Narrowband Codec Mode Test Conditions

Description	Test Conditions	Min	Typ	Max	Unit	Note
TAC – RAC overload level	Active state, GX = AX = 0 dB	3.4			V_{PK}	1, 2
Transmit level, A/D	0 dBm, GX = GX0, 1014 Hz		0		dBm0	
Receive level, D/A	0 dBm0, GR = GR0, 1014 Hz		0		dBm0	
Gain accuracy, D/A or A/D	0 dBm0, 1014 Hz, off-hook	-0.35		+0.35	dB	
Gain accuracy, D/A or A/D	0 dBm0, 1014 Hz, on-hook	-0.5		+0.5		
Idle channel noise $V_{TIPD} – V_{RINGD}$ Digital out	Digital input = 0, A-law, 0 dBr Digital input = 0, µ-law, 0 dBr $V_{TIPD} – V_{RINGD}$ = 0 V_{AC}, A-law, 0 dBr $V_{TIPD} – V_{RINGD}$ = 0 V_{AC}, µ-law, 0 dBr			-74 16 -65 19	dBm0p dBrnC0 dBm0p dBrnC0	5

.....continued

Description	Test Conditions	Min	Typ	Max	Unit	Note
Two-wire return loss	200 to 3400 Hz	26	30		dB	
Longitudinal to metallic balance	200 to 3400 Hz	50				7
Longitudinal signal generation	300 to 3400 Hz	42				7
Longitudinal current capability, per wire TIPD or RINGD	Active state	8.5			mA_{RMS}	1
Longitudinal impedance at TIPD or RINGD	0 to 100 Hz, LI = 0		100		Ω/pin	
Attenuation distortion	300 to 3000 Hz	-0.125		+0.125	dB	1, 3
Single frequency distortion	A-law or µ-law, off-hook			-46		4
Second harmonic distortion, D/A	GR = 0 dB, linear mode, off-hook			-50		
End-to-end absolute group delay	B = Z = 0; X = R = 1, C/L = 0			678	µs	1, 6
PESQ-LQ voice quality score	Linear, A-law, or µ-law					1

Note:

1. This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.
2. Overload level is defined when THD = 1%.
3. See figures Transmit (A to D) Path Attenuation vs. Frequency and Receive (D to A) Path Attenuation vs. Frequency.
4. 0 dBm0 input signal, 300 to 3400 Hz measurement at any other frequency, 300 Hz to 3400 Hz.
5. No single frequency component in the range above 3800 Hz may exceed a level of -55 dBm0.
6. The End-to-End Group Delay is the absolute group delay of the echo path with the B filter turned off.
7. This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.

5.12 Attenuation Distortion - Narrowband Codec Mode

The signal attenuation in either path is nominally independent of the frequency. The deviations from nominal attenuation will stay within the limits shown in the figures below. The reference frequency is 1014 Hz and the signal level is -10 dBm0.

Figure 5-1. Transmit (A to D) Path Attenuation vs. Frequency

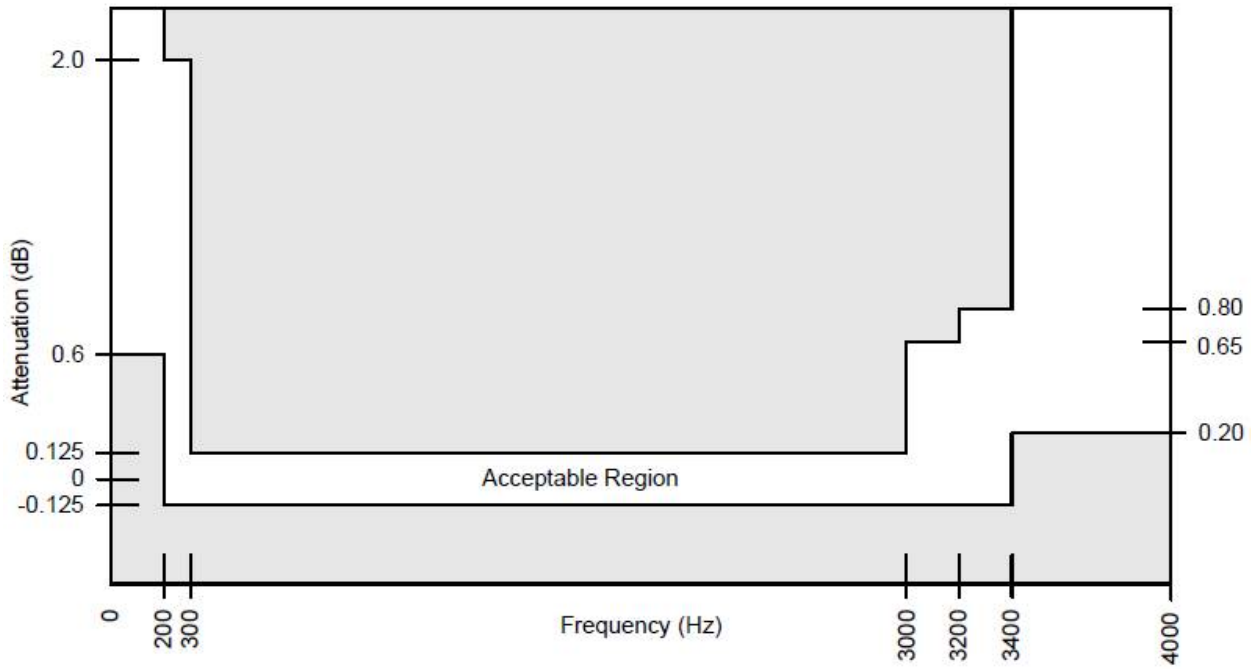
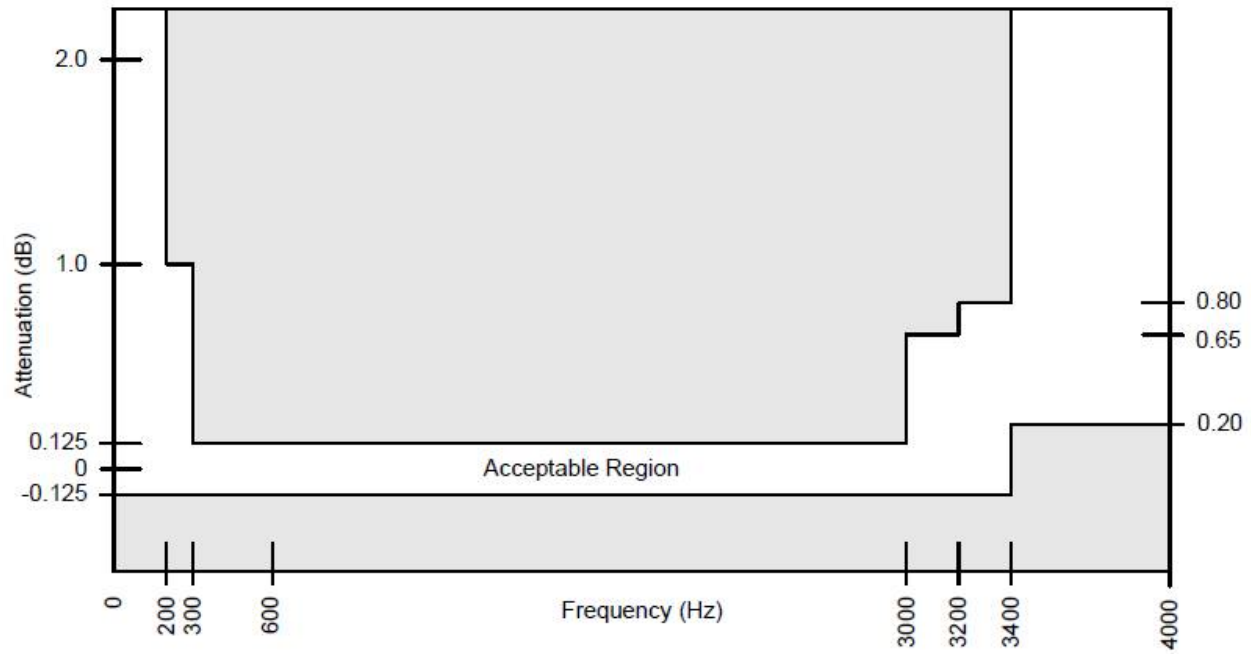


Figure 5-2. Receive (D to A) Path Attenuation vs. Frequency



5.13 Discrimination Against Out-of-Band Input Signals - Narrowband Codec Mode

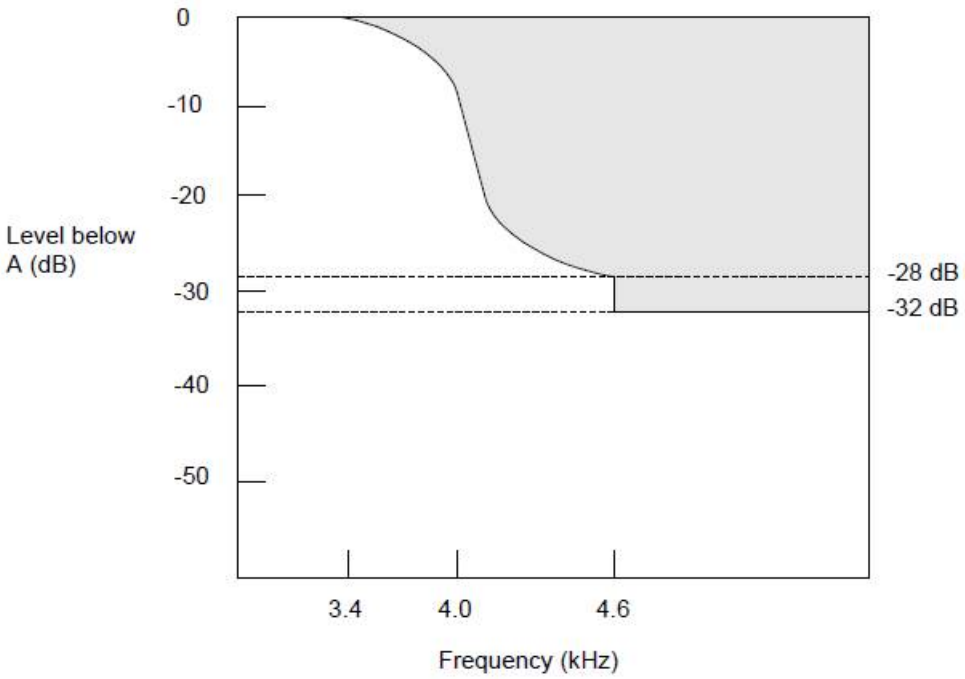
When an out-of-band sine wave signal of frequency f, and level A is applied to the analog input, there may be frequency components below 4 kHz at the digital output which are caused by the out-of-band signal. These components are at least the specified dB level below the level of a signal at the same output originating from a 1014-Hz sine wave signal with a level of A dBm0 also applied to the analog input. The minimum specifications are shown in the table below. The attenuation of the waveform below amplitude A, between 3400 Hz and 4600 Hz, is given by the formula:

$$\text{Attenuation} = \left[14 - 14\sin\left(\frac{\pi(4000 - f)}{1200}\right)\right] \text{dB}$$

Table 5-13. Out-of-Band Discrimination - Narrowband Codec Mode

Frequency of Out-of-Band Signal	Amplitude of Out-of-Band Signal	Level below A
16.6 Hz < f < 45 Hz	-25 dBm0 < A ≤ 0 dBm0	18 dB
45 Hz < f < 65 Hz	-25 dBm0 < A ≤ 0 dBm0	25 dB
65 Hz < f < 100 Hz	-25 dBm0 < A ≤ 0 dBm0	10 dB
3400 Hz < f < 4600 Hz	-25 dBm0 < A ≤ 0 dBm0	Refer to the figure below.
4600 Hz < f < 100 kHz	-25 dBm0 < A ≤ 0 dBm0	32 dB

Figure 5-3. Discrimination Against Out-of-Band Signals



5.14 Discrimination Against 12 kHz and 16 kHz Metering Signals – Narrowband Codec Mode

If the Le9643 device is used in a metering application where 12 kHz or 16 kHz tone bursts are injected onto the telephone line toward the subscriber, a portion of these tones may also appear at the transmit input. These

out-of-band signals may cause frequency components to appear below 4 kHz at the digital output. For a 12 kHz or 16 kHz tone, the frequency components below 4 kHz are reduced from the input by at least 70 dB. The sum of the peak metering and signal voltages must be within the TAC – RAC pin overload level.

5.15 Spurious Out-of-Band Signals at the Analog Output - Narrowband Codec Mode

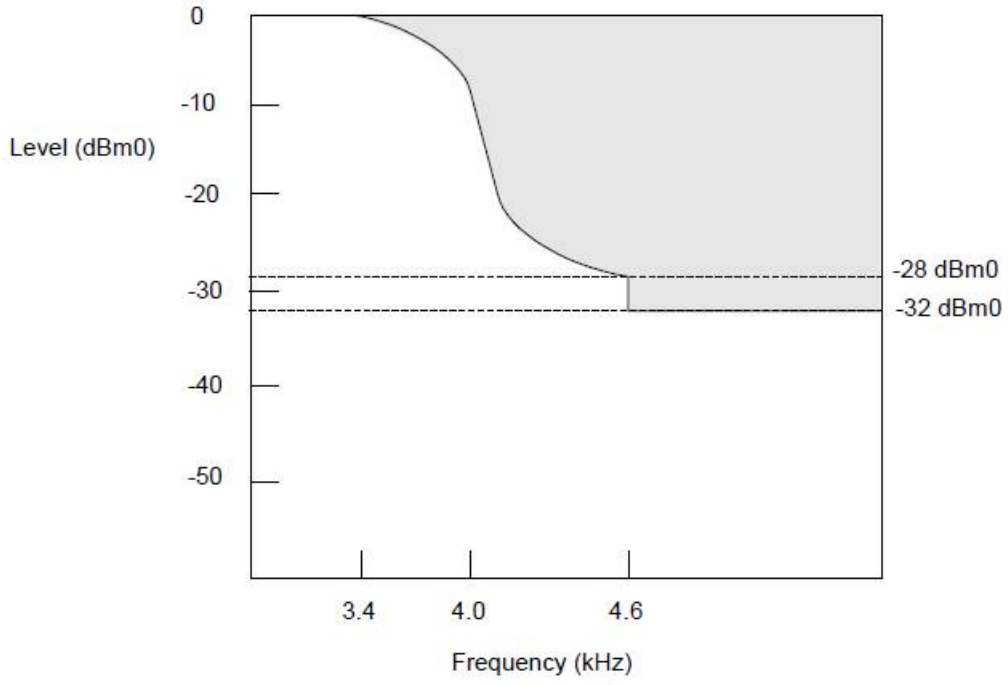
With PCM idle code being applied from the host and either a quiet 600 Ω termination or an open being applied to Tip and Ring, any single frequency tone between 0 and 16 kHz measured at the analog output shall be less than -50 dBm0. With PCM code words representing a sine wave signal in the range of 300 Hz to 3400 Hz at a level of 0 dBm0 applied to the digital input, the level of the spurious Out-of-Band signals at the analog output is less than the limits shown below.

Frequency	Level
4.6 kHz to 40 kHz	-32 dBm0
40 kHz to 240 kHz	-46 dBm0
240 kHz to 1 MHz	-36 dBm0

With code words representing any sine wave signal in the range 3.4 kHz to 4.0 kHz at a level of 0 dBm0 applied to the digital input, the level of the signals at the analog output are below the limits in the following figure. The amplitude of the spurious out-of-band signals between 3400 Hz and 4600 Hz is given by the formula:

$$\text{Level} = \left[-14 - 14\sin\left(\frac{\pi(f-4000)}{1200}\right)\right] \text{dBm0}$$

Figure 5-4. Spurious Out-of-Band Signals

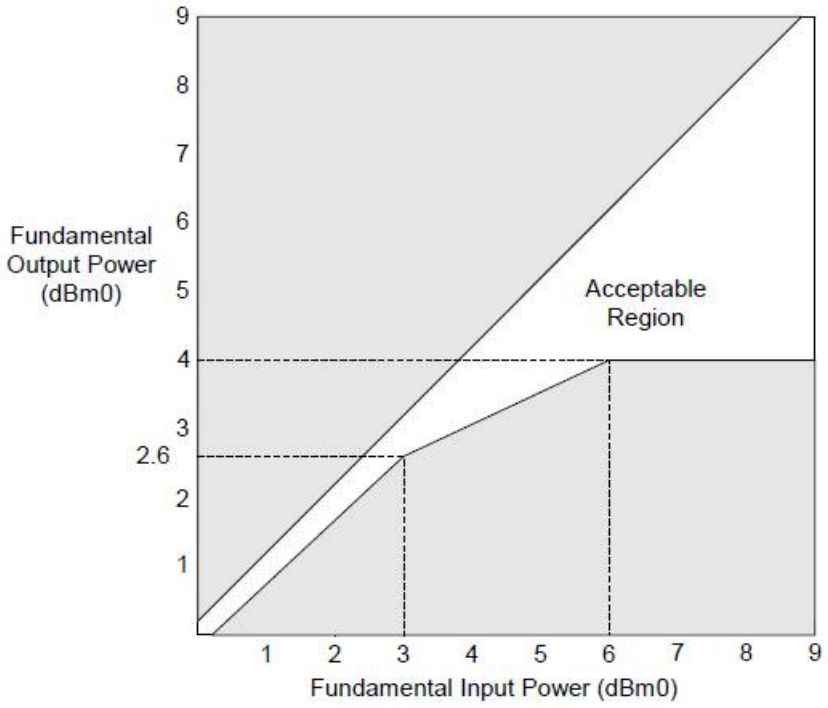


5.16 Overload Compression - Narrowband Codec Mode

The following figure shows the acceptable region of operation for input signal levels above the reference input power (0 dBm0). The conditions for this figure are:

1. +1.2 dB < GX ≤ +12 dB
2. -12 dB ≤ GR < -1.2 dB
3. Digital voice output of one channel connected to digital voice input of a second channel.
4. Measurement analog-to-analog

Figure 5-5. Analog-to-Analog Overload Compression



5.17 Gain Linearity - Narrowband Codec Mode

The gain deviation relative to the gain at -10 dBm0 is within the limits shown in the following figures (A-law and µ-law) for either transmission path when the input is a sine wave signal of 1014 Hz.

Figure 5-6. A-law Gain Linearity with Tone Input (Both Paths)

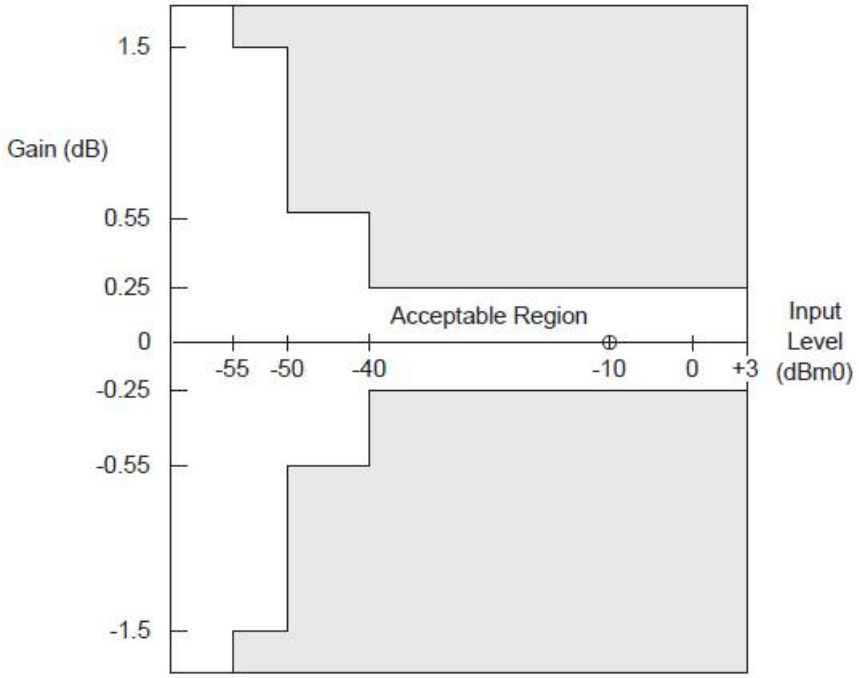
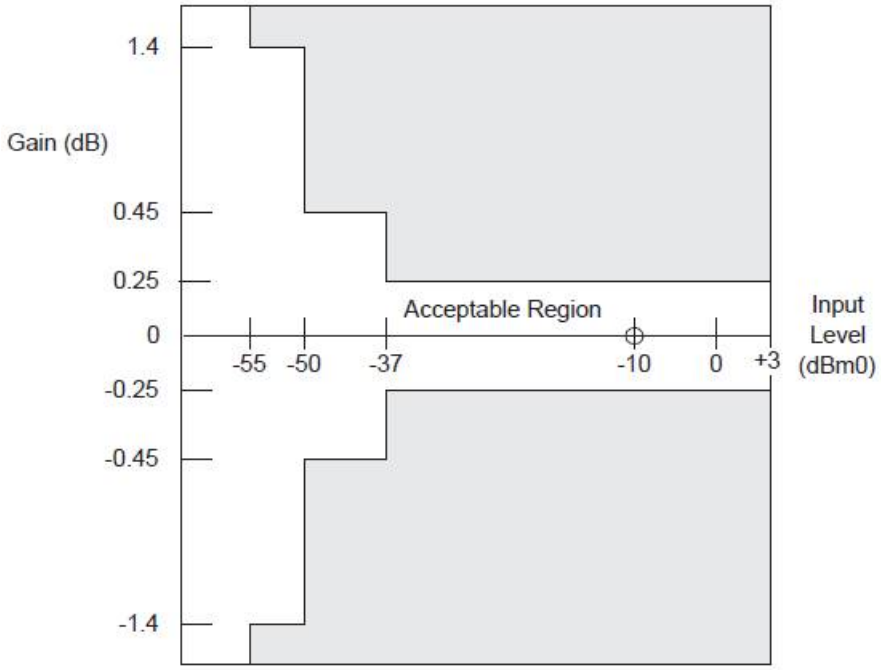


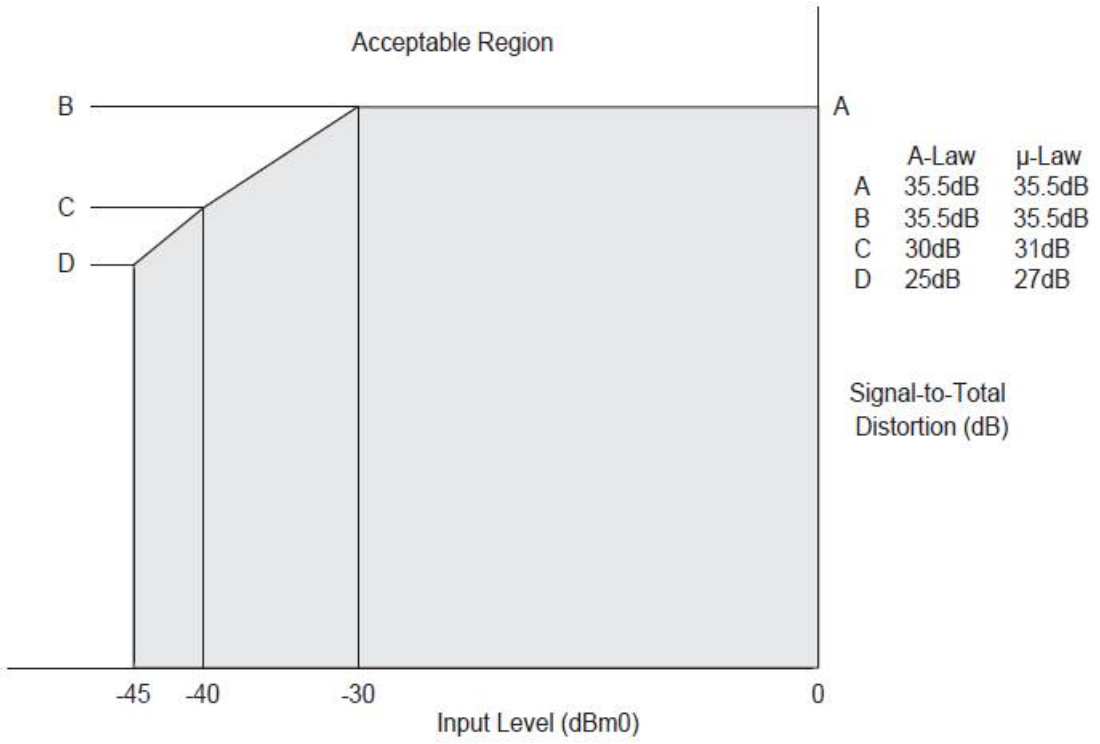
Figure 5-7. µ-law Gain Linearity with Tone Input (Both Paths)



5.18 Total Distortion Including Quantizing Distortion - Narrowband Codec Mode

The signal to total distortion ratio will exceed the limits shown in the following figure for either path when the input signal is a sine wave with a frequency of 1014 Hz, using psophometric weighting for A-law and C-message weighting for µ-law.

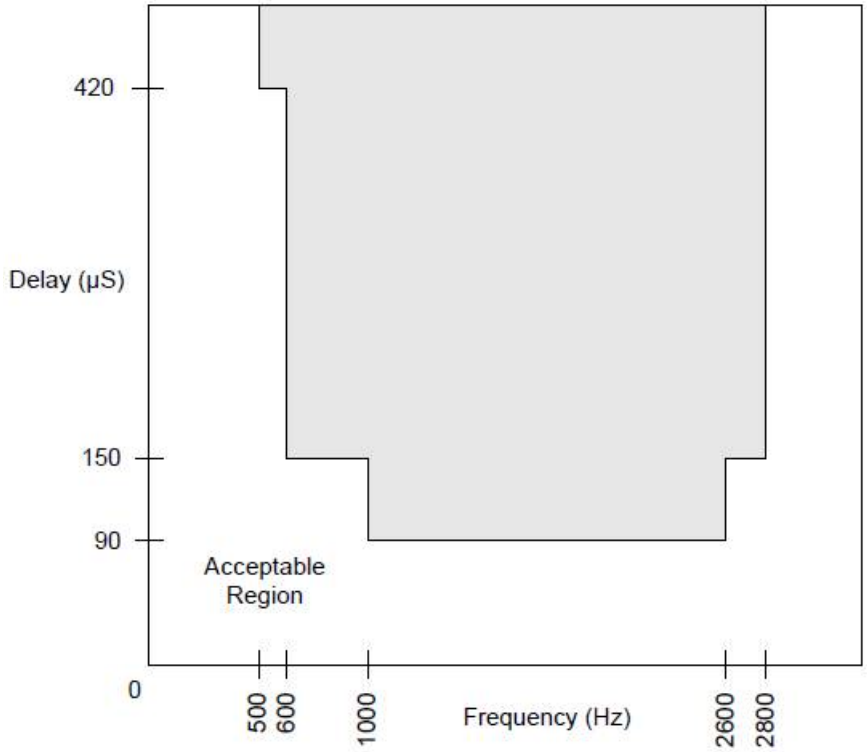
Figure 5-8. Total Distortion with Tone Input (Both Paths)



5.19 Group Delay Distortion - Narrowband Codec Mode

For either transmission path, the group delay distortion is within the limits shown in the following figure. The minimum value of the group delay is taken as the reference. The signal level should be 0 dBm0.

Figure 5-9. Group Delay Distortion



5.20 Transmission Characteristics – Wideband Codec Mode

Table 5-14. Wideband Codec Mode Test Conditions

Description	Test Conditions	Min	Typ	Max	Unit	Note
TAC – RAC overload level	Active state GX = AX = 0 dB	3.4			V_{PK}	1, 2
Transmit level, A/D	0 dBm, GX = GX0, 1014 Hz		0		dBm0	
Receive level, D/A	0 dBm0, GR = GR0, 1014 Hz		0		dBm	
Gain accuracy, D/A or A/D	0 dBm0, 1014 Hz, off-hook	-0.5		+0.5	dB	
Gain accuracy, D/A or A/D	0 dBm0, 1014 Hz, on-hook	-0.5		+0.5		1
Attenuation distortion	100 Hz to 6.0 kHz	-0.25		+0.25		3
Single frequency distortion	0 dBm0, Linear Mode, 150 Hz to 6.8 kHz, off-hook			-50		4
Signal to noise + distortion	0 dBm0, Linear Mode, 150 Hz to 6.8 kHz	50				4
Second harmonic distortion, D/A	GR = 0 dB, off-hook			-50		
Idle channel noise, $V_{TIPD} – V_{RINGD}$ Digital out	 Digital input = 0, linear, 0 dBr $V_{TIPD} – V_{RINGD}$ = 0 V_{AC}, linear, 0 dBr			-67 -67	dBm0p dBm0p	1, 5
End-to-end absolute group delay	B = Z = 0; X = R = 1, C/L = 0			340	µs	1, 6
Two-wire return loss	150 to 6800 Hz	20	26		dB	1
Longitudinal to metallic balance	200 to 3400 Hz 6000 Hz	50 43			dB	7
Longitudinal signal generation	300 to 3400 Hz	42				1
Longitudinal current capability, per wire TIPD or RINGD	Active state	8.5			mA_{RMS}	1
Longitudinal impedance at TIPD or RINGD	0 to 100 Hz, LI = 0		100		Ω/pin	1
PESQ-LQ voice quality score	Linear		4.30			1

Note:

1. This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.
2. Overload level is defined when THD = 1%.
3. See figures Transmit (A to D) Path Attenuation vs. Frequency – (with High-Pass Filter Enabled) and Receive (D to A) Path Attenuation vs. Frequency.
4. 0 dBm0 input signal, 150 to 6800 Hz measurement at any other frequency, 150 to 6800 Hz.
5. No single frequency component in the range above 7600 Hz may exceed a level of -55 dBm0.
6. The End-to-End Group Delay is the absolute group delay of the echo path with the B filter turned off.
7. This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.

5.21 Attenuation Distortion - Wideband Codec Mode

The signal attenuation in either path is nominally independent of the frequency. The deviations from nominal attenuation will stay within the limits shown in the following figures. The reference frequency is 1014 Hz and the signal level is -10 dBm0.

Figure 5-10. Transmit (A to D) Path Attenuation vs. Frequency – (with High-Pass Filter Enabled)

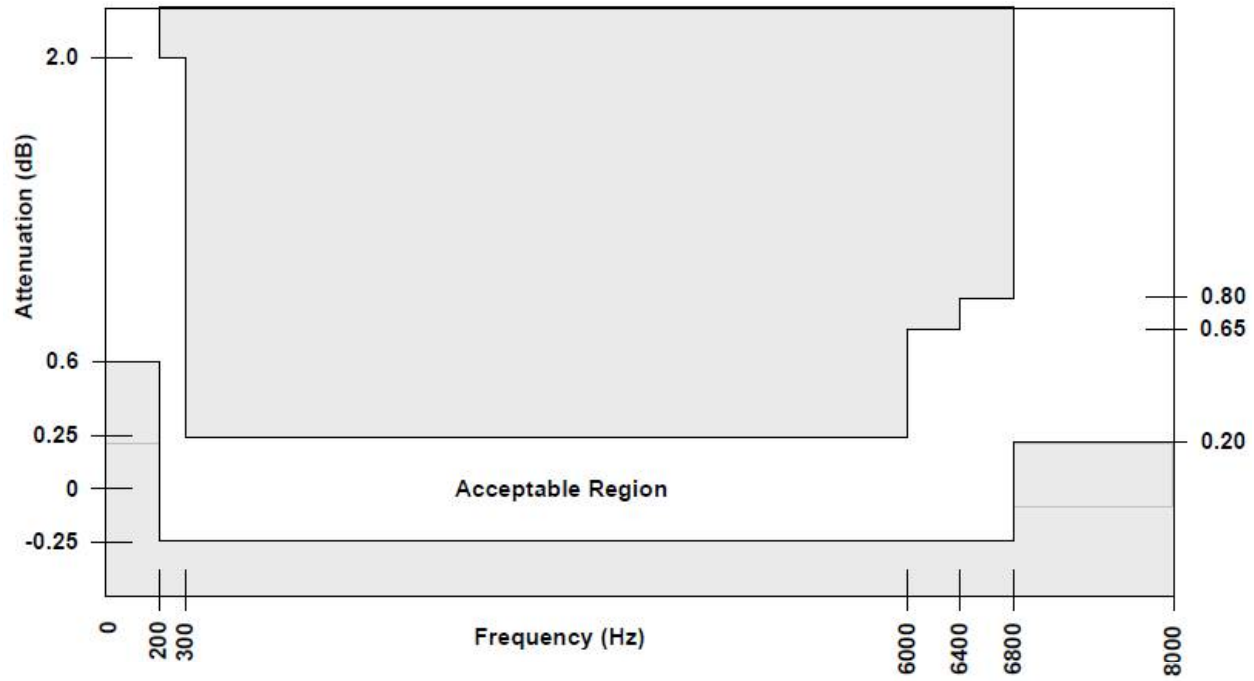
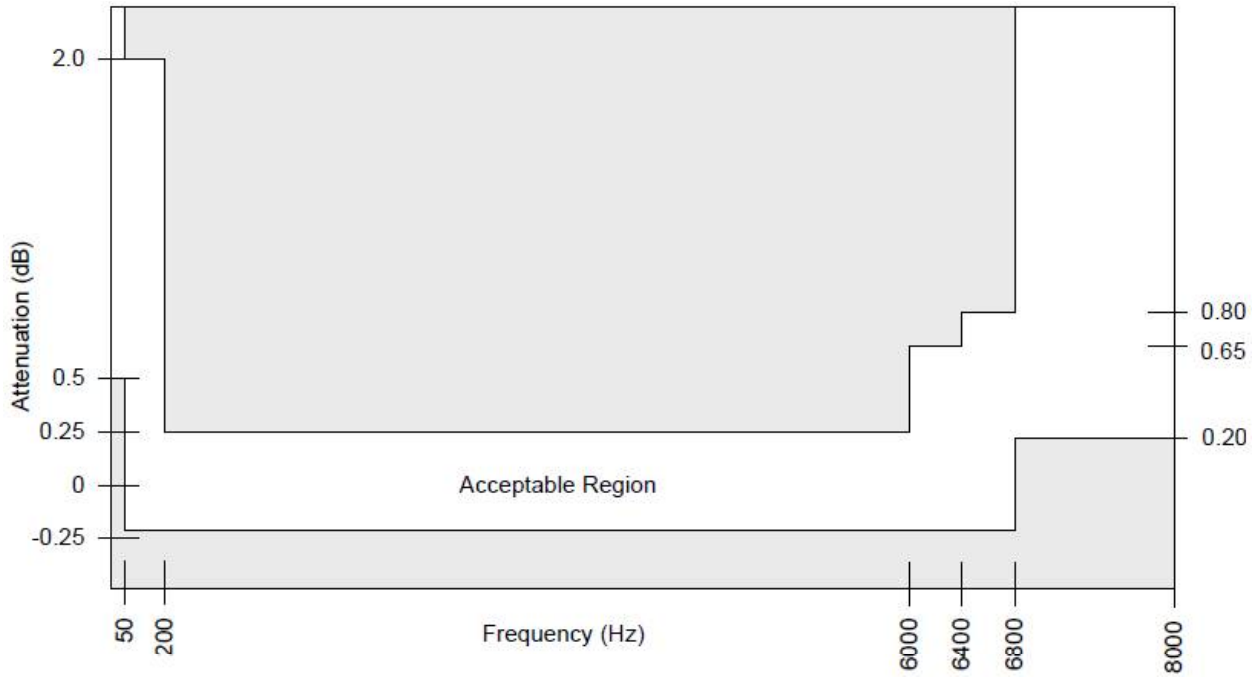


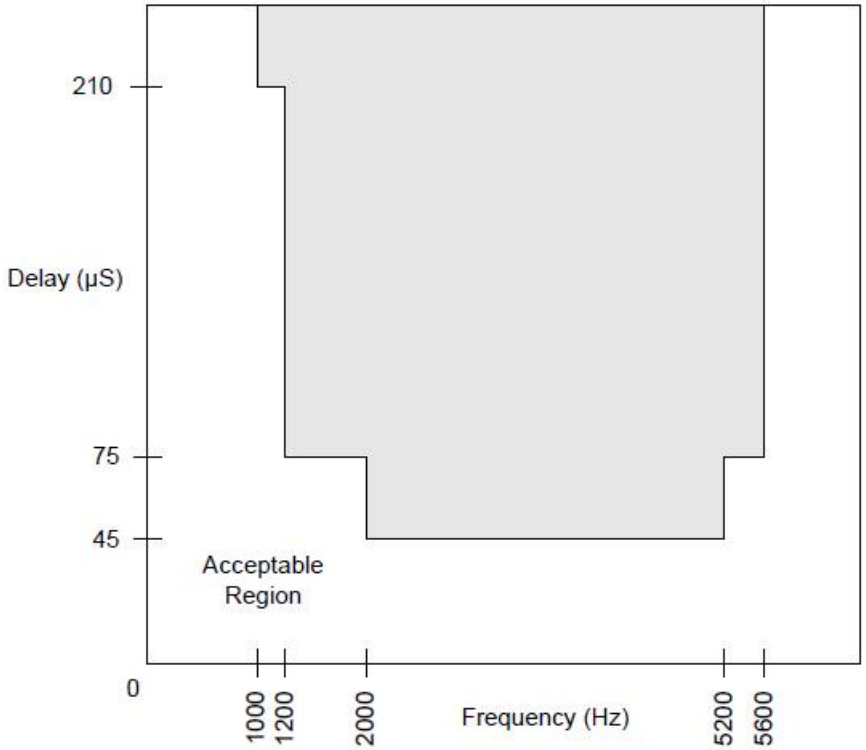
Figure 5-11. Receive (D to A) Path Attenuation vs. Frequency



5.22 Group Delay Distortion - Wideband Codec Mode

For either transmission path, the group delay distortion is within the limits shown in the following figure. The minimum value of the group delay is taken as the reference. The signal level should be 0 dBm0.

Figure 5-12. Group Delay Distortion



6. Switching Characteristics and Waveforms

The following are the switching characteristics over operating range, unless otherwise noted. Minimum and maximum values are valid for all digital outputs with a 115 pF load.

6.1 PCM and SPI Mode

The PCM and SPI mode is used to communicate audio and control information to the host processor. It is enabled when the $\overline{ZSI}$ pin is tied to DVDD. Unless otherwise specified, the SPI timing values are valid for VDDHPI = 1.8 V_{DC}, 2.5 V_{DC}, or 3.3 V_{DC}.

6.1.1 SPI Interface

Table 6-1. SPI Interface Parameters

No.	Symbol	Parameter	Min[2]	Typ	Max[2]	Unit	Note
1	t_{DCY}	Data clock period	122			ns	
2	t_{DCH}	Data clock high pulse width	48				
3	t_{DCL}	Data clock low pulse width	48				
4	t_{DCR}	Rise time of clock			8		
5	t_{DCF}	Fall time of clock			8		
6	t_{ICSS}	Chip select setup time, Input mode	5				
7	t_{ICSH}	Chip select hold time, Input mode	0				
8	t_{ICSL}	Chip select pulse width, Input mode		$8t_{DCY}$			
9	t_{ICSO}	Chip select off time, Input mode	0				
10	t_{IDS}	Input data setup time	5				
11	t_{IDH}	Input data hold time	0				
12	t_{OLH}	I/O_1 output latch valid			2500		
13	t_{OCSS}	Chip select setup time, Output mode	5				
14	t_{OCSH}	Chip select hold time, Output mode	0				
15	t_{OCSL}	Chip select pulse width, Output mode		$8t_{DCY}$			
16	t_{OCSO}	Chip select off time, Output mode	0				
17	t_{ODD}	Output data turn on delay			21		1
18	t_{ODH}	Output data hold time	2				
19	t_{ODOF}	Output data turn off delay	0		17		
20	t_{ODC}	Output data valid			32		

Note:

1. The first data bit is enabled on the falling edge of CS or the falling edge of DCLK, whichever occurs last.
2. Individual timing parameters guaranteed by correlation to device functionality testing.

Figure 6-1. SPI Interface (Input Mode)

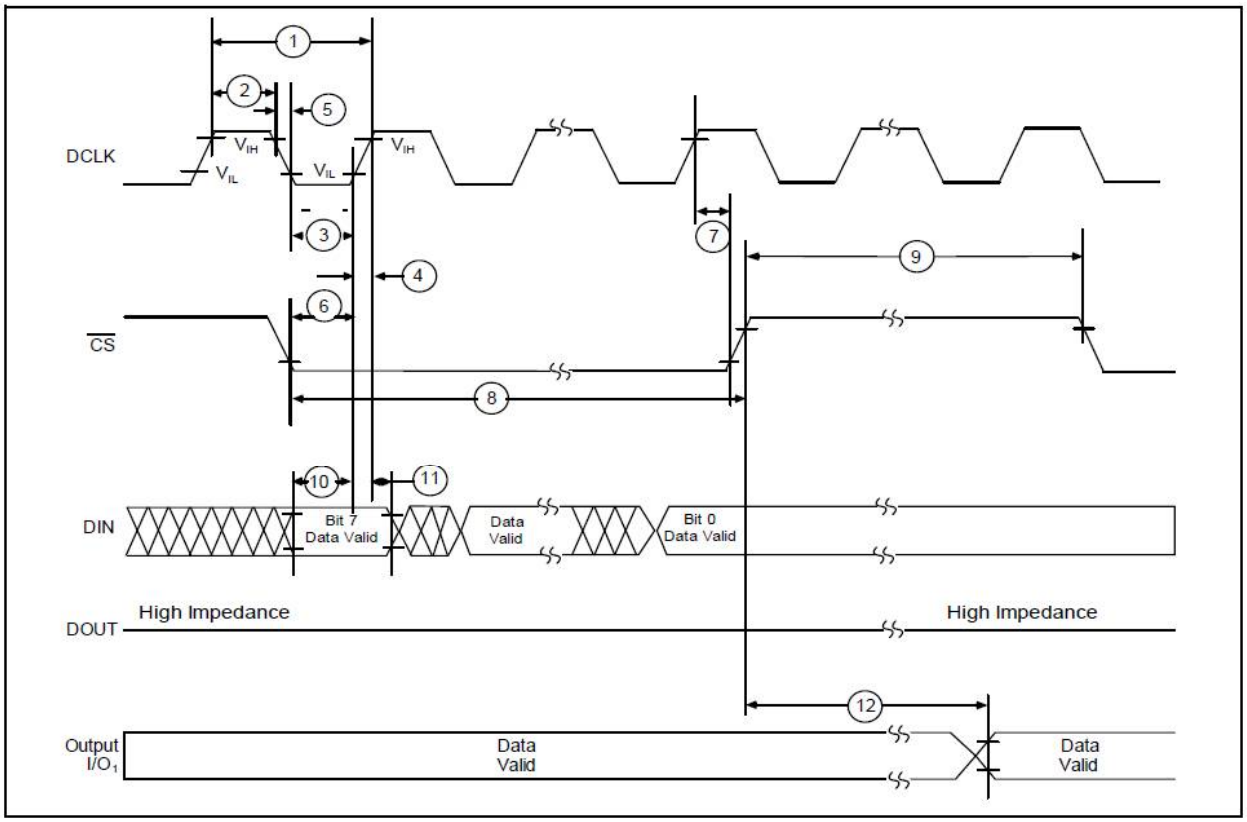
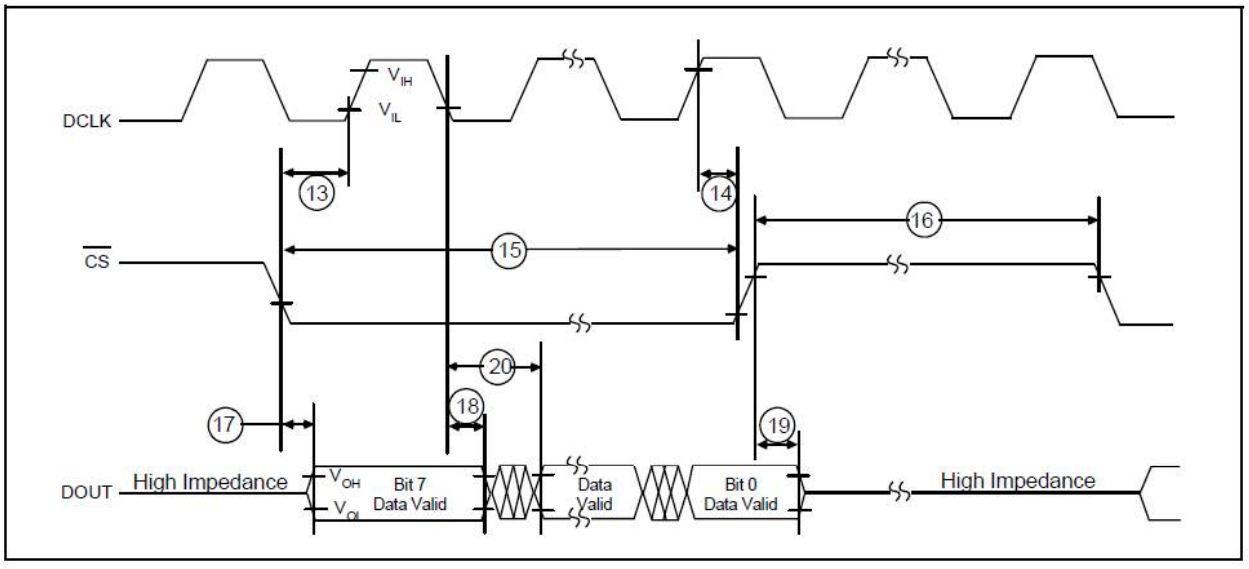


Figure 6-2. SPI Interface (Output Mode)



6.1.2 PCM Interface

PCLK shall not exceed 8.192 MHz. Unless otherwise specified, the PCM timing values are valid for VDDHPI = 1.8 VDC, 2.5 VDC, or 3.3 VDC. See the figures below for the PCM interface timing diagrams.

Table 6-2. PCM Interface Parameters

No.	Symbol	Parameter	Min[3]	Typ	Max[3]	Unit	Note
21	t_{PCY}	PCM Clock (PCLK) period	122		977	ns	1
22	t_{PCH}	PCLK high pulse width	48				
23	t_{PCL}	PCLK low pulse width	48				
24	t_{PCR}	PCLK rise time			8		
25	t_{PCF}	PCLK fall time			8		
26	t_{FSS}	FS setup time	5		t_{PCY}–30		
27	t_{FSH}	FS hold time	0				
-	t_{FST}	Allowed PCLK or FS jitter time	–25		25		1
30	t_{DXD}	PCM data output delay			32		
31	t_{DXH}	PCM data output hold time	2				
32	t_{DXZ}	PCM data output delay to high Z	0		19		
33	t_{DRS}	PCM data input setup time	5				
34	t_{DRH}	PCM data input hold time	0				
-	t_{FSL}	FS low pulse width	1.5 t_{PCY}				2

Note:

1. The PCLK frequency must be an integer multiple of the Frame Sync (FS) frequency. FS is expected to be an accurate 8 kHz (Narrowband or Wideband) or 16 kHz (Wideband) pulse train. The actual PCLK rate depends on the CSEL bit setting in the Chip Configuration register. The minimum frequency is 1.024 MHz and the maximum frequency is 8.192 MHz. If PCLK has jitter, care must be taken to ensure that all setup, hold, and pulse width requirements are met.
2. Applies only when FS is active low.
3. Individual timing parameters guaranteed by correlation to device functionality testing.

Figure 6-3. PCM Clock Timing

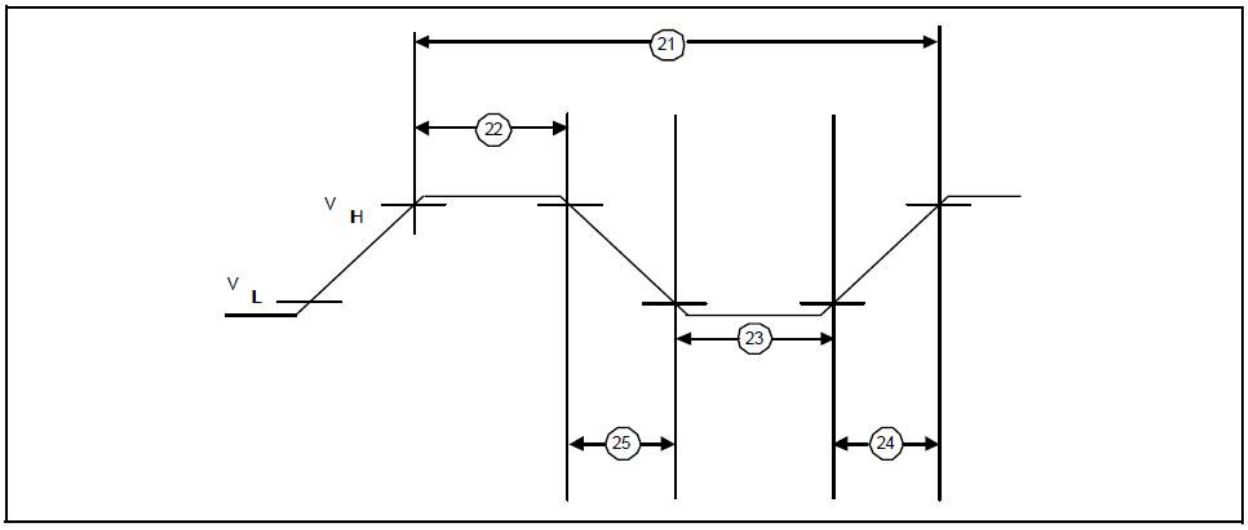


Figure 6-4. PCM Highway Timing for XE = 0 (Transmit on Negative PCLK Edge)

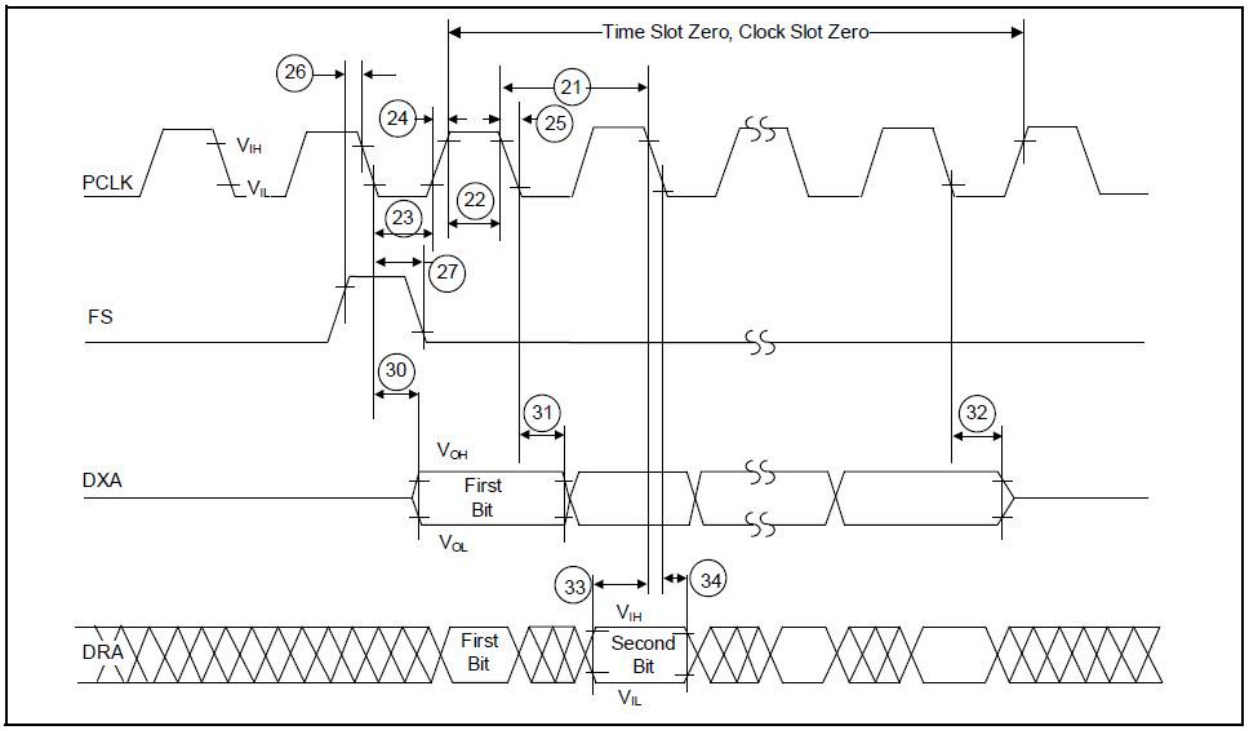
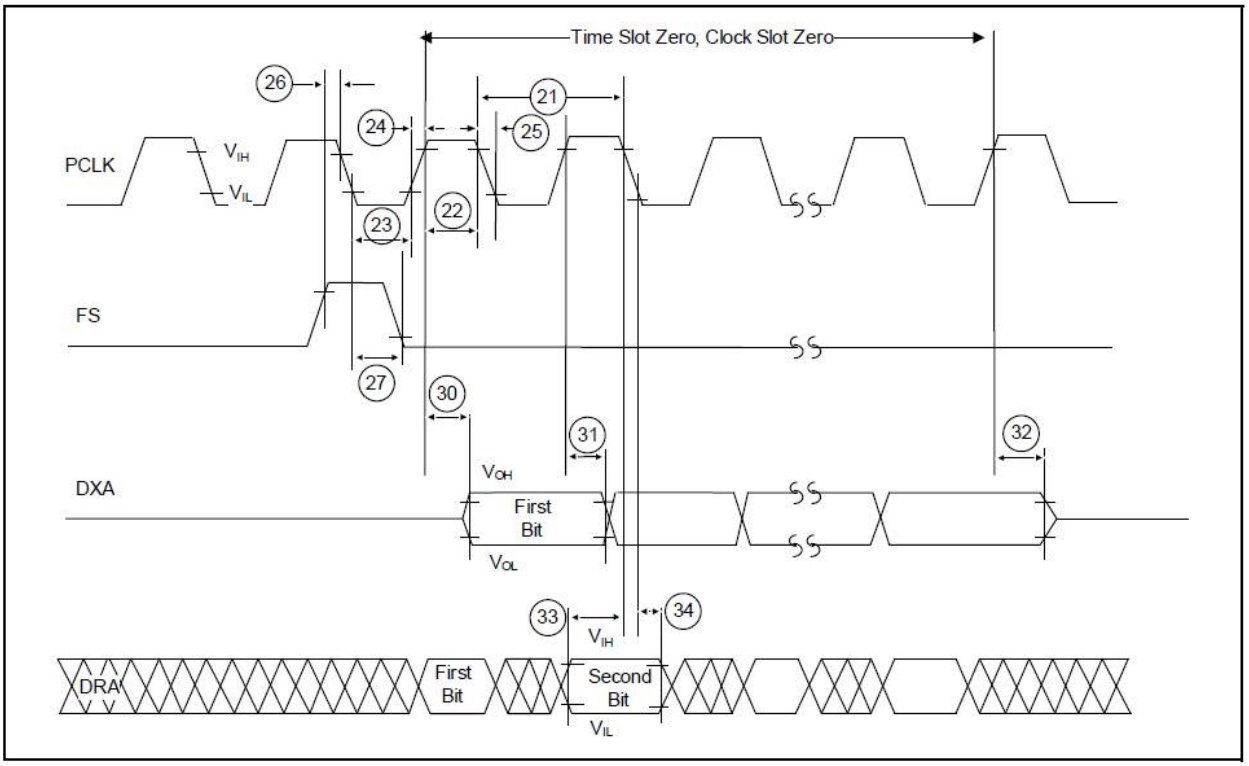


Figure 6-5. PCM Highway Timing for XE = 1 (Transmit on Positive PCLK Edge)



6.2 ZSI Interface

ZCLK shall not exceed 8.192 MHz. All input setup and hold, and output delay and hold times are relative to either edge of ZCLK. Unless otherwise specified, the ZSI timing values are valid for VDDHPI = 1.8 V_{DC}, 2.5 V_{DC}, or 3.3 V_{DC}. See the following figure for the ZSI interface timing diagram.

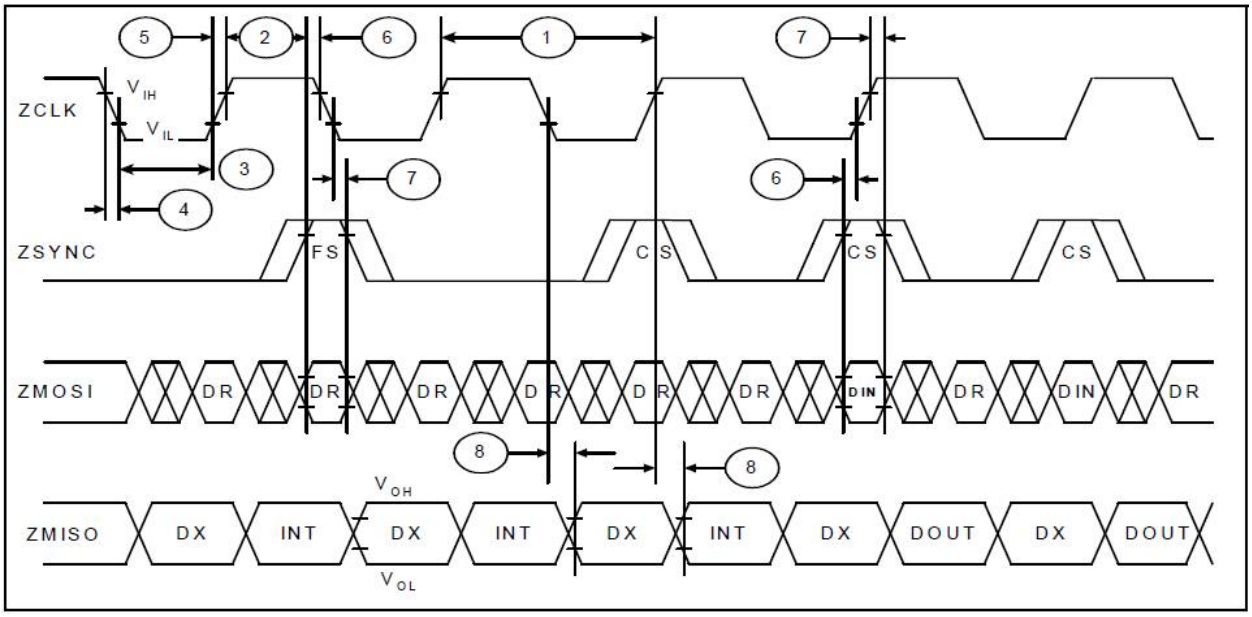
Table 6-3. ZSI Interface Parameters

No.	Symbol	Parameter	Min[3]	Typ	Max[3]	Unit	Note
1	t_{ZCY}	ZSI Clock (ZCLK) period	122		977	ns	1
2	t_{ZCH}	ZCLK high pulse width	48				
3	t_{ZCL}	ZCLK low pulse width	48				
4	t_{ZCF}	ZCLK fall time			8		
5	t_{ZCR}	ZCLK rise time			8		
6	t_{ZSS}	ZSYNC setup time	5				2
	t_{SIS}	ZMOSI device input setup time	5				
7	t_{ZSH}	ZSYNC hold time	0				2
	t_{SIH}	ZMOSI device input hold time	0				
8	t_{ZSOD}	ZMISO device output delay	0	16	30		2
9	t_{ZST}	Allowed ZCLK or ZSYNCFS jitter time	-25		25		2

Note:

1. The ZCLK frequency must be an integer multiple of the ZSYNC frequency. The ZSYNC FS is expected to be an accurate 8 kHz (Narrow- band or Wideband) or 16 kHz (Wideband) pulse train. The minimum frequency is 1.024 MHz and the maximum frequency is 8.192 MHz. If ZCLK has jitter, care must be taken to ensure that all setup, hold, and pulse width requirements are met.
2. ZSYNC, ZMOSI, and ZMISO contain dual data rate signals which are sampled or driven on both edges of the ZCLK clock.
3. Individual timing parameters guaranteed by correlation to device functionality testing.

Figure 6-6. ZSI Interface Timing Protocol



6.3 Switcher Output Timing

Switcher timing varies with switching regulator design and applied voltage. Values are device defaults and are shown for information purposes only. See the following figure for a typical SWOUTY timing diagram.

Table 6-4. Switcher Output Timing Parameters

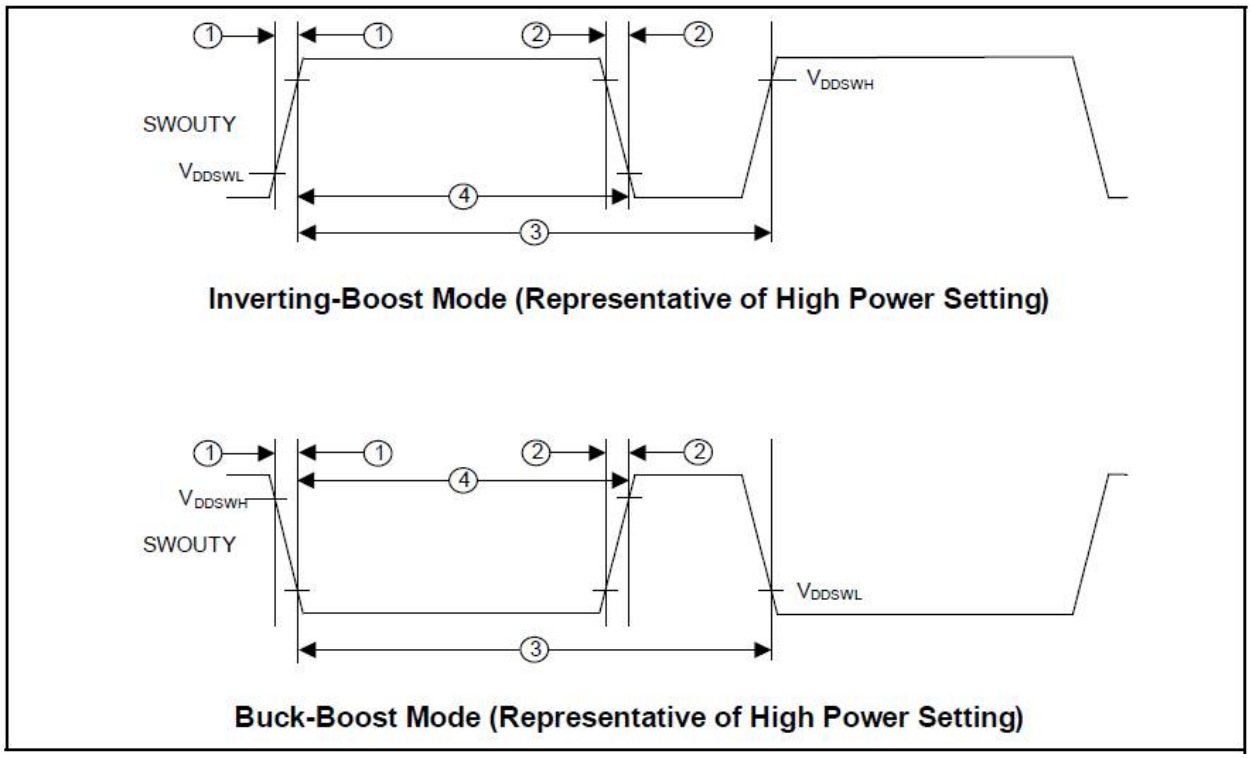
No.	Symbol	Parameter	Min	Typ	Max	Unit	Notes
1	Tfall	Output fall time		15		ns	1
2	Trise	Output rise time		30			
3LP	TPeriod	Period for Low Power mode		41.626		µs	2 and 5
4LP	Tmax	Max on-time for Low Power mode		1.017			
3MP	TPeriod	Period for Medium Power mode		3.337			3 and 5
4MP	Tmax	Max on-time for Medium Power mode		1.017			
3HP	TPeriod	Period for High Power mode		2.035			4 and 5
4HP	Tmax	Max on-time for High Power mode		1.017			
-	Duty Cycle LP	Duty cycle Low Power mode	0	2.5		%	2 and 5
-	Duty Cycle MP	Duty cycle Medium Power mode	0	30.4			3 and 5
-	Duty Cycle HP	Duty cycle High Power mode	0	52.0			4 and 5
-		SWISY leading edge blanking period		120		ns	6

Note:

1. Measured with a 1.5 nF load between $SWOUT_X$ and ground.

2. Register E6/E7h Write/Read Switching Regulator Control is loaded with Low Power mode 01h.
3. Register E6/E7h Write/Read Switching Regulator Control is loaded with Medium Power mode 02h.
4. Register E6/E7h Write/Read Switching Regulator Control is loaded with High Power mode 03h.
5. Timing values assume SWFS[1:0] = 00b in E4/E5h Write/Read Switching Regulator Parameters. Stated periods and on times scale inversely with frequency selected.
6. This is a programmable setting with the default value shown here. This value is automatically set by Profile Wizard.

Figure 6-7. Switcher Output Waveform SWOUTY



7. Device Pin Out

The pins of the Le9643 device are listed and described in this section. Note that there are no ground pins. All ground connections inside this device are made through the exposed pad.

Figure 7-1. Le9643 Device Pin Out (36-Pin QFN) – Top View

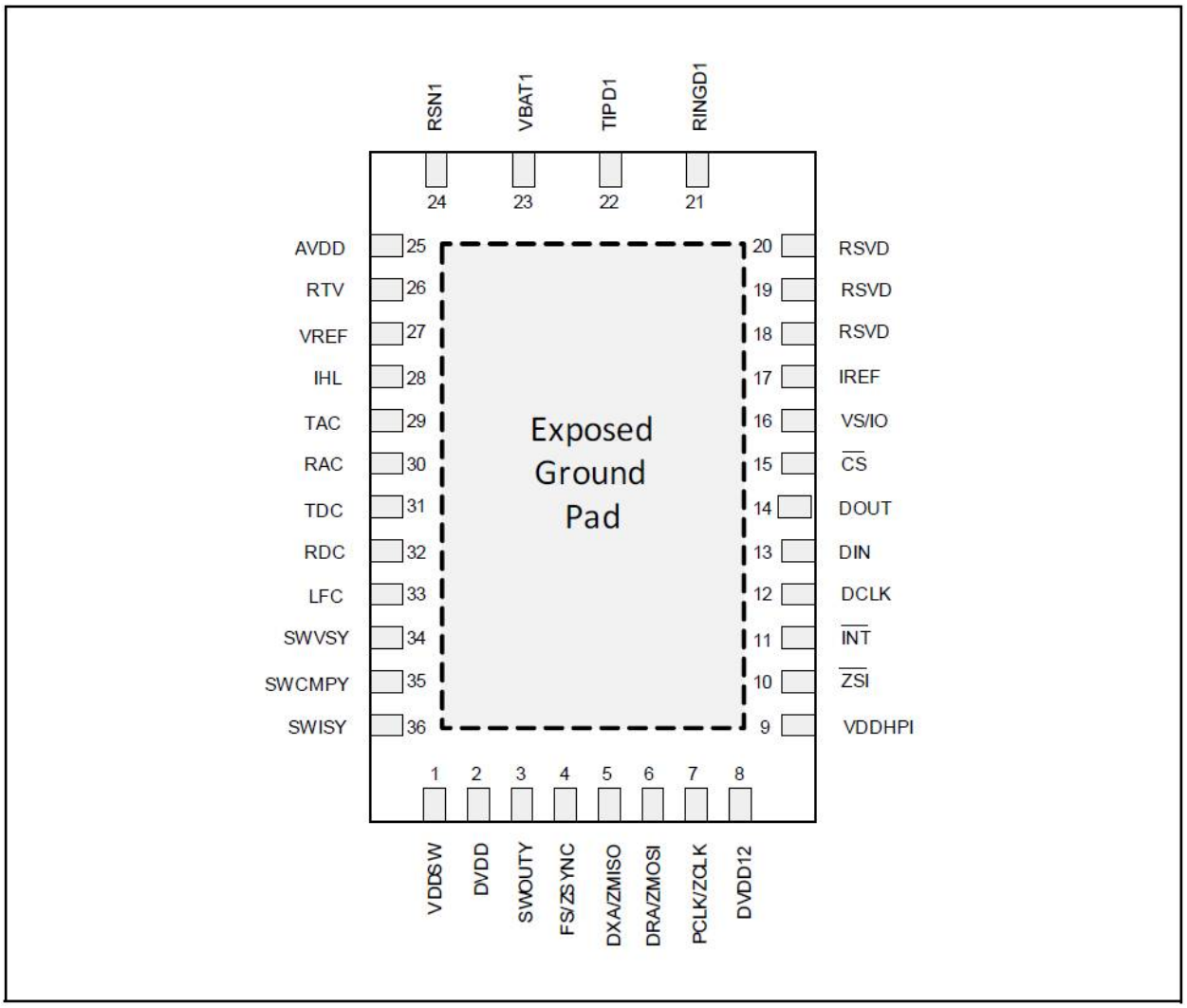


Table 7-1. Device Pin Out Parameters

Pin	Name	Type	Description
1	VDDSW	Power	This voltage is used to drive the switching regulator circuit and is dependent upon the switching regulator design used. This pin must be connected to a +3.3 V supply for bipolar Buck-Boost designs. Place a ceramic decoupling capacitor between this pin and ground.
2	DVDD	Power	+3.3 V Digital power supply inputs. For best performance, all of the VDD power supply pins should be connected together at the power supply or power connection to the printed circuit board.
3	SWOUTY	Output	Pulse output for gate drive to switching regulator transistor.
4	FS/ZSYNC	Input	Interface synchronization signal for PCM voice (in PCM and SPI mode) or for multiplexed PCM voice and control channels (in ZSI mode).
5	DXA/ZMISO	Output	PCM or ZSI Data Input. PCM voice (in PCM and SPI mode) or multiplexed PCM voice and control data (in ZSI mode) is written serially into the device though this pin, most significant bit first. PCLK/ZCLK determines the data rate.
6	DRA/ ZMOSI	Input	PCM or ZSI Data Output. PCM (in PCM and SPI mode) or multiplexed PCM voice and control data (in ZSI mode) is written serially out of the device through this pin, most significant bit first. PCLK/ZCLK determines the data rate.
7	PCLK/ZCLK	Input	PCM or ZSI Data Clock 1.024 to 8.192 MHz. This is the clock for the PCM (in PCM and SPI mode) or ZSI (in ZSI mode) interfaces.
8	DVDD1V2	Output	Internally generated 1.2 V supply. Connect a 0.1 µF ceramic decoupling capacitor between this pin and ground.
9	VDDHPI	Output	Digital power supply input for SPI and PCM/ZSI pins. Place a 0.1 µF ceramic decoupling capacitor between this pin and ground.
10	$\overline{\text{ZSI}}$	Input	ZSI Mode Select. Connect to ground with a 10 KΩ resistor for ZSI mode or to VDDHPI for PCM and SPI mode.
11	$\overline{\text{INT}}$	Output	Interrupt. INT is an active low output signal, which is programmable as either 3 V CMOS compatible or open drain (with external 4.7 KΩ pull-up resistor to VDDHPI required). This pin features a weak (1.0 MΩ) internal pull-up to VDDHPI. When using ZSI mode, this pin is active even if the ZSI clocks are not present (if operating in Free Run mode and the host is not configured for shutdown on a clock fault).
12	DCLK	Input	Data Clock. In the PCM and SPI mode, the Data Clock input shifts data into and out of the microprocessor interface of the device. The maximum clock rate is 8.192 MHz. This pin features a weak (1.0 MΩ) internal pull-up to VDDHPI.
13	DIN	Input	Data Input. In the PCM and SPI mode, control data is serially written into the device via the DIN pin, most significant bit first. The Data Clock determines the data rate. This pin features a weak (1.0 MΩ) internal pull-up to VDDHPI.
14	DOUT	Output	Data Output. In the PCM and SPI mode, control data is serially written out of the device via the DOUT pin, most significant bit first. The Data Clock determines the data rate. DOUT is high impedance except when data is being transmitted, which allows DIN and DOUT to be directly tied together in systems which use a single line for data input and output. This pin features a weak (1.0 MΩ) internal pull-up to VDDHPI.

.....continued

Pin	Name	Type	Description
15	$\overline{CS}$	Input	In the PCM and SPI mode, the Chip Select input (active low) enables the device so that control data can be written to or read from the part. This pin features a weak (1.0 MΩ) internal pull up to VDDHPI.
16	VS/IO	I/O or Input	General Purpose Input/ Output or Voltage Sense. When configured as a voltage sense input, connect a 1.0 MΩ 1% resistor between this pin and the voltage to be monitored. The maximum working voltage rating of the resistor must be higher than the monitored voltage.
17	IREF	Input	Current Reference. An external resistor RREF connected between this pin and analog ground generates an accurate current reference used by the analog circuits on the chip.
18 19 20	RSVD	-	Reserved. Make no connections to these pins.
21	$RINGD_1$	Output	RING-lead (B) output to the two-wire line.
22	$TIPD_1$	Output	TIP-lead (A) output to two-wire line.
23	$VBAT_1$	Supply	Negative Battery Supply. Used for all states.
24	RSN_1	Input	High voltage line drive receive current summing node.
25	AVDD	Power	+3.3 V Analog supply inputs.
26	RTV	Output	Drive output for two-wire AC impedance scaling resistor.
27	VREF	Output	Analog Voltage Reference. The VREF output has an external capacitor connected to ground, filtering noise present on the internal voltage reference.
28	IHL	Output	High Level Current Drive Filter.
29	TAC	Input	Tip lead AC Sense. A series R + C network is connected from this pin to the Tip lead.
30	RAC	Input	Ring lead AC sense. A series R + C network is connected from this pin to the Ring lead.
31	TDC	Input	Tip lead DC Sense. A resistor is connected from this pin to the Tip lead. The connection can be to either side of the protection resistor.
32	RDC	Input	Ring lead DC Sense. A resistor is connected from this pin to the Ring lead. The connection can be to either side of the protection resistor.
33	LFC	Output	Connection for longitudinal filter capacitor.
34	SWVSY	Input	Voltage sense for switching regulator controller.
35	SWCMPY	Output	Compensation connection for switching regulator controller.
36	SWISY	Input	Current sense input for switching regulator controller.
-	Exposed Ground Pad	Power	Thermal Pad and Circuit Ground. Connect to a ground plane on the printed circuit board for thermal conduction and electrical connection to ground return. This is the only ground connection on the device.

8. Application Information

8.1 Line Interface Circuit

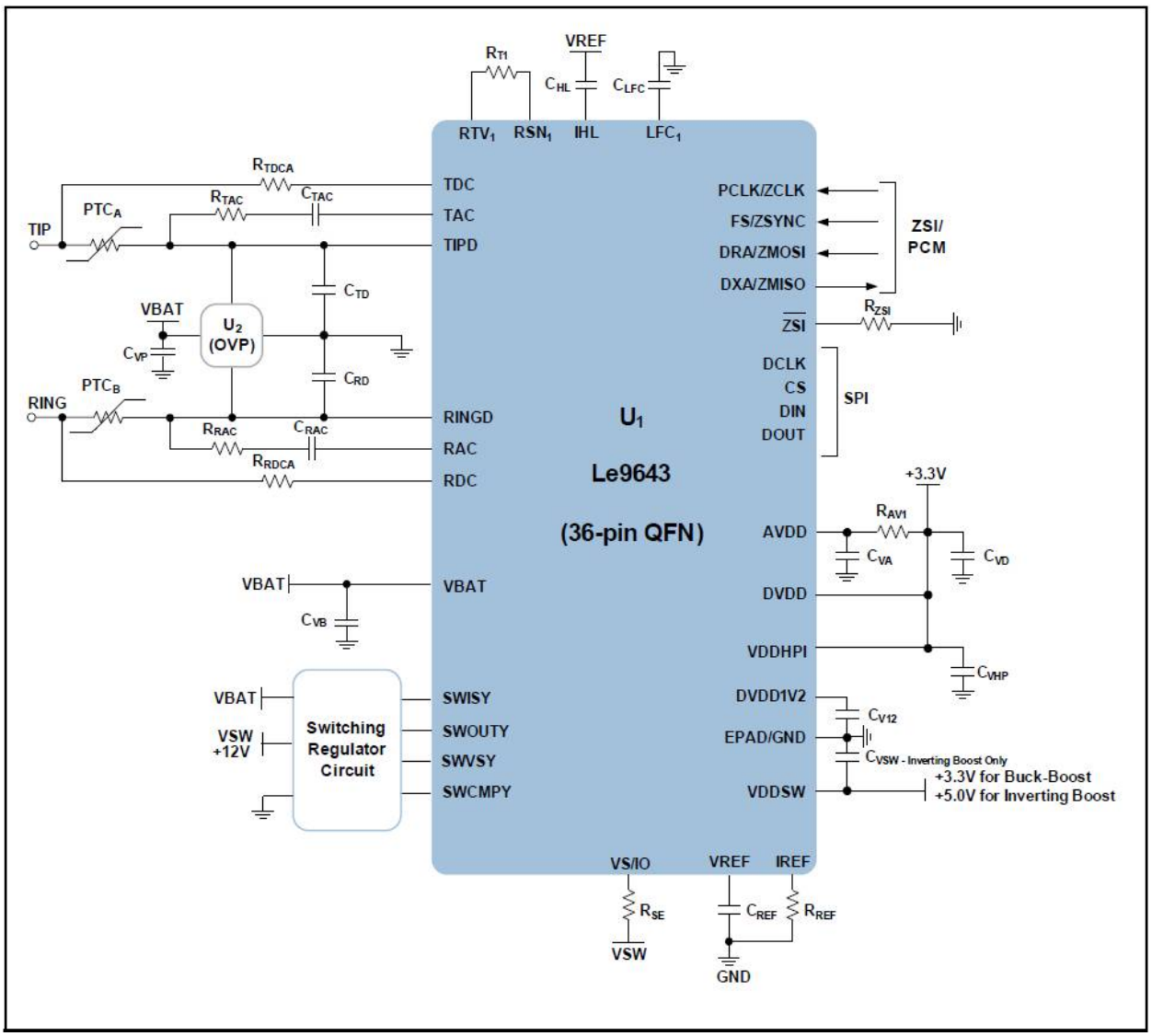
The following figure shows a typical line interface circuit for the Le9643. The ZSI control interface is illustrated.

The switching regulator circuit can be configured for Buck-Boost fixed tracking or Inverting-Boost operation. Decoupling, filtering, reference generation components, and protection are shown. Consult Microchip for the most recent reference design.

The parts list for this circuit is shown in the Line Interface Circuit Bill of Materials section.

The Buck-Boost switching regulator circuit is detailed in the Buck-Boost Switching Regulator Circuit figure. The Inverting-Boost switching regulator circuit is detailed in the 90V Inverting-Boost Switching Regulator Circuit figure.

Figure 8-1. Le9643 Line Interface Circuit (ZSI Configuration shown)



8.2 Line Interface Circuit Bill of Materials

Table 8-1. Line Interface Circuit Components

Qty.	Item	Type	Value	Tol.	Rating	Size	Part Number / Note
4	C_{HL}, C_{VA}, C_{VD}, C_{LFC}	Ceramic Capacitor	4.7 µF, X5R	20%	6.3 V	0402	
3	C_{V12}, C_{VA}, C_{VSW}	Ceramic Capacitor	0.1 µF, X7R	10%	16 V	0402	
4	C_{RAC}, C_{RD1}, C_{TAC}, C_{TD}	Ceramic Capacitor	0.022 µF, X7R	10%	100 V	0603 or 0805	
1	C_{REF}	Ceramic Capacitor	1 µF, X5R	10%	10 V	0603	1 µF to 10 µF
1	C_{VB}	Ceramic Capacitor	0.01 µF, X7R	10%	100 V	0603	
2	C_{VD}, C_{VHP}	Ceramic Capacitor	0.01 µF, X7R	10%	16 V	0402	
1	C_{VP}	Ceramic Capacitor	0.1 µF, X7R	10%	100 V	0805 or 0603	
2	P_{TC1}	Dual Matched PTC Thermistors	7 Ω, 0.13 A Hold	20%	250 V_{RMS} / 3A		1 and 2
1	R_{AV1}	Resistor	2.0 Ω	5%	1/10 W	0402	
2	R_{RAC}, R_{TAC}	Resistor	10 KΩ	1%	150 V	0603	
2	R_{RDCA}, R_{TDCA}	Resistor	1.0 MΩ	1%	200 V	1206	
1	R_{REF}	High-Precision Thin Film Resistor	75.0 KΩ	0.5%, 25ppm	1/16 W	0402	3
1	R_{SE}	Resistor	1.0 MΩ	1%	50 V	0402	4
1	R_T	Resistor	47.5 KΩ	1%	1/16 W	0402	
1	R_{ZSI}	Resistor	10 KΩ	1%	1/16 W	0402	
1	U_1	IC, miSLIC™				QFN-36	Microchip Le9643
1	U_2	IC, Programmable SLIC Protector			-150 V/30 A	SOIC-8	1, Bourns TISP61089B or equivalent

Note:

1. Protection components depend on the target application. The components on the BOM are believed to be suitable for ITU-T Recommendation K.21 (Basic Level) and Telcordia GR-1089-CORE Intra-Building compliance. Please check with Microchip for component selection for other safety or EMC standards.
2. Recommended dual PTCs include Bourns CMF-SDP07 or MF-SD013/250.
3. The tolerance and stability of this resistor are critical as they affect calibration and measurement accuracy. Microchip recommends using resistors with 0.5% tolerance and 25 ppm/°C temperature coefficient for most applications. Examples include Susumu RR0510P-753-D, Panasonic ERA-2AED753X, and Yageo

RT0402DRD0775KL. For high-performance applications, 0.1% 25 ppm/°C resistors such as Panasonic ERA-2AEB753X or Yageo RT0402BRD0775KL are recommended.

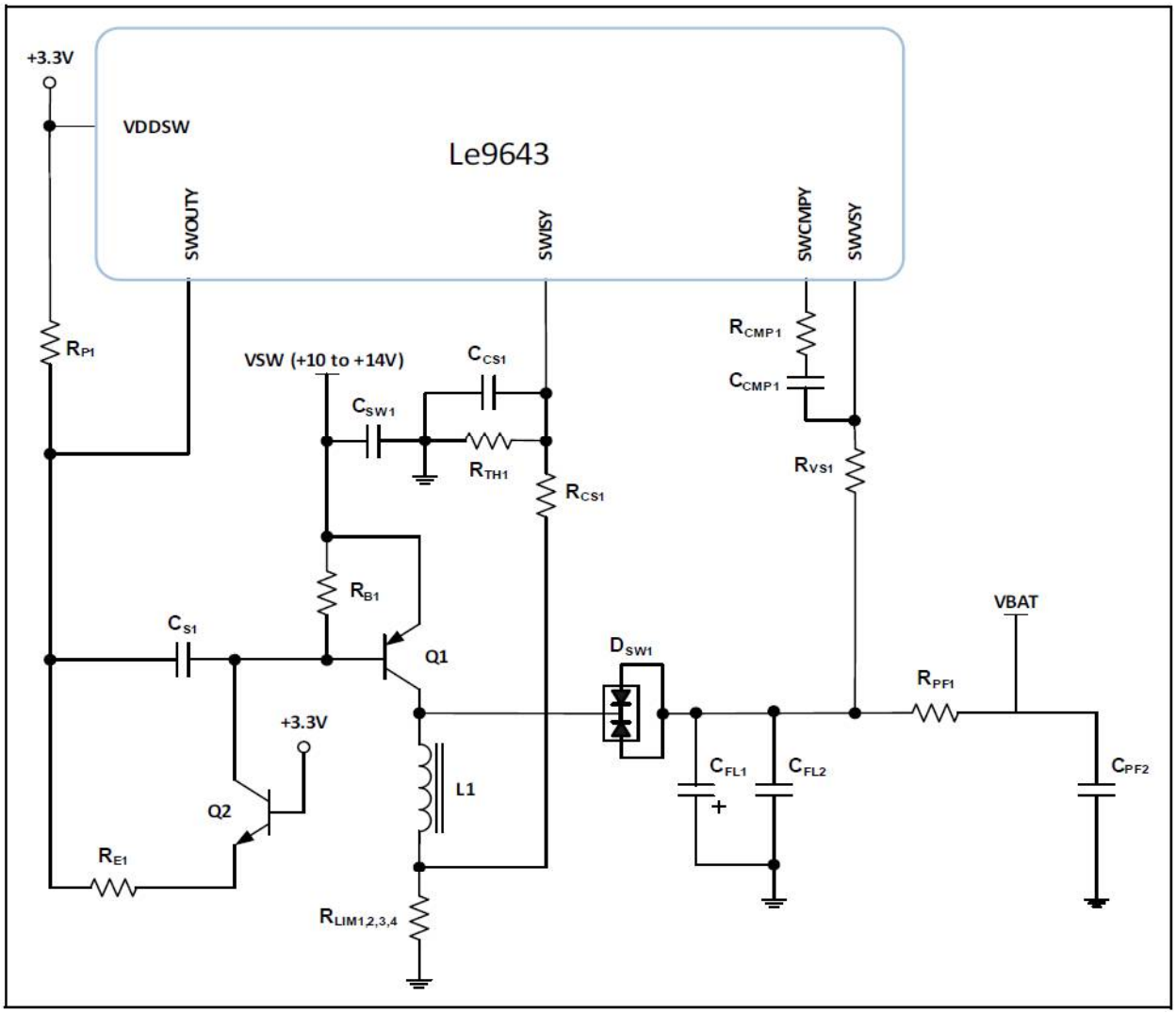
4. Populate only to sense the voltages shown on the schematic. Always make sure that this resistor is selected so that the maximum working DC voltage rating is more than the desired sensed voltage.

8.3 Buck-Boost Switching Regulator Circuit

The Buck-Boost fixed tracker switching regulator circuit and BOM are presented here.

The circuit is capable of driving 60VRMS ringing into a 3 REN load or 50VRMS ringing into a 5 REN load with appropriate component selection. The circuit uses +12 V for VSW, +5 V versions (with reduced drive capability) are available.

Figure 8-2. Buck-Boost Switching Regulator Circuit



8.4 Buck-Boost Switching Regulator Circuit Bill of Materials

Table 8-2. Buck-Boost Switching Regulator Components

Qty.	Item	Type	Value	Tol.	Rating	Size	Part Number / Note
1	C_{CMP1}	Ceramic Capacitor	0.0022 µF, X7R	10%	16 V	0402	
1	C_{CS1}	Ceramic Capacitor	220 pF, X7R	10%	25 V	0402	
1	C_{FL1}	Electrolytic Capacitor	10 µF	20%	100 V		
2	C_{FL2}, C_{PF2}	Ceramic Capacitor	0.1 µF, X7R	10%	100 V	0603	
1	C_{S1}	Ceramic Capacitor	0.1 µF, X7R	10%	25 V	0603	Do not use 0402
1	C_{SW1}	Ceramic Capacitor	10 µF, X5R	20%	25 V	1206	
1	D_{SW1}	Dual Diode	BAV23C		150 V	SOT23	600mA Repetitive Rating
1	L1	Power Inductor	47 µH	20%	1.2 A I_{SAT}		
1	Q1	Transistor	PNP, Low Vce		140 V	SOT89	*ZXTP2014Z Diodes Inc.® or equivalent*[1]
1	Q2	Transistor	NPN			SOT23	*MMBT3904 Diodes Inc.® or equivalent*
1	R_{B1}	Resistor	1 KΩ	5%	1/16 W	0402	
1	R_{E1}	Resistor	120Ω	5%	1/10 W	0603	
1	R_{CMP1}	Resistor	1.0 MΩ	1%	1/16 W	0402	
1	R_{CS1}	Resistor	2.32 KΩ	1%	1/16 W	0402	
1	R_{PF1}	Resistor	20 Ω	5%	1/4 W	1206	
4	R_{LIM1}, R_{LIM2}, R_{LIM3}, R_{LIM4}	Resistor	1.0 Ω	5%	1/16 W	0402	
1	R_{P1}	Resistor	10 KΩ	5%	1/16 W	0402	
1	R_{TH1}	Resistor	1 KΩ	1%	1/16 W	0402	
1	R_{VS1}	Resistor	1.0 MΩ	1%	1/8 W	0805	

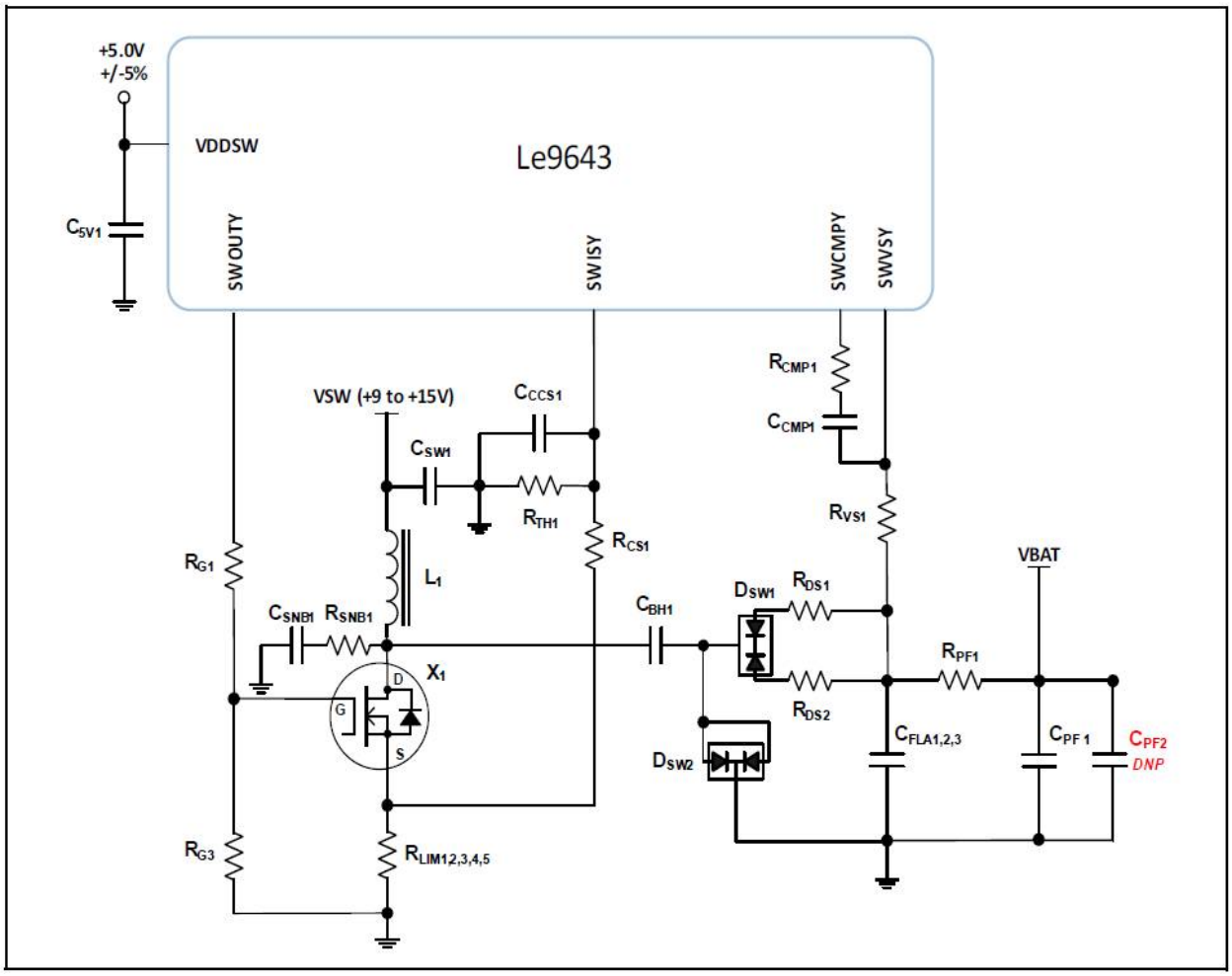
Note: The ZXTP2013G is acceptable for ringing up to 50 V_{RMS}, for ringing > 50 V_{RMS} use a ZXTP2014G, 140 V PNP or equivalent.

8.5 Inverting-Boost Switching Regulator Circuit

The Inverting-Boost switching regulator circuit and BOM are presented here.

The circuit is capable of driving 70-VPK ringing into 5 REN and 85-VPK into 3 REN when tracking the ringing voltage during ringing. The circuit uses +12 V for VSW, +5 V versions (with reduced drive capability) and lower REN options are available.

Figure 8-3. 90V Inverting-Boost Switching Regulator Circuit



8.6 90V Inverting-Boost Switching Regulator Circuit Bill of Materials[1]

Table 8-3. 90V Inverting-Boost Switching Regulator Components

Qty.	Item	Type	Value	Tol.	Rating	Size	Part Number / Note
1	C_{BH1}	Ceramic Capacitor	0.22 µF, X7R	10%	100 V	0805	
1	C_{CMP1}	Ceramic Capacitor	1.8 nF, X7R	10%	16 V	0402	
1	C_{CCS1}	Ceramic Capacitor	220 pF, X7R	10%	50 V	0402	

.....continued

Qty.	Item	Type	Value	Tol.	Rating	Size	Part Number / Note
3	C_{FL1}, C_{FL2}, C_{FL3}	Ceramic Capacitor	0.1 µF, X5R/X7R	10%	100 V	0805	
2			0.22 µF, X5R/X7R				
1			0.47 µF, X5R/X7R			1206	
1			1.0 µF, X5R/X7R				
1	C_{PF1}, C_{PF2}	Ceramic Capacitor	0.1 µF, X5R/X7R	10%	100 V	0805	*CPF2 Optional*
1	C_{SW1}	Ceramic Capacitor	4.7 µF, X5R or X7R	20%	25 V	0805	
1	C_{5V1}	Ceramic Capacitor	0.1 µF, X7R	10%	16 V	0402	
1	C_{SNB1}	Ceramic Capacitor	220 pF, X7R	10%	100V	0603	
2	D_{SW1}, D_{SW2}	Dual Diode	trr ≤ 50 nS		0.4 A/ 200 V	SOT-23	*Diodes Inc BAV23C* *NXP BAV23C* *On Semi BAV23CL* *Fairchild BAV23C*
1	R_{CMP1}	Resistor	1.0 MΩ	1%	1/16 W	0402	
1	R_{CS1}	Resistor	2.74 KΩ	1%	1/16 W	0402	1.0 KΩ if R_{LIM} is 0.05Ω
2	R_{DS1}, R_{DS2}	Resistor	2 Ω	5%	1/16 W	0603	
1	R_{G1}	Resistor	10 Ω	5%	1/16 W	0402	
1	R_{G3}	Resistor	10 KΩ	5%	1/16 W	0402	
5	$R_{LIM1/2/3/4/5}$	Current Sense Resistor	1.0 Ω	5%	1/16 W	0402	For lower power consumption, replace these resistors with one 0.05 Ω resistor (0603).
1	R_{PF1}	Resistor	20 Ω	5%	200 V/ 1/4 W	0805	
1	R_{TH1}	Resistor	1.0 KΩ	1%	1/16 W	0402	
1	R_{VS1}	Resistor	1.0 MΩ	1%	1/8 W	0805	
1	R_{SNB1}	Resistor	100 Ω	5%5	1/4 W	1206	

.....continued

Qty.	Item	Type	Value	Tol.	Rating	Size	Part Number / Note
1	L_1	Power Inductor	10 µH, I_{SAT} ≥ 1.9 A - 12V 4.7 µH, I_{SAT} ≥ 2.5 A - 5V	30%		6x6 or 8x8 mm	*For 12V Applications Bourns SRN6028-100M* *Taiyo Yuden NR6028T 100M NIC NPIS63LS100MTRF*
1	X_1	MOSFET, N-Channel	$R_{DS\ (ON)}$ ≤ 250 mΩ, V_{DS} 100V V_{GS} 4.5V Qg(total) at VGS = 4.5 V: <8 nC recommended			SOT-23 SOT6	*SOT-23 100V* *IR IRLML0100TRPbF* *Diodes Inc. DMN10H220L Vishay Si239DS* *Toshiba SSM3K361R*

Note: *For information only, not for Design Purposes.* Please see ZLR965324H Reference Design User Guide for the Le9643 and Le9653 miSLIC™ Device, Document Number 159172 for the latest Reference Design.

9. Programming the Le9643

The Le9643 device is programmed through the *VoicePath Application Program Interface II (VP-API-II).* This API hides the complexity of the device and its internal registers and provides a much simpler interface to the software engineer. The *VP-API-II* allows for rapid development on proven software that is currently used to control over 100 million subscriber lines worldwide.

9.1 Programmable Features

- AC and DC coefficient programming
- Ringing parameter (amplitude, frequency, bias, type) and power management
- Tone generation (frequency, amplitude, and modulation)
- Programmable tone and ringing cadence
- Universal Caller ID generation (Types 1 and 2) with FSK and DTMF signaling
- Loop start signaling, including dial pulse detection
- Ground start signaling
- Seamless integration of the Microchip *VeriVoice Professional Test Suite Software* for *Telcordia® GR-909- CORE* metallic loop testing
- Three modes of interrupt support (Level Triggered, Efficient Polling and Simple Polling)

9.2 VoicePath API-II Software Overview

The *VP-API-II* is an OS independent, C source library that abstracts the Microchip ZL880, VE790, VE880, VE890 and miSLIC™ device registers into a common application interface used for configuration and control of the devices.

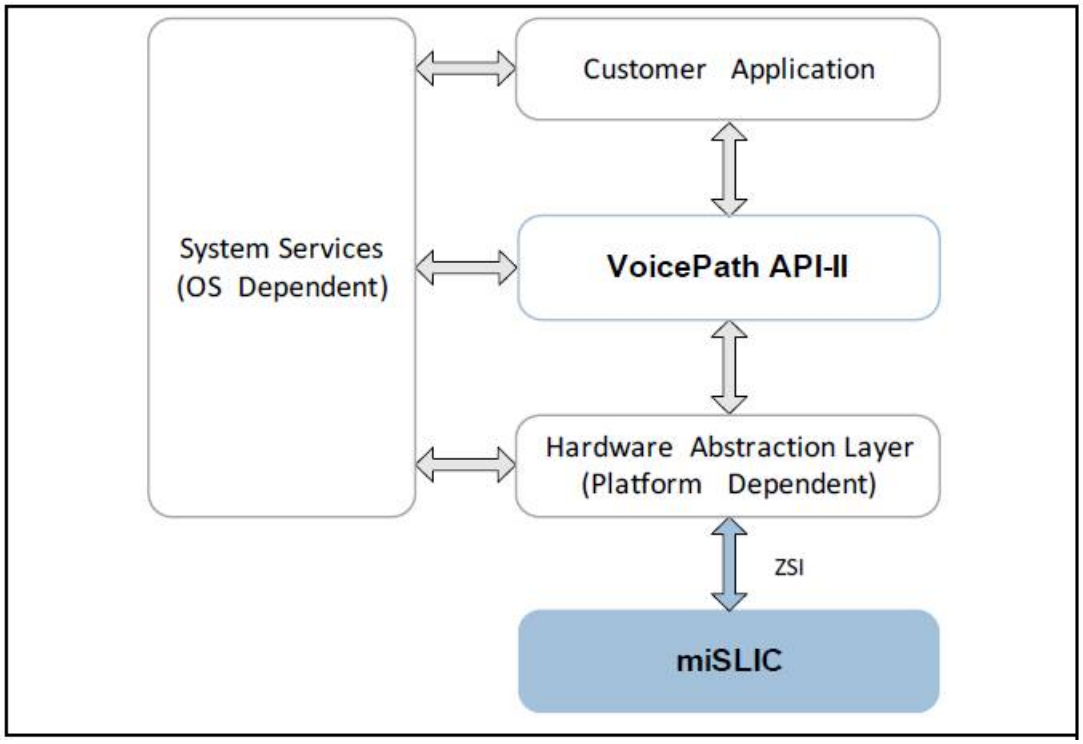
The *VP-API-II* is available from the Microchip Line Circuits web page. The software package (*LE71SK0002*) contains the source code and requires a Software License Agreement (SLA). The miSLIC device is supported by *VP-API-II* versions 2.25.0 and later.

The following sections cover the more commonly used aspects of the *VP-API-II*. See the *VoicePath API-II Reference Guide (included in the LE71SK002 package)* for complete coverage of this software.

9.2.1 Introduction to VoicePath API-II

The Microchip V*oicePath Application Programming Interface II* (*VP-API-II*) is a C source code module that provides a standard software interface for controlling, testing, and passing digitized voice through a set of subscriber lines using the Microchip family of voice termination devices. This section describes a few of the device and line control capabilities using the *VP-API-II* interface. For a complete list, refer to *VP-API-II Reference Guide*. *VP-API-II* uses the layered architecture shown in the figure below (ZSI control). The block in the diagram in blue outline and bold print is Microchip-provided code, the blocks in gray outline are customer-provided code. The solid blue block is the actual Microchip device.

Figure 9-1. VP-API-II Software Architecture



9.2.2 Customer Application

This block represents the user's line management module that performs tasks such as initializing the system, configuring lines, changing the line states in response to line events and other inputs, switching digitized voice traffic, etc. Microchip provides example implementations of this layer as part of the *VoicePath SDK*.

9.2.3 VoicePath API-II

The *VoicePath API-II* is the core component of the Microchip *VoicePath SDK*. This software module runs on the host microprocessor that controls one or more Microchip voice telephony devices. This code is provided by Microchip and should not require modification by the application developer.

9.2.4 Hardware Abstraction Layer

The Hardware Abstraction Layer (HAL) provides access to Microchip voice telephony devices through the SPI or multiplexed ZSI interface. The HAL software is platform-dependent and must be implemented by the *VP-API-II* user. Microchip provides example HAL source code with the *VoicePath SDK*.

9.2.5 System Services Layer

The System Services layer provides critical section, timing and interrupt control functions. These functions are system-dependent and must be implemented specifically for each platform on which the *VP-API-II* is used. Example code is provided with the VP-API-II LE71SK0002 software package. The following functions are included in the System Services layer.

Table 9-1. VP-API-II Functions for System Services

Function Name	Description
`VpSysEnterCritical()`	A semaphore operation to provide protected access to device or shared memory. Required only in multi-threaded architectures.
`VpSysExitCritical()`	A semaphore operation to release protected access to device or shared memory. Required only in multi-threaded architectures.

.....continued	
Function Name	**Description**
VpSysWait()	Delay operator used to suspend program/thread execution. Delay parameter passed in 125 µs steps.
VpSysDebugPrintf()	Print mechanism used by *VP-API-II* debug features.
VpSysTestInt()	Interrupt function for Efficient Poll Mode. Required for backward compatibility with *VE880* code.

9.3 System Configuration Functions

Two main functions in *VP-API-II* are required in all applications are listed below:

Table 9-2. VP-API-II Functions for System Configuration

Function Name	Description
VpMakeDeviceObject()	Configures a specific device (chip select) to a device context. Provides *VP-API-II* with device specific type (*deviceType*).
VpMakeLineObject()	Configures a specific line (channel) to a line and device context. Provides *VP-API-II* with line specific type (*termType*).

When using the Le9643 device, the following settings must be used:

- The value for *deviceType* in VpMakeDeviceObject() must be: VP_DEV_886_SERIES or VP_DEV_887_SERIES
- The value for *termType* in VpMakeLineObject() must be:
  - VP_TERM_FXS_GENERIC when *channelId*= 0 and Normal Standby operation is desired
  - VP_TERM_FXS_LOW_PWR when *channelId*= 0 and Low Power Standby operation is desired.

Please refer to *VP-API-II Reference Guide* for additional details.

9.4 Initialization

The *VP-API-II* functions that perform initialization are listed below.

Table 9-3. Initialization Functions in VP-API-II

Function Name	Description
VpInitDevice()	Resets and initializes device with parameters defined in the specified *Profiles*.
VpInitLine()	Resets and initializes line with parameters defined in the specified *Profiles*.
VpInitRing()	User function to provide Ringing Cadence. Also allows use selection of *Caller ID Profile* associated with ringing.

9.5 Line State Control

The following sections describe the Line State information to perform control functions such as DC feed, ringing generation, and channel line test.

Table 9-4. VP-API-II Functions for Line State Control

Function Name	Description
VpSetLineState()	Sets line to state specified. After VpInitDevice() or VpInitLine(), the default line state is VP_LINE_DISCONNECT.

9.5.1 VP_LINE_DISCONNECT

In the VP_LINE_DISCONNECT state, the SLIC block outputs are shut off providing a high impedance to the line. This state can be used for denial of service. The switching regulator is active and outputs the programmed SWFV floor voltage. The voice channel is normally deactivated, but can be activated and used with the converter configuration command to monitor the voltages on Tip or Ring for line diagnostics.

9.5.2 VP_LINE_STANDBY

The VP_LINE_STANDBY state is used when On-Hook. This state behaves differently based on the FXS line termination type selected as per the System Configuration Functions section.

If the termination type VP_TERM_FXS_GENERIC is selected, the DC feed is active, and hook supervision functions are enabled. The loop feed polarity is controlled by the *VP-API-II*. The high voltage switching regulator only generates the voltage needed to support the DC line voltage defined by the DC feed curve shown in the Active State I / V Characteristic figure. The DC feed drives Tip and Ring to the programmed VOC. Voice transmission is disabled to save power.

If the termination type VP_TERM_FXS_LOW_PWR is selected, a special *Low Power Idle Mode (LPIM)* state is supported to reduce on-hook power consumption, while still being able to detect off-hook transitions. In this mode, the DC feed is not active and a voltage is presented to the Ring lead. The line voltage is monitored so that any transitions to off-hook state can be detected. Voice transmission is disabled in this state.

9.5.3 VP_LINE_OHT, VP_LINE_OHT_POLREV

In the VP_LINE_OHT states, the DC feed is activated and voice transmission is enabled. VP_LINE_OHT allows the transmission of Caller ID information. Hook supervision functions are operating. The switching regulator only generates the negative high voltage needed to support the DC line voltage defined by the DC feed curve. In this way, power consumption is minimized.

9.5.4 VP_LINE_ACTIVE, VP_LINE_ACTIVE_POLREV, VP_LINE_TALK, VP_LINE_TALK_POLREV

In the VP_LINE_ACTIVE and VP_LINE_TALK states, the DC feed is activated. The PCM highway is enabled in VP_LINE_TALK and disabled in VP_LINE_ACTIVE. Both states allow the transmission of Caller ID information for Type 2 Caller ID. Hook supervision functions are operating. The switching regulator only generates the negative high voltage needed to support the DC line voltage defined by the DC feed curve. In this way, power consumption is minimized.

9.5.5 VP_LINE_TIP_OPEN

In the VP_LINE_TIP_OPEN state, the device provides a high impedance on the Tip lead and drives the Ring lead to the programmed VOC voltage. The loop supervision detector monitors the ground key current. When this current is larger than the programmed threshold, the *VP-API-II* reports a ground start event. This state can also be used to determine Ring to ground leakage and Ring to ground capacitance in combination with the appropriate converter configuration.

9.5.6 VP_LINE_RING_OPEN

In the VP_LINE_RING_OPEN state, the device provides a high impedance on the Ring lead and drives the Tip lead to the programmed VOC voltage. The loop supervision detector monitors the ground key current. When this current is larger than the programmed threshold, the *VP-API-II* reports a ground start event. This state can also be used to determine Tip to ground leakage and Tip to ground capacitance in combination with the appropriate converter configuration.

9.5.7 VP_LINE_RINGING, VP_LINE_RINGING_POLREV

In the VP_LINE_RINGING state, the voice DAC is used to apply the ringing signal generated from Signal Generator A and the Bias generator to the SLIC block. Internal feedback maintains a low (200 Ω) system output impedance during ringing. The current limit is increased in the *Ringing* state and is programmable via the parameter, ILR. In order to minimize line transients, entry and exit from the VP_LINE_RINGING states are intelligently managed by the Le9643. When ringing is requested by the user, the corresponding signal generators are started but not applied to the subscriber line until the ringing voltage is equal to the on-hook Tip-Ring voltage. This algorithm, known as *Ring Entry*, assures that there is a smooth line transition when entering the VP_LINE_RINGING state. *Ring Entry* is guaranteed to occur within one period of the programmed ringing frequency. *Ring Exit i*s an analogous procedure whereby the ringing signal is not immediately removed from the line after a ring trip or new state request. The ringing signal will persist until its voltage is equal to the required line voltage. Ring Entry and Ring Exit are configured using the *VP-API-II* option VP_OPTION_ID_RING_CNTRL.

While in the VP_LINE_RINGING state, the integrated switching regulator may be programmed. Refer to the Device Profile and Ringing Profile sections for information on setting the switcher topology.

9.5.8 VP_LINE_HOWLER, VP_LINE_HOWLER_POLREV

In the VP_LINE_HOWLER state, the transmit (A to D) voice path and impedance generation are disabled. Gain is increased by 11.5 dB compared to a 0 dBr D/A setting.

9.6 VpShutdownDevice()

This function puts all lines into the VP_LINE_DISABLED state, shuts down all power supplies, stops all timers, and masks all interrupts for the specified device. The device must be reinitialized with VpInitDevice() to be used again.

9.7 Line Status Monitoring

Line status is monitored by the *VP-API-II* using the functions listed in the table below.

Table 9-5. VP-API-II Functions for Line Status Monitoring

Function Name	Description
VpGetEvent()	Typically used to implement event driven method to monitor line status. Provides event queue such that a single event reported for each instance function is called (when an event is active).
VpGetLineStatus()	Typically used to implement polling method to monitor line status.
	• VP_INPUT_HOOK -- Hook Status timing per Dial Pulse Detection.
	• VP_INPUT_RAW_HOOK -- Real time hook status. Changes during Dial Pulse
	• VP_INPUT_GKEY -- Real time ground key status.

9.8 VoicePath API-II Software QuickStarts

The VP-API-II software is distributed with minimalistic examples known as QuickStarts. These examples are intended to provide *VP-API-II* users with a starting point for their end application. The QuickStarts show how to properly setup, initialize, and configure the VP-API. Additionally, the examples show how to properly respond to VP-API events. The QuickStarts code also provide examples of the platform specific Hardware Abstraction Layer and System Service Layer functions discussed in the Hardware Abstraction Layer and System Services Layer sections.

9.9 DTMF

The VP-API II offers a software based DTMF (Dual-tone Multi-frequency) signal detection feature for Microchip miSLIC™ devices. This feature can be used for applications where the host processor does not have access to voice data and therefore cannot run its own DTMF decode algorithm.

10. VP-API-II Profiles

Profiles are structures that contain design data to meet specific system requirements. Many *VP-API-II* functions take *Profiles* as one or more arguments. There are several types of *Profiles*. Each defines a different set of parameters for a service aspect of the device. The table below provides a summary of all the *Profiles* that are used by the *VP-API-II* with the Le9643 device. *Profiles* are created using *VP Profile Wizard*.

Table 10-1. VP-API-II Profile Types

Profile Name	Description
Device	The *Device Profile* provides default start-up values for device-specific configuration options that are normally set at initialization and never changed. These options include the bus clock frequency and configuration information, interrupt mode, voltage monitoring mode, dial pulse correction, device mode register, and switching regulator configuration.
AC FXS	Used for programming the transmission characteristics of the system, the *AC FXS Profile* holds the programmable gain and filter coefficient data. Over 70 country-specific *AC FXS Profiles* are provided and the user can select the one or ones that are required for his or her application.
DC	The *DC Profile* holds the DC feed and loop supervision parameters.
Ringing	The *Ringing Profile* contains the necessary commands and data to set up the ring generator of an FXS channel. Different *Profiles* can be used to vary the ringing characteristics of a line. Options available in the *Ringing Profile* include ringing waveform, frequency, amplitude, DC offset, ring trip method, maximum peak power, and ring cadence control.
Tone	The *Tone Profile* defines the various call progress tones that might be used in the FXS channel. The tones include dial tone, busy, ring-back, re-order, and howler.
Ringing Cadence	The *Ringing Cadence Profile* defines the cadence that is associated with ringing.
Tone Cadence	The *Tone Cadence Profile* defines the various call progress cadences that might be used in a system. The cadences include stutter dial, busy, ring-back, and reorder.
Caller ID	The *Caller ID Profile* defines the on- and off-hook signal generation for services such as Caller ID and message waiting indication. This *Profile* abstracts the physical and data link layers of the protocol. FSK and DTMF signaling are supported.
Metering	The *Metering Profile* sets the frequency (12- or 16-kHz), transition type, peak current, and echo voltage limits.

10.1 Profile Wizard Project Definition

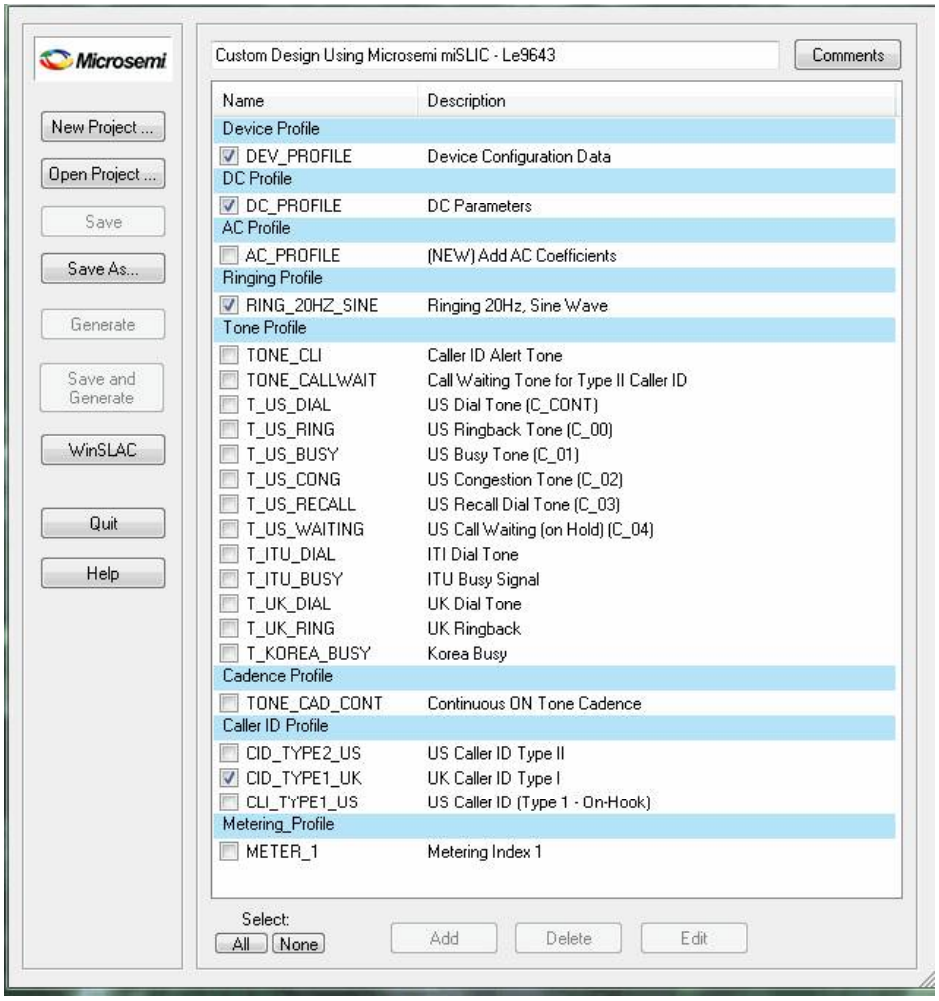
The *Profile Wizard* application allows the user to define the requirements of the telephone line characteristics, switching and signaling with an intuitive user interface. After selecting the requirements, the user can generate the corresponding *Profiles* (.c and.h files) which the *VP-API-II* software uses to initialize and control the Le9643 device. Microchip provides many example *Profiles* based on known country or standard requirements.

After launching *Profile Wizard*, it presents the user with the option of creating a new project based on a Microchip telephony device family or reference design or to open an existing project.

10.2 Profile Wizard Main Menu

The following figure shows a typical screen shot of the main menu of *Profile Wizard* when a device family is selected. Note that the user can select from many standard country *Profiles*.

Figure 10-1. Profile Wizard – Main Menu

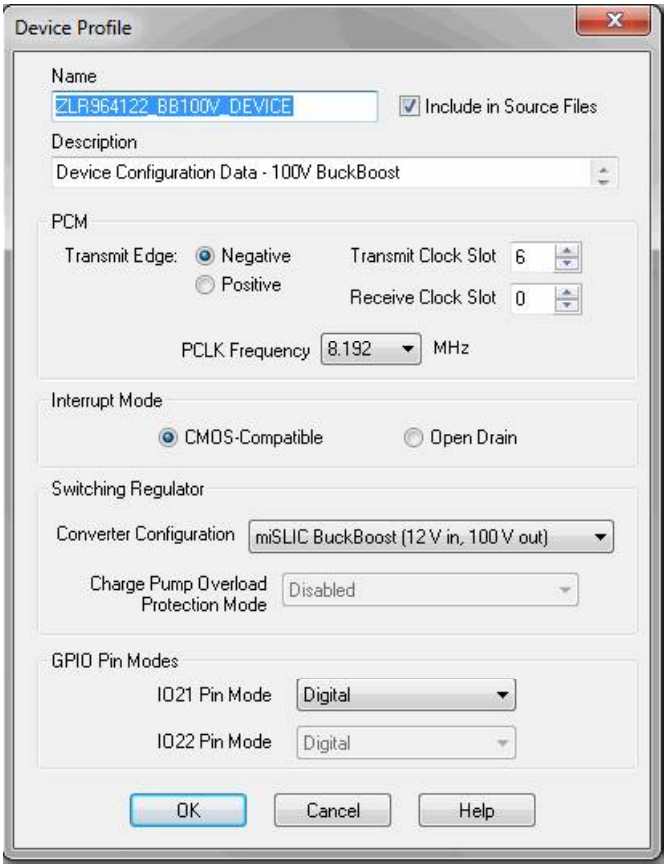


10.3 Device Profile

The *Device Profile* configures device or circuit level parameters for the entire device. This *Profile* is required to enable reliable host communication with the device, to configure the switching regulator, and to define *VP-API-II* driver parameters. An example *Device Profile* is shown in the following figure.

Note: Charge pump and corresponding overload protection is not supported on the LE9643 device.

Figure 10-2. Profile Wizard – Device Profile Configuration



The table below lists the *VP-API-II* functions which use values that are defined in the *Device Profile*.

Table 10-2. VP-API-II Functions For Device Configuration

Function Name	Description
`VpInitDevice()`	Resets and initializes device with parameters defined in *Device Profile* and optionally configures all lines on the device with AC, DC, and Ringing parameters.
`VpCalLine()`	This function may need to be called under some circumstances following the above function. Refer to the *VP-API-II Reference Guide* for more details.

10.4 AC FXS Profiles

AC FXS Profiles are used to define the input impedance, receive and transmit frequency response, hybrid balance, and initial gain values. Microchip provides *AC FXS Profile* examples for over 70 countries including the following:

Table 10-3. Supported AC Source Impedances

Input Impedance	Network Balance Impedance	Countries
150 Ω + (510 Ω // 47 nF)	150 Ω + (510 Ω // 47 nF)	Russia
200 Ω + (680 Ω // 100 nF)	200 Ω + (680 Ω // 100 nF)	China
220 Ω + (820 Ω // 115 nF)	220 Ω + (820 Ω // 115 nF)	Bulgaria, Germany, and South Africa
220 Ω + (820 Ω // 120 nF)	220 Ω + (820 Ω // 120 nF)	Australia

.....continued

Input Impedance	Network Balance Impedance	Countries
270 Ω + (750 Ω // 150 nF)	270 Ω + (750 Ω // 150 nF)	Belgium, Croatia, Denmark, Egypt, Estonia, France, Greece, Hungary, Iceland, Ireland, Israel, Italy, Ivory Coast, Netherlands, Nigeria, Norway, Portugal, Romania, Spain, Sweden, Switzerland, and Turkey
270 Ω + (910 Ω // 120 nF)	270 Ω + (1200 Ω // 120 nF)	Finland
370 Ω + (620 Ω // 310 nF)	370 Ω + (620 Ω // 310 nF)	New Zealand
300 Ω + (1000 Ω // 220 nF)	370 Ω + (620 Ω // 310 nF)	United Kingdom
600 Ω	600 Ω	USA, Argentina, Armenia, Belarus, Canada, Chile, Colombia, Czech Republic, Ecuador, El Salvador, Georgia, Hong Kong, India, Indonesia, Jordan, Korea, Kuwait, Malaysia, Mexico, Pakistan, Paraguay, Peru, Philippines, Poland, Qatar, Saudi Arabia, Singapore, South Korea, Taiwan, Thailand, Ukraine, UAE, Uruguay, and Venezuela.
600 Ω + 1.0 µF	600 Ω + 1.0 µF	Japan and PBX
900 Ω	900 Ω	Brazil
900 Ω + 2.16 µF	800 Ω // (0.05 µF + 100 Ω)	T*elcordia GR-57-CORE* Non-Loaded Loop

Note:

1. The table above provides suggested AC source impedances for the listed countries and are believed to be accurate as of the date of publication of this document. However, standards can and do change from time to time or new ones may be introduced. Some countries may support more than one standard AC source impedance. Customers are responsible for using the appropriate AC FXS Profiles for their applications.
2. VP Profile Wizard makes it easy to add additional countries as long as they are based on the supported impedances.
3. The standard files provided with VP Profile Wizard are for FXS interfaces with two 7-ohm PTC's in series with Tip and Ring. Please contact Microchip Line Circuits Applications if alternate series resistor or PTC resistance values are planned.
4. Narrowband and Wideband versions of these Profiles are available.

The following table lists the *VP-API-II* functions which use values that are defined in the *AC FXS Profile*.

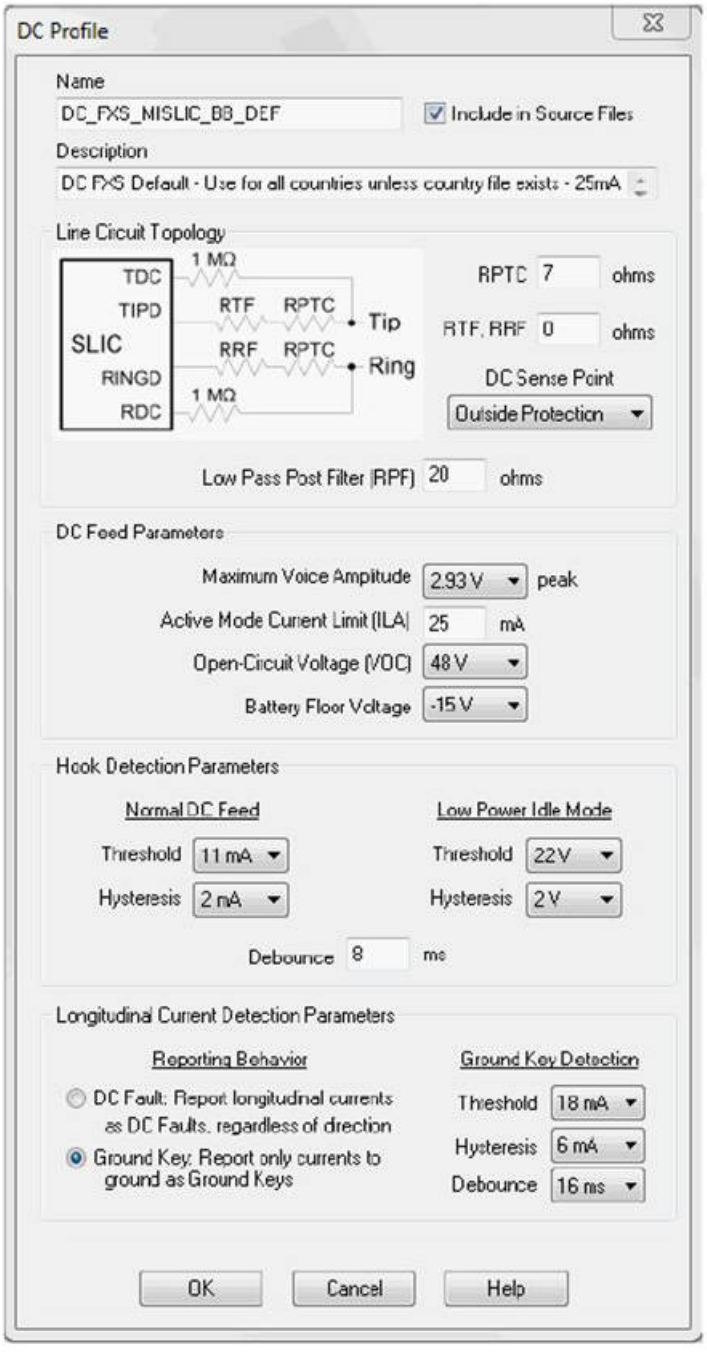
Table 10-4. VP-API-II Functions Using AC FXS Profile

Function Name	Description
`VpInitDevice()`	Resets and initializes device with parameters defined in *Device Profile* and optionally configures all lines on the device with AC, DC, and Ringing parameters.
`VpInitLine()`	Resets and initializes line with AC, DC, and Ringing parameters.
`VpConfigLine()`	Configures line with AC, DC, and Ringing parameters. Similar to `VpInitLine()` but line is not reset. Values not provided in function call result in line retaining previously set parameters.
`VpCalLine()`	This function may need to be called under some circumstances following the functions listed above. Refer to the *VP-API-II Reference Guide* for more details.

10.5 DC Profile

DC Profiles are used to define the feed and loop supervision conditions of the line. An example *DC Profile* is shown in the following figure.

Figure 10-3. Profile Wizard – DC Profile Configuration Example



The following table lists the *VP-API-II* functions which use values that are defined in the *DC Profile*.

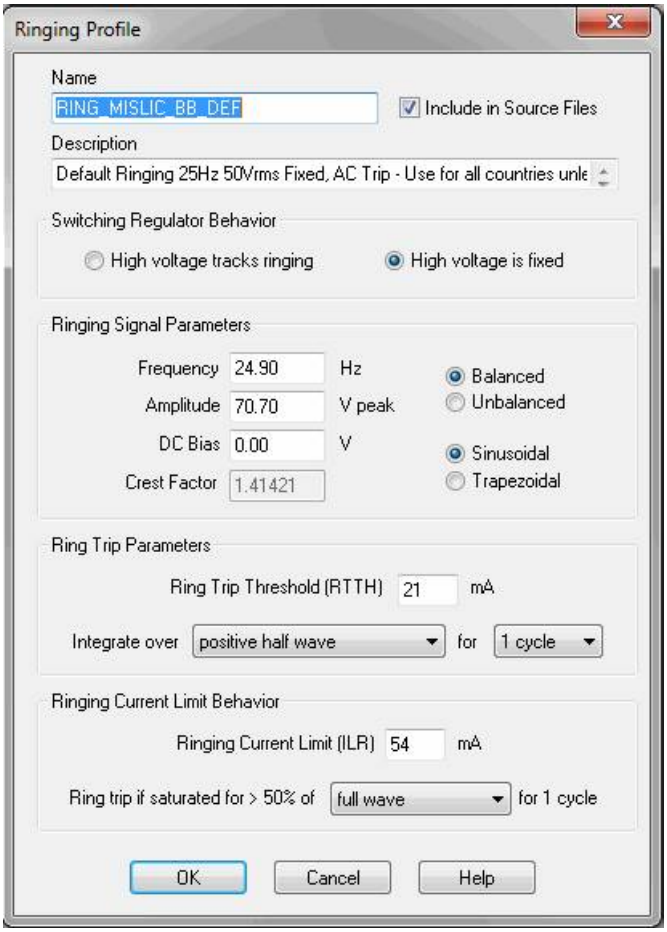
Table 10-5. VP-API-II Functions For DC Feed and Hook Detection Configuration

Function Name	Description
`VpInitDevice()`	Resets and initializes device with parameters defined in *Device Profile* and optionally configures all lines on the device with AC, DC, and Ringing parameters.
`VpInitLine()`	Resets and initializes line with AC, DC, and Ringing parameters.
`VpConfigLine()`	Configures line with AC, DC, and Ringing parameters. Similar to `VpInitLine()` but line is not reset. Values not provided in function call result in line retaining previously set parameters.
`VpCalLine()`	This function may need to be called under some circumstances following the functions listed above. Refer to the *VP-API-II Reference Guide* for more details.

10.6 Ringing Profile

The *Ringing Profile* is used to define the type of ringing, ringing frequency, amplitude, offset, ring trip threshold, and ringing current limit. The *Ringing Profile* for the Le9643 using *VP Profile Wizard* is shown in the following figure.

Figure 10-4. Profile Wizard – Ringing Profile Configuration Example



The following table lists the *VP-API-II* functions which use values that are defined in the *Ringing Profile*.

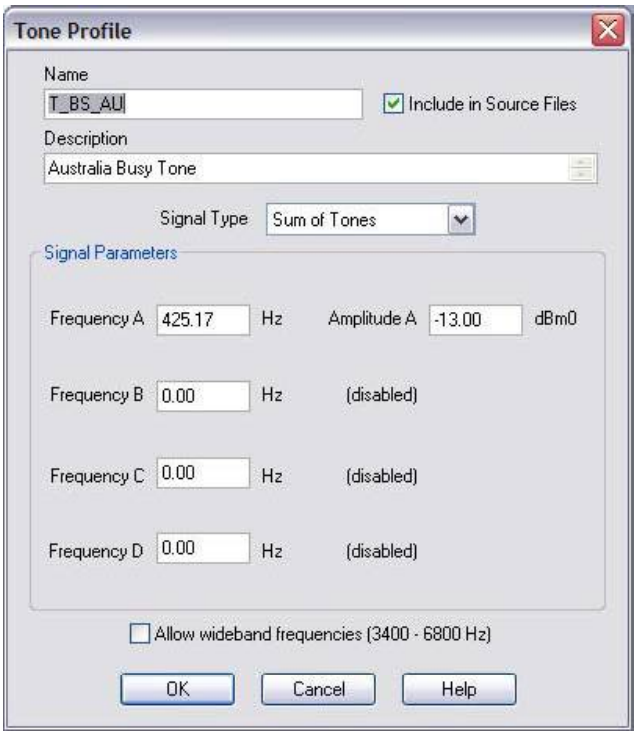
Table 10-6. VP-API-II Functions For Ringing and Ring Trip Definition

Function Name	Description
`VpInitDevice()`	Resets and initializes device with parameters defined in *Device Profile* and optionally configures all lines on the device with AC, DC, and Ringing parameters.
`VpInitLine()`	Resets and initializes line with AC, DC, and Ringing parameters.
`VpConfigLine()`	Configures line with AC, DC, and Ringing parameters. Similar to `VpInitLine()` but line is not reset. Values not provided in function call result in line retaining previously set parameters.
`VpCalLine()`	This function may need to be called under some circumstances following the functions listed above. Refer to the *VP-API-II Reference Guide* for more details.

10.7 Tone Profile

Tone Profiles provide the capability to program up to four simultaneous tones on the line. The *Tone Profile* for the Le9643 using *VP Profile Wizard* is shown in the following figure.

Figure 10-5. Profile Wizard – Tone Profile Configuration



The following table lists the *VP-API-II* function which uses values that are defined in the *Tone Profile*.

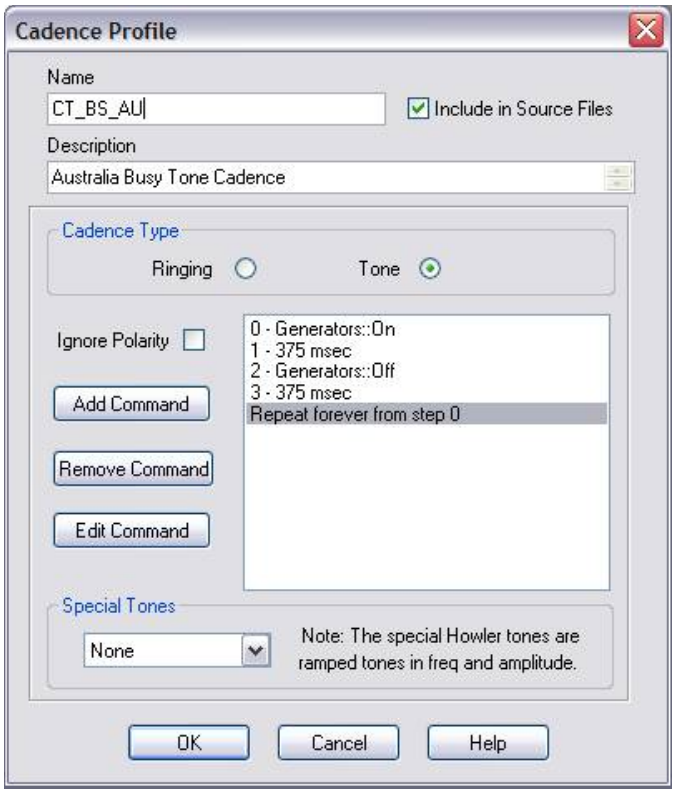
Table 10-7. VP-API-II Function Using Tone Profile

Function Name	Description
`VpSetLineTone()`	Starts a tone on the line. The tone can be cadenced or “always on”.

10.8 Tone Cadence Profile

VP-API-II Tone Cadencing is a highly flexible set of operators the user selects to implement any country-specific ringing or tone cadence requirements including Special Information Tones (SIT) and howler tones. The following figure shows you how to define cadences for call progress tones with *VP Profile Wizard*.

Figure 10-6. Profile Wizard – Tone Cadence Profile Example



The *VP-API-II* Cadencer supports the following operations:

1. Time -- Delays (in a non-blocking fashion) program execution.
2. Generator Control -- Enable/Disable selection on a per-generator basis.
3. Branch -- Forces the cadencing to return to a previous step with "repeat" for *n* number of times. If *n* == 0, repeat forever.
4. Line State -- Sets line to specific *VP-API-II* Line State.

The following table lists the *VP-API-II* function which uses values that are defined in the *Tone Cadence Profile*.

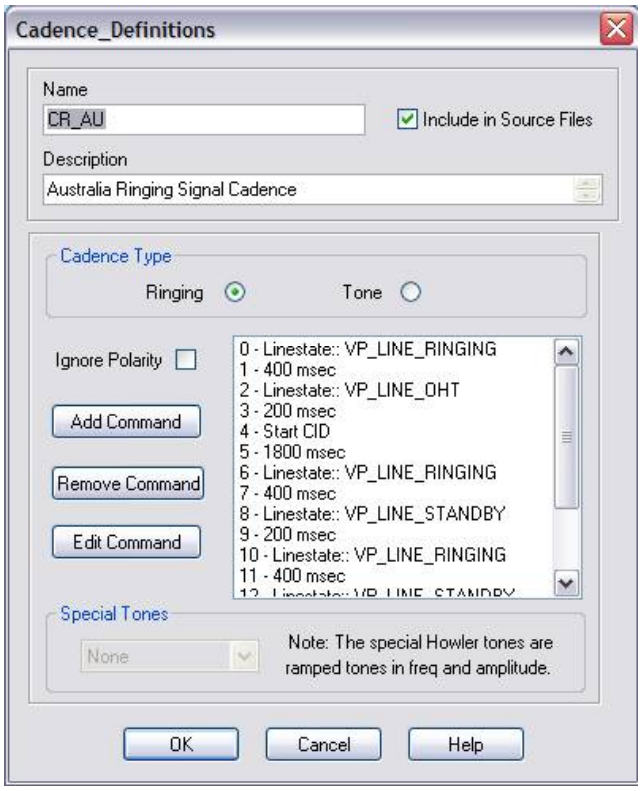
Table 10-8. VP-API-II Function For Tone Cadencing

Function Name	Description
`VpSetLineTone()`	Provides tone cadencing for up to four tones. Also supports country-specific howler tone cadencing (AUS, UK, NTT) with ramp frequency and amplitude.

10.9 Ringing Cadence Profile

VP-API-II ringing cadencing is a flexible set of operators the user selects to implement any country-specific ringing cadence. The following figure shows how to define cadences for ringing generation with *VP Profile Wizard*. Note that events that are associated with Type 1 (on-hook) Caller ID ringing are included by this Profile.

Figure 10-7. Profile Wizard – Ringing Cadence Profile Example



The *VP-API-II* Cadencer supports the following operations:

1. Time -- Delays (in a non-blocking fashion) program execution.
2. Generator Control -- Enable/Disable selection on a per-generator basis.
3. Branch -- Forces the cadencing to return to a previous step with "repeat" for *n* number of times. If *n* == 0, repeat forever.
4. Line State -- Sets line to specific *VP-API-II* line state.
5. Send CID -- Starts Caller ID (CID) on the line while continuing to run cadence. Used for Type 1 Caller ID when CID occurs after first regular ringing cycle in order to achieve a precise delay between the first and second rings.
6. Wait On Caller ID -- Starts Caller ID on the line and suspends currently running cadence. Used for Type 1 Caller ID when CID occurs prior to the first regular ringing cycle.

The following table lists the *VP-API-II* functions which use values that are defined in the *Ringing Cadence Profile*.

Table 10-9. VP-API-II Functions For Ringing Cadencing

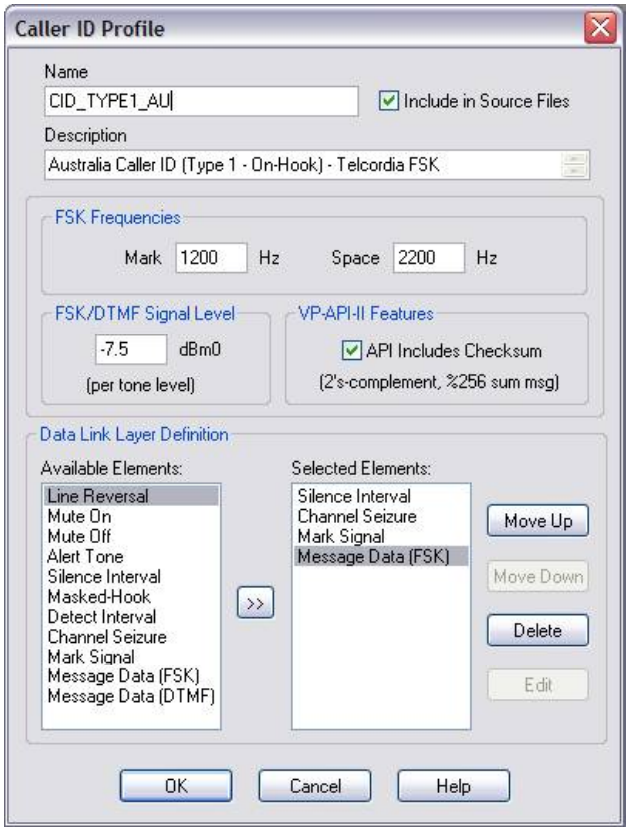
Function Name	Description
`VpSetLineState()`	`VP_LINE_RINGING` and `VP_LINE_RINGING_POLREV` for Ringing Cadence.
`VpInitRing()`	User function to provide Ringing Cadence. Also allows use selection of *Caller ID Profile* associated with ringing.

10.10 Caller ID Profile

The Caller ID block uses Generators C and D to generate phase-continuous 1200 baud FSK tones for on- or off-hook information such as Calling Line ID (or Caller ID) and Visual Message Waiting Indication (VMWI). The duration of each (bit) tone is fixed at 0.833 ms (1200 baud).

Bell 202 tone frequencies are used in the North American and some international markets, and the *ITU-T Recommendation V.23* tone frequencies are used in most of Europe and other international markets. The signal generator amplitude may need to be adjusted depending on the programmed loss plan. Data transmission levels are normally specified as -13.5 dBm +/-1.5 dB.

Figure 10-8. Profile Wizard – Type 1 Caller ID Profile Example



Exact preamble and mark sequences are generated by adjusting the framing mode and sending the appropriate number of characters. The *VP-API-II* abstracts this into a simple driver level interface. *VP Profile Wizard* enables the user to select the Caller ID parameters and build them into the *Caller ID Profile*, which generates the necessary coefficients and instructions for the *VP-API-II*. Note that the signal level in the example below is -7.5 dBm0, which corresponds to a transmitted signal of -13.5 dBm0 to the line due to the 6 dB D/A loss in the default *AC Profile*.

The following table lists the *VP-API-II* functions which use values that are defined in the *Caller ID Profile*.

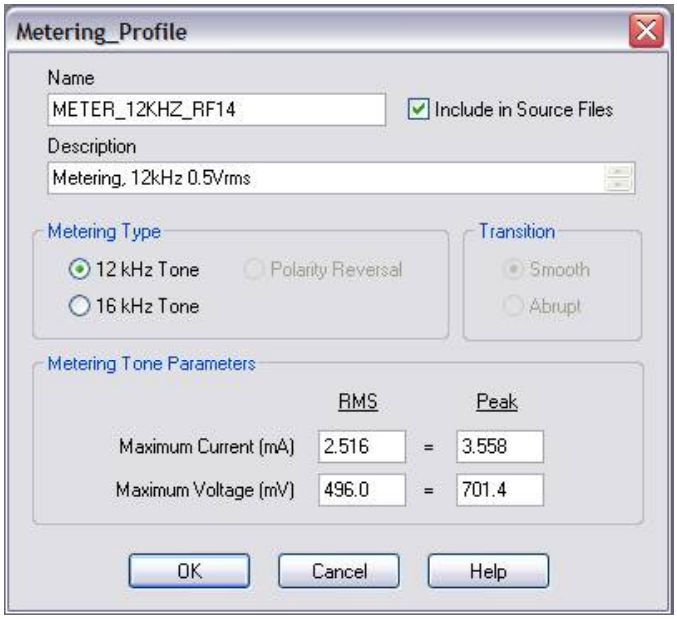
Table 10-10. VP-API-II Functions For Caller ID

Function Name	Description
`VpInitRing()`	User function to provide *Caller ID Profile* associated with ringing.
`VpSendCid()`	Configures and starts Caller ID immediately. Used for Type 2 Caller ID.
`VpInitCid()`	Input for Caller ID Message Data up to 32 bytes.

.....continued	
Function Name	**Description**
`VpContinueCid()`	Input for Caller ID Message Data up to 16 bytes. Called after `VpInitCid()` or `VpSendCid()` when event `VP_LINE_EVID_CID_DATA` is generated.

10.11 Metering Profile

Figure 10-9. Profile Wizard – Metering Profile Example



The *Metering Profile* allows the user to define the pulse metering frequency (12 or 16 kHz), peak current, and voltage limit. The above figure shows you an example of the *Metering Profile* definition in *VP Profile Wizard*.

The following table lists the *VP-API-II* functions which use values that are defined in the *Metering Profile*.

Table 10-11. VP-API-II Functions for Metering

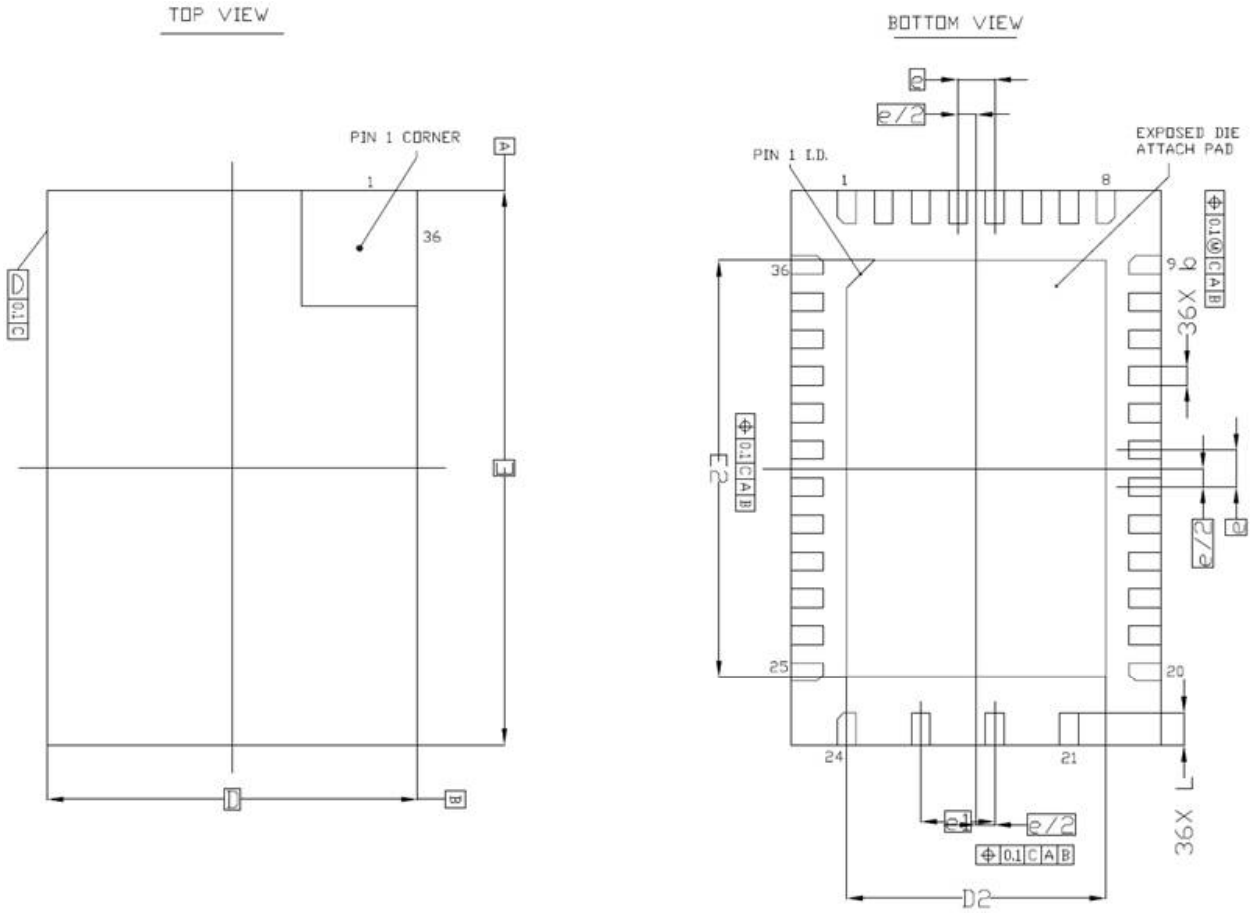
Function Name	Description
`VpInitMeter()`	Configures the metering signal generator of an individual line.
`VpStartMeter()`	Starts metering pulses.

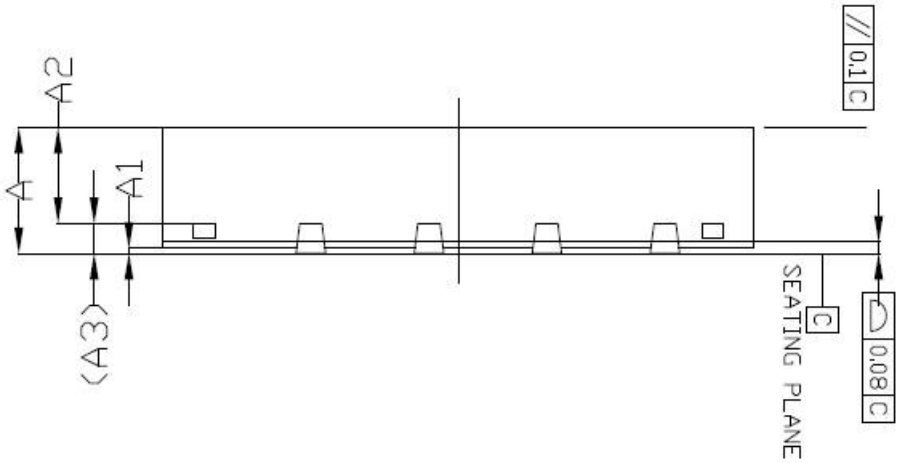
11. Package Outline

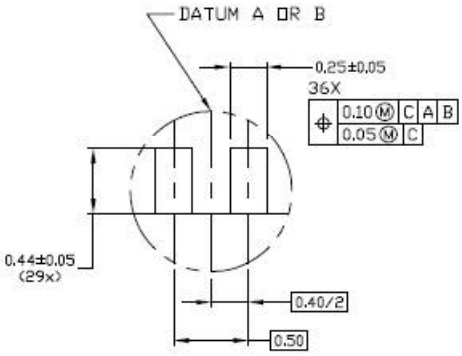
The package outline drawings and the recommended land pattern for the Le9643 are presented in this section.

Note: Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.
All dimensions are in mm.

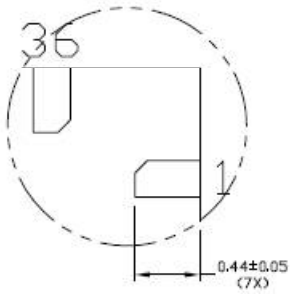
Figure 11-1. Le9643 (36-Pin QFN) Package Drawing







DETAIL A (SCALE 3:1)



CORNER LEADS WITH CHAMFER
DETAIL B (SCALE 3:1)

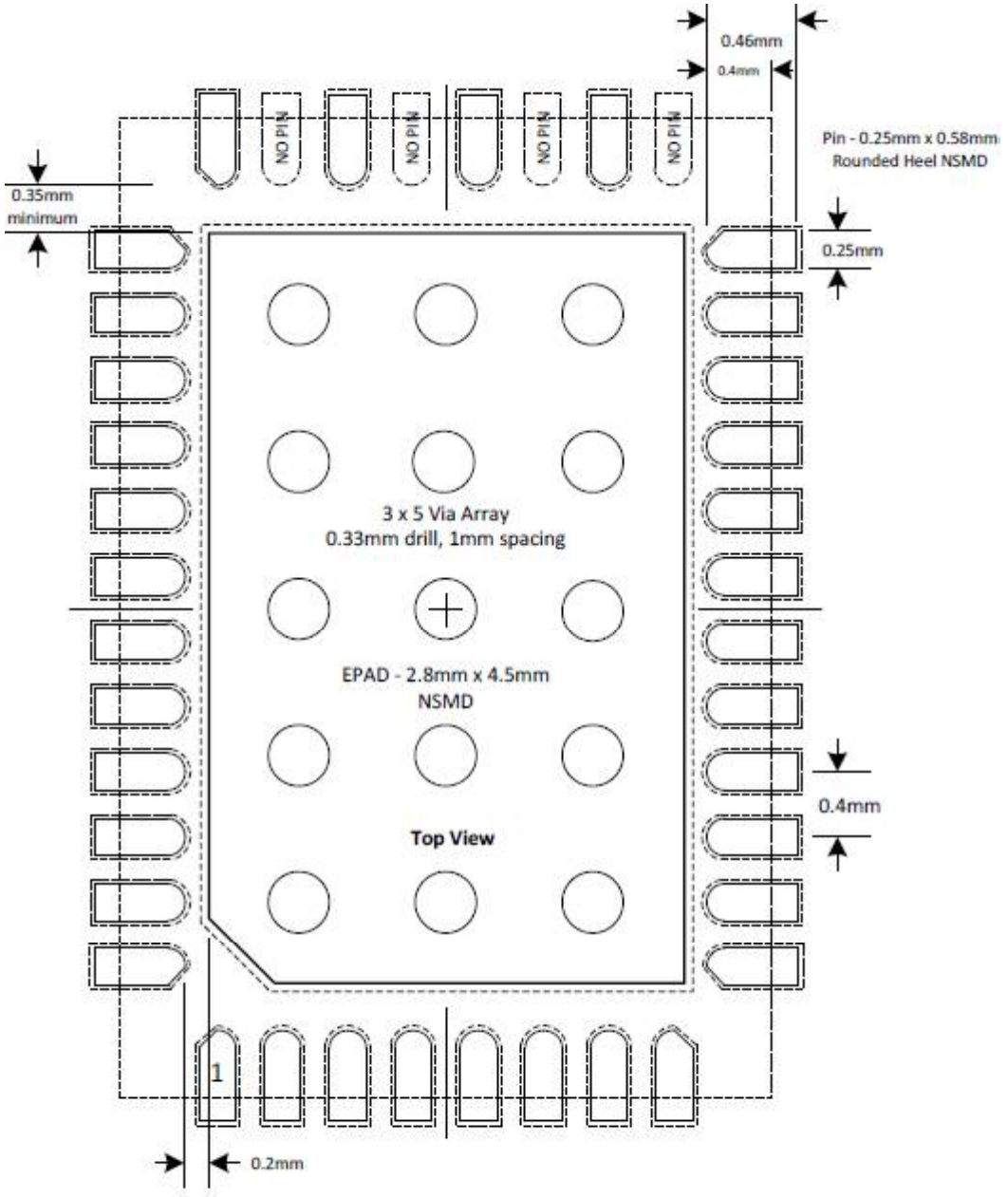
		Mils			mm		
Attribute	Symbol	Min	Nom	Max	Min	Nom	Max
Total Thickness	A	31.5	35.43	39.37	0.8	0.9	1.0
Stand off	A1	0	0.79	1.97	0	0.02	0.05
L/F thickness	A3	7.48	7.87	8.26	0.19	0.2	0.21
Lead Width	b	5.91	7.87	9.84	0.15	0.20	0.25
Body Size X	D	153.54	157.48	161.42	3.9	4.0	4.1
Body Size Y	E	232.28	236.22	240.16	5.9	6.0	6.1
Lead Pitch	e		15.75			0.4	
Lead Pitch	e1		31.5			0.8	
EP Size X	D2	106.30	110.24	114.17	2.7	2.8	2.9
EP Size Y	E2	173.23	177.17	181.10	4.4	4.5	4.6
Lead Length	L	11.81	13.78	15.75	0.300	0.350	0.400
Coplanarity	⌓ 0.08 C			3.15			0.08

NOTES:

1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5–1994
   ALL DIMENSIONS ARE IN MILLIMETERS ° IN DEGREES

2. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP (BOTH ROWS). IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA

Figure 11-2. Recommended Land Pattern (36-Pin QFN) – Top View



Microchip 36QFN
4mm x 6mm, 0.4mm pitch

12. Related Collateral

The following documentation is available on the Microchip website.

12.1 Documentation

- **Le9622 Data Sheet**
- **Le9632 Data Sheet**
- **Le9643 Data Sheet**
- **Le9653 Data Sheet**
- **Le9622/Le9632 Product Brief**
- **Le9643/Le9653 Product Brief**
- **VP-API-II Reference Guide (*included with software download*)**
- **Line Test API (LT-API) User's Guide (*included with software download*)**
- **VeriVoice Professional Data Sheet *(included with software download*)**

12.1.1 Application Notes

- **EMI Radiated Immunity**
- **Two Layer PCB Design**
- **VP-API II Based DTMF Detection**

12.2 Development Hardware

Contact your sales representative for the latest Le9643 reference design hardware.

- **ZLR964321L SM2 Line Module**
  - The *ZLR964321L Line Module* features one Le9643 *miSLIC*™ Line Circuit operating in ZSI mode with a 1 FXS 12 V Buck-Boost battery supply capable of 85-VPK ringing with a 3 REN ringer load. This module plugs into the *SM2* receptacle on the VP-Demo platform.
- **ZLR965324H SM2 Line Module**
  - The *ZLR965324H Line Module* features one *Le9643 miSLIC*™ Line Circuits operating in PCM/SPI mode and one *Le9653 miSLIC*™ Line Circuits operating in PCM/SPI mode. The Le9543 is configured with a 1 FXS Inverting-Boost battery supply that is powered by 12 V and capable of 85-VPK tracking ringing with a 3 REN ringer load. The Le9653 device is configured with a 1 FXS High Voltage Inverting- Boost battery supply that is powered by 12 V and capable of 125-VPK tracking ringing with a 5 REN ringer load. This module plugs into the *SM2* receptacle on the VP-Demo platform.

12.3 Downloads, Firmware and Drivers

- **Le9643 IBIS Model,** available on the Microchip Line Circuits website.

12.4 Development Software

URLs for the following software are available on the Microchip Line Circuits website.

- **Le71SK0002 VoicePath API-II Software**
  - The *VP-API-II* is a set of C source used by the host application to interface to the *VE880*, *VE890*, *ZL880, and miSLIC Series* and other Microchip voice product families. A signed Software License Agreement (SLA) is required.
- **Le71SDKTK Microchip Toolkit**
  - The Microchip Line Circuits Toolkit application is a scripting environment that allows for the development and distribution of Tcl related collateral for Line Circuits hardware and software products. The Toolkit includes several custom Line Circuits Tcl extensions, i.e. VP-Demo.
  - The VP-Demo extension is intended to provide a robust interactive GUI and scripting environment for each of the currently manufactured Microchip Line Circuits products.
- **Le71SDKPRO Profile Wizard**
  - The *VP Profile Wizard* is a *Microsoft Windows* GUI application that aids in the organization and creation of country *Profiles* used in the *VP-API-II* into a single project file.
- **ZL880SLVVP VeriVoice Professional Test Suite**
  - The *VeriVoice™ Professional Test Suite* provides customers with the most cost-effective, reliable VoIP line-testing tools available on the market. The *VeriVoice Test Suite Software* is used in conjunction with *VoicePath™ API-II* software to provide line test and self-test for select devices from the miSLIC™ Series and ZL880 VoicePort™ Series. The *VeriVoice™ Professional Test Suite* software is available in C code, allowing for easy integration and customization by a developer.
- **ZLS880VVMT VeriVoice Manufacturing Test Package**
  - The *VeriVoice™ Manufacturing Test Package* is a stand-alone, self contained test package intended to facilitate factory testing of new products based on Line Circuits' *miSLIC™ Series, ZL880 Series, VE880 Series, and VE890 chipsets*. The software is distributed as a portable, platform- independent C source code module. The software is architected as a rapid set of tests which provide thorough test cover. The software eliminates the need for expensive test equipment.

13. Revision History

Revision Level	Description
A	Converted the legacy document to the Microchip format and updated the following sections: • Package Outline • Related Collateral

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