Product Change Notification / SYST-15LRMT047

Date:

16-Jun-2021

Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ERRATA - ATtiny1624/1626/1627 Silicon Errata and Data Sheet Clarification

Affected CPNs:

SYST-15LRMT047_Affected_CPN_06162021.pdf
SYST-15LRMT047_Affected_CPN_06162021.csv

Notification Text:

SYST-15LRMT047

Microchip has released a new Product Documents for the ATtiny1624/1626/1627 Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at ATtiny1624/1626/1627 Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change:• Device: 2.2.1 IDD Power-Down Current Consumption
• USART: 2.6.2 Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 16 Jun 2021

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

ATtiny1624/1626/1627 Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

ATTINY1624-SSF
ATTINY1624-SSFR
ATTINY1624-SSU
ATTINY1624-SSUR
ATTINY1624-XF
ATTINY1624-XFR
ATTINY1624-XU
ATTINY1624-XUR
ATTINY1626-MF
ATTINY1626-MFR
ATTINY1626-MU
ATTINY1626-MUR
ATTINY1626-SF
ATTINY1626-SFR
ATTINY1626-SU
ATTINY1626-SUR
ATTINY1626-XF
ATTINY1626-XFR
ATTINY1626-XU
ATTINY1626-XUR
ATTINY1627-MF
ATTINY1627-MFR
ATTINY1627-MU
ATTINY1627-MUR

ATtiny1624/1626/1627

Silicon Errata and Data Sheet Clarifications

The ATtiny1624/1626/1627 devices you have received conform functionally to the current device data sheet (www.microchip.com/DS40002234), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the ATtiny1624/1626/1627 devices.

Notes:

- This document summarizes all the silicon errata issues from all revisions of silicon, previous as well as current
- Refer to the Device/Revision ID section in the current device data sheet (www.microchip.com/DS40002234) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

1. Silicon Issue Summary

Legend

- **-** Erratum is not applicable.
- **X** Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision
		Rev. E[1]
Device	2.2.1 IDD Power-Down Current Consumption	X
CCL	2.3.1 The CCL Must be Disabled to Change the Configuration of a Single LUT	X
TCA	2.4.1 Restart Will Reset Counter Direction in NORMAL and FRQ Mode	X
TCB	2.5.1 CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode	X
USART	2.6.1 Open-Drain Mode Does not Work When TXD Is Configured as Output	X
USART	2.6.2 Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode	X

Note:

1. This revision is the initial release of the silicon.

2. Silicon Errata Issues

2.1 Errata Details

-	Erratum is not applicable.
X	Erratum is applicable.

2.2 Device

2.2.1 IDD Power-Down Current Consumption

For material with date code 2045 (manufactured in the year 2020, week 45) or older, the IDD power-down leakage can exceed the targeted maximum value of 2 µA. Note that this maximum value is a target and not documented in the preliminary data sheet.

Work Around
None.

Affected Silicon Revisions

Rev. E
X

2.3 CCL - Configurable Custom Logic

2.3.1 The CCL Must be Disabled to Change the Configuration of a Single LUT

To reconfigure a LUT, the CCL peripheral must be disabled (write ENABLE in CCL.CTRLA to '0'). Writing ENABLE to '0' will disable all the LUTs, and affects the LUTs not under reconfiguration.

Work Around
None

Affected Silicon Revisions

Rev. E
X

2.4 TCA - 16-Bit Timer/Counter Type A

2.4.1 Restart Will Reset Counter Direction in NORMAL and FRQ Mode

When the TCA is configured to a NORMAL or FRQ mode (WGMODE in TCAn.CTRLB is '0x0' or '0x1'), a RESTART command or Restart event will reset the count direction to default. The default is counting upwards.

Work Around
None.

Affected Silicon Revisions

Rev. E
X

2.5 TCB - 16-Bit Timer/Counter Type B

2.5.1 CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode

When the TCB is operating in 8-bit PWM mode (CNTMODE in TCBn.CTRLB is '0x7'), the low and high bytes for the CNT and CCMP registers operate as 16-bit registers for read and write. They cannot be read or written independently.

Work Around

Use 16-bit register access. Refer to the data sheet for further information.

Affected Silicon Revisions

Rev. E
X

2.6 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.6.1 Open-Drain Mode Does not Work When TXD Is Configured as Output

When configured as an output, the USART TXD pin can drive the pin high regardless of whether the Open-Drain mode is enabled or not.

Work Around

Configure the TXD pin as an input by writing the corresponding bit in PORTx.DIR to '0' when using Open-Drain mode.

Affected Silicon Revisions

Rev. E
X

2.6.2 Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode

The Start-of-Frame Detection feature enables the USART to wake up from Standby sleep mode upon data reception. The Start-of-Frame Detector can unintentionally be triggered when the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register is set, and the device is in Active mode. If the Receive Data (RXDATA) registers are read while receiving new data, the Receive Complete Interrupt Flag (RXCIF) in the USARTn.STATUS register is cleared. This results in the Start-of-Frame Detector being triggered and falsely detecting the following falling edge as a start bit. When the Start-of-Frame Detector detects a start condition, the frame reception is restarted, resulting in corrupt received data. Note that the USART Receive Start Interrupt Flag (RXSIF) always is '0' when in Active mode. No interrupt will be triggered.

Work Around

Disable Start-of-Frame Detection by writing '0' to the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register when the device is in Active mode. Re-enable it by writing the bit to '1' before transitioning to Standby sleep mode. This work around depends on a protocol preventing a new incoming frame when re-enabling Start-of-Frame Detection. Re-enabling Start-of-Frame Detection, while a new frame is already incoming, will result in corrupted received data.

Affected Silicon Revisions

Rev. E
X

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (www.microchip.com/DS40002234).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 Fuses - Correct Factory Default Value for Reserved Fuse Bits is '1'

The factory default values for fuses are following the recommendation to write reserved fuse bits to '1', but the default values stated in the data sheet are presenting the reserved fuse bits written to '0'. For this reason, the on-device default values of the following fuses are differing from the values stated in the data sheet:

Fuse	Stated Factory Default in Data Sheet	Actual Factory Default on Device
OSCCFG	0x02	**0x7E**
SYSCFG0	0xD4	**0xF6**
SYSCFG1	0x07	**0xFF**

Note: These changes do not alter the default behavior or configuration of the device.

4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc. Rev.	Date	Comments
C	06/2021	Updated errata: • Device: 2.2.1 IDD Power-Down Current Consumption • USART: 2.6.2 Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode
B	12/2020	• Silicon revision D not released to production. Silicon revision E is the initial release: – Removed silicon revision D from *Silicon Issues Summary* and all *Affected Versions* tables – Removed all errata only applicable to silicon revision D • Added errata: – Device: *IDD Power-Down Current Consumption* – CCL: *The CCL Must be Disabled to Change the Configuration of a Single LUT* – TCA: *Restart Will Reset Counter Direction in NORMAL and FRQ Mode* – TCB: *CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode* – USART: *Open-Drain Mode Does Not Work When TXD is Configured as Output* • Added data sheet clarification: – Fuses: *Correct Factory Default Value for Reserved Fuse Bits is '1'*
A	07/2020	Initial document release

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