Product Change Notification / SYST-21DTWG564

## Date:

24-May-2021

## Product Category:

32-bit Microcontrollers

## PCN Type:

Document Change

## Notification Subject:

ERRATA - PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family Silicon Errata Document Revision

## Affected CPNs:

SYST-21DTWG564_Affected_CPN_05242021.pdf
SYST-21DTWG564_Affected_CPN_05242021.csv

## Notification Text:

SYST-21DTWG564

Microchip has released a new Product Documents for the PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family Silicon Errata of devices. If you are using one of these devices please read the document located at PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family Silicon Errata.

**Notification Status:** Final

**Description of Change:**
1) Terminology for "Master" and "Slave" was updated to "Host" and "Client" respectively. This change may not be reflected in all associated Microchip documentation. For more information, contact a Microchip sales repre[1]sentative.
2) Added a new Data Sheet Clarification for 3. Module:EBI.
3) Added the following new silicon issues:
- 39. Module: (ADC)
- 40. Module: (USB)
- 41. Module: (EBI)
- 42. Module: (DMA)
- 43. Module: (Device)
- 44. Module: (Timer2-9

**Impacts to Data Sheet:** None

**Reason for Change:** To Improve Productivity

**Change Implementation Status:** Complete

**Date Document Changes Effective:** 24 Mar 2021

**NOTE:** Please be advised that this is a change to the document only the product has not been changed.

**Markings to Distinguish Revised from Unrevised Devices:** N/A

## Attachments:

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family Silicon Errata

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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SYST-21DTWG564 - ERRATA - PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family Silicon Errata Document Revision

Affected Catalog Part Numbers(CPN)

PIC32MZ0512EFE124-E/TL
PIC32MZ0512EFF124-E/TL
PIC32MZ0512EFK124-E/TL
PIC32MZ1024EFE124-E/TL
PIC32MZ1024EFF124-E/TL
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PIC32MZ1024EFM100T-E/PF
PIC32MZ2048EFG100T-E/PF
PIC32MZ2048EFH100T-E/PF
PIC32MZ2048EFM100T-E/PF
PIC32MZ0512EFE100T-E/GJX
PIC32MZ0512EFF100T-E/GJX
PIC32MZ0512EFK100T-E/GJX
PIC32MZ1024EFE100T-E/GJX
PIC32MZ1024EFF100T-E/GJX
PIC32MZ1024EFG100T-E/GJX
PIC32MZ1024EFH100T-E/GJX
PIC32MZ1024EFK100T-E/GJX
PIC32MZ1024EFM100T-E/GJX
PIC32MZ2048EFG100T-E/GJX
PIC32MZ2048EFH100T-E/GJX
PIC32MZ2048EFM100T-E/GJX
PIC32MZ0512EFE144T-E/PL
PIC32MZ0512EFF144T-E/PL

PIC32MZ0512EFK144T-E/PL
PIC32MZ1024EFE144T-E/PL
PIC32MZ1024EFF144T-E/PL
PIC32MZ1024EFG144T-E/PL
PIC32MZ1024EFH144T-E/PL
PIC32MZ1024EFK144T-E/PL
PIC32MZ1024EFM144T-E/PL
PIC32MZ2048EFG144T-E/PL
PIC32MZ2048EFH144T-E/PL
PIC32MZ2048EFM144T-E/PL
PIC32MZ0512EFE144T-E/JWX
PIC32MZ0512EFF144T-E/JWX
PIC32MZ0512EFK144T-E/JWX
PIC32MZ1024EFE144T-E/JWX
PIC32MZ1024EFF144T-E/JWX
PIC32MZ1024EFG144T-E/JWX
PIC32MZ1024EFH144T-E/JWX
PIC32MZ1024EFK144T-E/JWX
PIC32MZ1024EFM144T-E/JWX
PIC32MZ2048EFG144T-E/JWX
PIC32MZ2048EFH144T-E/JWX
PIC32MZ2048EFM144T-E/JWX
PIC32MZ0512EFF064T-E/MR021
PIC32MZ0512EFE064T-E/MRA21
PIC32MZ0512EFE064T-E/MR
PIC32MZ0512EFF064T-E/MR
PIC32MZ0512EFK064T-E/MR
PIC32MZ1024EFE064T-E/MR
PIC32MZ1024EFF064T-E/MR
PIC32MZ1024EFG064T-E/MR
PIC32MZ1024EFH064T-E/MR
PIC32MZ1024EFK064T-E/MR
PIC32MZ1024EFM064T-E/MR
PIC32MZ2048EFG064T-E/MR
PIC32MZ2048EFH064T-E/MR
PIC32MZ2048EFM064T-E/MR
PIC32MZ0512EFF064T-E/MRV01
PIC32MZ1024EFG064T-E/MRVAO
PIC32MZ0512EFE144T-E/PH
PIC32MZ0512EFF144T-E/PH
PIC32MZ0512EFK144T-E/PH
PIC32MZ1024EFE144T-E/PH
PIC32MZ1024EFF144T-E/PH
PIC32MZ1024EFG144T-E/PH
PIC32MZ1024EFH144T-E/PH
PIC32MZ1024EFK144T-E/PH
PIC32MZ1024EFM144T-E/PH

PIC32MZ2048EFG144T-E/PH
PIC32MZ2048EFH144T-E/PH
PIC32MZ2048EFM144T-E/PH
PIC32MZ0512EFE064T-E/PT
PIC32MZ0512EFF064T-E/PT
PIC32MZ0512EFK064T-E/PT
PIC32MZ1024EFE064T-E/PT
PIC32MZ1024EFF064T-E/PT
PIC32MZ1024EFG064T-E/PT
PIC32MZ1024EFH064T-E/PT
PIC32MZ1024EFK064T-E/PT
PIC32MZ1024EFM064T-E/PT
PIC32MZ2048EFG064T-E/PT
PIC32MZ2048EFH064T-E/PT
PIC32MZ2048EFM064T-E/PT
PIC32MZ0512EFE100T-E/PT
PIC32MZ0512EFF100T-E/PT
PIC32MZ0512EFK100T-E/PT
PIC32MZ1024EFE100T-E/PT
PIC32MZ1024EFF100T-E/PT
PIC32MZ1024EFG100T-E/PT
PIC32MZ1024EFH100T-E/PT
PIC32MZ1024EFK100T-E/PT
PIC32MZ1024EFM100T-E/PT
PIC32MZ2048EFG100T-E/PT
PIC32MZ2048EFH100T-E/PT
PIC32MZ2048EFM100T-E/PT
PIC32MZ1024EFH100T-E/PTV06
PIC32MZ1024EFH100T-E/PTVAO

# PIC32MZ EF FAMILY

## PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family Silicon Errata and Data Sheet Clarification

The PIC32MZ Embedded Connectivity with Floating Point Unit (EF) family of devices that you have received conform functionally to the current Device Data Sheet (DS60001320G), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC32MZ Embedded Connectivity with Floating Point Unit (EF) family silicon.

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (B2).

Data Sheet clarifications and corrections (if applicable) start on page 16, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® X IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB X IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB X IDE project.
3. Configure the MPLAB X IDE project for the appropriate device and hardware debugger.
4. Select *Window > Dashboard*, and then click the **Refresh Debug Tool Status** icon ( ).
5. The part number and the Device and Revision ID values appear in the **Output** window.

**Note:** If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various PIC32MZ EF Family silicon revisions are shown in Table 1.

**TABLE 1: SILICON DEVREV VALUES**

| Part Number | Device ID(1) | Revision ID for Silicon Revision(1) | | |
|---|---|---|---|---|
| | | A1 | A3 | B2 |
| PIC32MZ0512EFE064 | 0x7201053 | 0x1 | 0x3 | 0x6 |
| PIC32MZ0512EFF064 | 0x7206053 | | | |
| PIC32MZ0512EFK064 | 0x722E053 | | | |
| PIC32MZ1024EFE064 | 0x7202053 | | | |
| PIC32MZ1024EFF064 | 0x7207053 | | | |
| PIC32MZ1024EFK064 | 0x722F053 | | | |
| PIC32MZ1024EFG064 | 0x7203053 | | | |
| PIC32MZ1024EFH064 | 0x7208053 | | | |
| PIC32MZ1024EFM064 | 0x7230053 | | | |
| PIC32MZ2048EFG064 | 0x7204053 | | | |
| PIC32MZ2048EFH064 | 0x7209053 | | | |
| PIC32MZ2048EFM064 | 0x7231053 | | | |

**Note 1:** Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS60001320G) for detailed information on Device and Revision IDs for your specific device.

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**TABLE 1: SILICON DEVREV VALUES (CONTINUED)**

| Part Number | Device ID(1) | Revision ID for Silicon Revision(1) | | |
|---|---|---|---|---|
| | | A1 | A3 | B2 |
| PIC32MZ0512EFE100 | 0x720B053 | 0x1 | 0x3 | 0x6 |
| PIC32MZ0512EFF100 | 0x7210053 | | | |
| PIC32MZ0512EFK100 | 0x7238053 | | | |
| PIC32MZ1024EFE100 | 0x720C053 | | | |
| PIC32MZ1024EFF100 | 0x7211053 | | | |
| PIC32MZ1024EFK100 | 0x7239053 | | | |
| PIC32MZ1024EFG100 | 0x720D053 | | | |
| PIC32MZ1024EFH100 | 0x7212053 | | | |
| PIC32MZ1024EFM100 | 0x723A053 | | | |
| PIC32MZ2048EFG100 | 0x720E053 | | | |
| PIC32MZ2048EFH100 | 0x7213053 | | | |
| PIC32MZ2048EFM100 | 0x723B053 | | | |
| PIC32MZ0512EFE124 | 0x7215053 | 0x1 | 0x3 | 0x6 |
| PIC32MZ0512EFF124 | 0x721A053 | | | |
| PIC32MZ0512EFK124 | 0x7242053 | | | |
| PIC32MZ1024EFE124 | 0x7216053 | | | |
| PIC32MZ1024EFF124 | 0x721B053 | | | |
| PIC32MZ1024EFK124 | 0x7243053 | | | |
| PIC32MZ1024EFG124 | 0x7217053 | | | |
| PIC32MZ1024EFH124 | 0x721C053 | | | |
| PIC32MZ1024EFM124 | 0x7244053 | | | |
| PIC32MZ2048EFG124 | 0x7218053 | | | |
| PIC32MZ2048EFH124 | 0x721D053 | | | |
| PIC32MZ2048EFM124 | 0x7245053 | | | |
| PIC32MZ0512EFE144 | 0x721F053 | 0x1 | 0x3 | 0x6 |
| PIC32MZ0512EFF144 | 0x7224053 | | | |
| PIC32MZ0512EFK144 | 0x724C053 | | | |
| PIC32MZ1024EFE144 | 0x7220053 | | | |
| PIC32MZ1024EFF144 | 0x7225053 | | | |
| PIC32MZ1024EFK144 | 0x724D053 | | | |
| PIC32MZ1024EFG144 | 0x7221053 | | | |
| PIC32MZ1024EFH144 | 0x7226053 | | | |
| PIC32MZ1024EFM144 | 0x724E053 | | | |
| PIC32MZ2048EFG144 | 0x7222053 | | | |
| PIC32MZ2048EFH144 | 0x7227053 | | | |
| PIC32MZ2048EFM144 | 0x724F053 | | | |

**Note 1:** Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS60001320G) for detailed information on Device and Revision IDs for your specific device.


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**TABLE 2: SILICON ISSUE SUMMARY**

| Module | Feature | Issue | Issue Summary | Affected Revisions(1) | | |
|---|---|---|---|---|---|---|
| | | | | A1 | A3 | B2 |
| Oscillator | Reference Clock | 1. | The Reference Clock cannot divide input frequencies greater than 100 MHz. | X | X | X |
| Oscillator | Primary Oscillator Crystal | 2. | **Revision A1 Silicon:** A crystal oscillator cannot be used as an input to the Primary Oscillator (OSC1/OSC2 pins).<br>**Revision A3 and B2 Silicon:** The Primary Oscillator has been tested in a normal power-up sequence and supports specific crystal operation. | X | X | X |
| Oscillator | FRC Tuning | 3. | The OSCTUN register only increases the frequency of the FRC. | X | | |
| Secondary Oscillator | Crystal Use | 4. | The Secondary Oscillator (SOSC) does not support crystal operation. | X | X | |
| Power-Saving | PMD bits | 5. | Turning off REFCLK through the PMD bits causes unpredictable device behavior. | X | X | |
| $I^2C$ | — | 6. | The $I^2C$ module does not function reliably under certain conditions. | X | X | |
| UART | Auto-baud | 7. | The Auto-baud feature does not function to set the baud rate. | X | X | X |
| UART | Synchronization | 8. | On a RX FIFO overflow, shift registers stop receiving data, which causes the UART to lose synchronization. | X | X | X |
| USB | Suspend Mode | 9. | The USB module will not function if the device enters Sleep mode and the USB PHY is turned off by setting the USBSSEN bit in the CFGCON register to '1'. | X | X | X |
| Power-Saving Modes | Sleep Mode | 10. | The device may not exit Sleep mode. | X | X | |
| ADC | Digital Filters | 11. | Using multiple digital filters may result in data not being captured accurately. | X | X | |
| ADC | Level Trigger | 12. | The ADC level trigger will not perform burst conversions in Debug mode. | X | X | |
| ADC | DNL | 13. | In Differential mode, DNL for code 3072 is out of specification. | X | X | X |
| ADC | Low-voltage Operation | 14. | When the operating voltage (VDD/AVDD) is below 2.5V (i.e., charge pumps are ON), only one ADC core can be used. | X | X | X |
| ADC | Turbo Mode | 15. | Turbo mode is not functional. | X | X | X |
| USB | Resume | 16. | The USB module does not support remote wake-up. | X | X | X |
| Oscillator | External Clock Mode | 17. | The EC mode timing specifications for the Primary Oscillator (POSC) are not met. | X | | |
| Temperature Sensor | — | 18. | The Temperature Sensor does not function. | X | X | X |
| ICSP | TDO | 19. | The TDO pin becomes an output and toggles while programming on any ICSP™ PGECx/PGEDx pair. | X | X | X |
| DMA | PMD bits | 20. | Setting the PMD bit for DMA (PMD7<4>) does not disable clocks or the DMA peripheral. | X | X | X |
| PMP | Status Bits | 21. | The PMP input buffer full flag, IB0F, and the output buffer underflow, OBUF, are set as soon as the PMP is turned on in Client mode (when TTLEN = 1). | X | X | X |

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.

**TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)**

| Module | Feature | Issue | Issue Summary | Affected Revisions(1) | | |
|---|---|---|---|---|---|---|
| | | | | A1 | A3 | B2 |
| Sleep | IPD | 22. | A 3 mA increase occurs during Sleep mode when PB5DIV is disabled. | X | X | X |
| SQI | RX/TX FIFO | 23. | The SQI may continuously receive invalid data or fail to transmit when the SQICLKDIV is used. | X | X | X |
| POR | GPIO | 24. | Whenever VDD is less than1.75V, the I/O pin states may be indeterminate. | X | X | |
| Crypto | Partial Packet | 25. | The cryptographic DMA module does not support partial packet processing. | X | X | X |
| Crypto | Zero Length Packet | 26. | Zero length packets fail to process. The crypto DMA does not support an empty string hash. | X | X | X |
| SPI | Block Transmission | 27. | At the end of a transmission, the SRMT bit can indicate the completion of the transmission for one PBCLK even though the transmission has one block remaining. | X | X | X |
| SQI | Special Function Registers | 28. | The CPU stalls if the SQI Special Function Registers are read before the REFCLKO2 clock is enabled after a Reset. | X | X | X |
| Sleep | Wake-ups | 29. | Multiple sleep attempts which occur before the CPU has fully awakened, may stall the CPU until the next reset event. | X | X | X |
| Security | System Bus Access | 30. | The note at the end of the CFGPG register (Register no. 34-10) indicates that the CPU as system bus initiator is controlled within the CPU core is incorrect. The CPU core internal state will not control the CPU system bus initiator permission group. | X | X | |
| UART | High Speed Mode | 31. | The UART Stop bit duration is shorter than expected in High-Speed mode (UxMODE.BRGH =1) for baud rates less than 7.5 Mbps. | X | X | X |
| Reset | NMI Number | 32. | The NMICNT bit field in the RNMICON register is 8 bits instead of 16 bits. | X | X | |
| I2C3 | I2C3 | 33. | $I^2C3$ on the A3 revision is non functional. | | X | |
| USB | Host Disconnect Detection | 34. | The USB Host module does not wake up CPU from sleep when a USB device is disconnected. | X | X | X |
| USB | LPM | 35. | The USB Link Power Management (LPM) feature is not functional. | X | X | X |
| USB | Host Resume | 36. | The USB Host module does not send correct resume signal on the USB bus on subsequent suspend/resume sequences. | X | X | X |
| I2C | Speed | 37. | The $I^2C$ module does not meet low period of the SCL clock (tLOW) parameter from $I^2C$ specification for clock frequency >= 400 kHz. | X | X | X |
| System Bus | Speed | 38. | When SYSCLK >184 MHz and Flash Wait states = 2, device operation does not conform to published PROGRAM FLASH MEMORY WAIT STATES specification. | | | X |

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.


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**TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)**

| Module | Feature | Issue | Issue Summary | Affected Revisions(1) | | |
|---|---|---|---|---|---|---|
| | | | | A1 | A3 | B2 |
| ADC | External VREF | 39. | Excessive current flows through the VREF- pin when external voltage reference is used, and voltage on the VREF- pin is greater than AVss. | X | X | X |
| USB | FIFO | 40. | Writing '1' to the FLUSH bit (USBIENCSRx<19>, where x =1-7) does not flush the TX FIFO and reset the TX FIFO pointer. | X | X | X |
| EBI | FBIRDYx pin as GPIO | 41. | EBIRDYEN1 bit (CFGEBIC<25>), EBIRDYEN2 bit (CFGEBIC<26>), EBIRDYEN3 bit (CFGEBIC<27>) are not functional and always set to '1'. | X | | X |
| DMA | Channel Destination Half Full Interrupt | 42. | DMA Channel Destination Half Full interrupt can trigger twice. | X | X | X |
| Device | Peripheral Bus x Clock Divisor Control | 43. | Cannot wake-up from sleep by pin change interrupt. | X | X | X |
| Timer2-9 | Match | 44. | If timer match coincides with entry into sleep mode, timer event triggers and interrupt may not occur. | X | X | X |

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.

## Silicon Errata Issues

| | |
|---|---|
| **Note:** | This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**B2**). |

### 1. Module: Oscillator

The Reference Module cannot divide input frequencies greater than 100 MHz. Therefore, SYSCLK cannot be divided if the SYSCLK operates at frequencies greater than 100 MHz.

**Work around**

Instead of using SYSCLK, use PBCLK1 as the input, which is limited to 100 MHz and is synchronized to SYSCLK.

Alternatively, do not divide the SYSCLK and allow the destination peripheral (i.e., SQI, SPI) to divide it as needed. To do this, set the RODIV<14:0> bits and the ROTRIM<8:0> bits to '0'.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2. Module: Oscillator

**Revision A1 Silicon:** A crystal oscillator cannot be used as an input to the Primary Oscillator (POSC) pins OSC1 and OSC2.

**Silicon Work around**

Use an external clock or the Internal FRC Oscillator.

**Revision A3 and B2 Silicon:** The POSC has been tested in a normal power-up sequence and supports specific crystal operation.

**Silicon Work around 1**

The Primary Oscillator (POSC) has been characterized to operate at 8 MHz, 12 MHz, and 24 MHz when the circuit in Figure 1 is implemented, and the operating conditions listed in Table 3 are met.

**FIGURE 1: POSC CRYSTAL CIRCUIT**

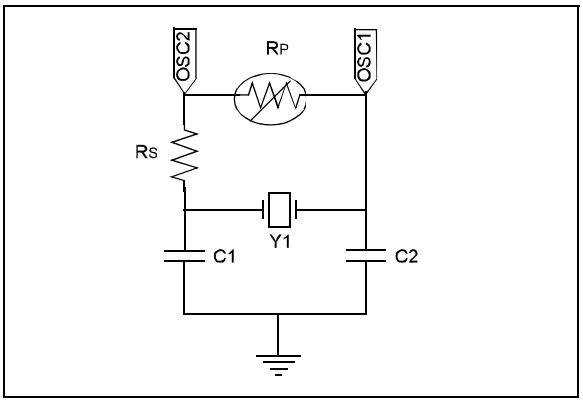


**TABLE 3: CRYSTAL SPECIFICATIONS**

| Crystal Frequency (see Note 1) | Series Resistor (Rs) | POSC Gain Setting POSCGAIN<1:0> (DEVCFG0<20:19>) | POSC Boost Setting POSCBOOST (DEVCFG0<21>) |
|---|---|---|---|
| 8 MHz | 2 kΩ | '0b00 (GAIN_0) | '0b1 (ON) |
| 12 MHz | 1 kΩ | '0b00 (GAIN_0) | '0b1 (ON) |
| 24 MHz | 0 kΩ | '0b00 (GAIN_0)) | '0b1 (ON) |

Note 1: Using any other crystal frequency will require special component selection and characterization.
2: A parallel resistor (RP) should not be used to increase the gain of the POSC.

**Silicon Work around 2**

Alternatively, use an external clock or the Internal FRC oscillator.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 3. Module: Oscillator

The OSCTUN register only increases the frequency of the FRC, which results in the TUN<5:0> bits (OSCTUN<5:0>) functioning as follows:

**TUN<5:0>:** FRC Oscillator Tuning bits

111111 = Center frequency +4%


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111110 =

.
.
.

000001 =

000000 = Center frequency; Oscillator runs at nominal frequency (8 MHz)

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## 4. Module: Secondary Oscillator

A crystal oscillator cannot be used as the input to the Secondary Oscillator (Sosc) pins SOSCI and SOSCO.

**Silicon Work around**

Use an external clock source (32,768 Hz) applied to the SOSCO pin with the FSOSCEN bit (DEVCFG1<6>) set to '0' (i.e., the Sosc is disabled through the Configuration Word) for a real-time clock base; otherwise, use the internal LPRC for non-precision requirements.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

## 5. Module: Power-Saving

Turning off the REFCLK modules through the PMD bits causes unpredictable behavior.

**Work around**

None. Do not disable the REFCLK modules through the PMD bits.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

## 6. Module: I²C

Indeterminate I²C module behavior may result when data rates > 100 kHz and/or continuous sequential data transfers > 500 bytes are used.

The potential false intermittent error signals can result in one of the following error conditions, which are listed in order of decreasing frequency:

- **False Error Condition 1:**
  False Host Bus Collision Detect (Host-mode only) – The error is indicated through the BCL bit (I2CxSTAT<10>).
- **False Error Condition 2:**
  Receive Overflow (Host or Client modes) – The error is indicated through the I2COV bit (I2CxSTAT<20>).
- **False Error Condition 3:**
  Suspended I²C Module Operations (Host or Client modes) – I²C transactions in progress are inadvertently suspended without error indications.

| **Note:** | All three false error conditions are recoverable in software. |
|---|---|

**Revision A1 Silicon Work around 1**

**False Error Condition 1:**

Clear the Host Bus Collision Detect (BCL bit (I2CxSTAT<10>), after the bus returns to an Idle state. The software can monitor the S bit (I2CxSTAT<3>) and the P bit (I2CxSTAT<4>) to wait for an Idle bus. When the software services the bus collision Interrupt Service Routine and the I²C bus is free, the software can resume communication by asserting a new Start condition.

**False Error Condition 2:**

Clear the Receive Overflow Status flag I2COV bit (I2CxSTAT<20>), and then resume normal operation.

**False Error Condition 3:**

First, initialize a Timer to slightly greater than the worst case I²C transaction cycle, (i.e., from Start-to-Stop, including the sum of all other application PC flow latencies, calls, interrupts, etc.). Exact timing is not required, rather just long enough so that a normal transaction is not interrupted. Prior to the beginning of each transaction, start the timer. Be sure to stop and reset the timer after completion of each successful I²C transaction.

Then, during the Timer interrupt (meaning the I²C transaction has timed out), disable the I²C module by setting the ON bit (I2CxCON<15>) = `0`. After disabling the module, wait 4 instruction cycles, after which time the I2CxSTAT register will automatically be cleared. Then, re-enable the I²C module by setting the ON bit = `1` and resume normal operation.

**Revision A1 Silicon Work around 2**

Instead of using the hardware I²C module, use a software “bit-bang” implementation.

**Revision A3 Silicon Work around**

The work arounds described for revision A1 silicon will also work for silicon revision A3, with the exception of I2C3, as I2C3 must use a software “bit-bang” implementation.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |


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## 7. Module: UART

The UART automatic baud rate feature is intended to set the baud rate during run-time based on external data input. However, this feature does not function.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 8. Module: UART

During a RX FIFO overflow condition, the shift register stops receiving data. This causes the UART to lose synchronization with the serial data stream. The only way to recover from this is to turn the UART OFF and ON until it synchronizes. This could require several OFF/ON sequences.

**Work arounds**

**Work around 1:**

Avoid the RX overrun condition by ensuring that the UARTx module has a high enough interrupt priority such that other peripheral interrupt processing latencies do not exceed the time to overrun the UART RX buffer based on the application baud rate. Alternately or in addition to, set the URXISEL bits in the UxSTA register to generate an earlier RX interrupt based on RX FIFO fill status to buy more time for interrupt latency processing requirements.

**Work around 2:**

If avoiding RX FIFO overruns is not possible, implement an ACK/NAK software handshake protocol to repeat lost packet transfers after restoring the UART synchronization.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 9. Module: USB

The USB module will not function if the device enters Sleep mode and the USB PHY is turned off by setting the USBSSEN bit in the CFGCON register to '1'.

**Work around**

Keep the USB PHY operational in Sleep mode by setting the USBSSEN bit to '0'.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 10. Module: Power-Saving Modes

The device may not exit Sleep mode when Flash is powered down through the FSLEEP bit in the DEVCFG0/ADEVCFG0 Configuration register.

**Work around**

Enable Flash in Sleep mode by clearing the Flash Sleep Mode Configuration bit, FSLEEP, in the DEVCFG0/ADEVCFG0 Configuration register.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

## 11. Module: ADC

When using multiple digital filters, the filters may not capture data correctly when the assigned data sources are ready at the same time.

**Work around**

Only one digital filter may be used at a time.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

## 12. Module: ADC

The ADC level trigger will not perform burst conversions in Debug mode.

**Work around**

Do not use Debug mode with the ADC level trigger.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

## 13. Module: ADC

In Differential mode, code 3072 has a DNL of +3.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

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## 14. Module: ADC

When the operating voltage (VDD/AVDD) is below 2.5V (i.e., charge pumps are ON), only one ADC core can be used.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 15. Module: ADC

Turbo mode is not functional when two channels are linked for the purpose of increasing throughput.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 16. Module: USB

The USB module does not support remote wakeup through the USBRIE bit (USBCRCON<1>).

**Work around**

None.

USB descriptors must inform the host that the device does not support remote wake-up.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 17. Module: Oscillator

The Primary Oscillator in EC mode only functions up to 24 MHz

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## 18. Module: Temperature Sensor

The temperature sensor does not function.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 19. Module: ICSP

Regardless of other functions shared on the TDO pin, the TDO function becomes an active output and toggles while programming on any ICSP PGECx/PGEDx pair.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | x | | | | | |

## 20. Module: DMA

Setting the PMD bit for DMA (PMD7<4>) does not disable clocks or the DMA peripheral.

**Work around**

None.

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 21. Module: PMP

The PMP input buffer full flag, IB0F, and the output buffer underflow, OBUF, are set as soon as the PMP is turned on in Client mode (when TTLEN = 1).

**Work around**

After PMP initial initialization is complete, and before the PMP and interrupts are enabled, clear the TTLEN bits in user software.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |


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## 22. Module: Sleep

If the ON bit (PB5DIV<15>) = 0 and PBCLK5 is disabled, a 3mA increase in Sleep IPD current occurs.

**Work around**

Do not disable PBCLK5 before entering Sleep mode.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 23. Module: SQI

When the SQI clock divider is used (by setting CLKDIV ≠ 0), any one of the following error conditions may occur on some of the devices, which are depending on the DDRMODE setting:

- With DDRMODE = 0, the SQI fails in reception only.
- With DDRMODE = 1, the SQI may fail in both reception and transmission.

**Work around**

Set the CLKDIV bits to '0' and use the REFCLK02 as the SQI base clock.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 24. Module: POR

Whenever VDD is less than 1.75V, the I/O pin state and logic level may be indeterminate.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

## 25. Module: Crypto

Attempting to run part of a cryptographic packet through the peripheral may not result in a usable initial vector for continuing the cryptographic operation.

**Work around**

Do not interrupt a cryptographic operation with another, instead, always process a hash completely.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 26. Module: Crypto

Using the crypto DMA on an empty hash string will cause the peripheral to time out and not return a valid hash.

**Work around**

Use the fixed known hash of the empty string.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 27. Module: SPI

Just before the last block of a transmission is shifted out to the SPI pins, the SRMT bit may incorrectly indicate that the transmission is done. However, this does not affect the Transmit Buffer Empty Interrupt (STXISEL = 0).

**Work around**

Use the interrupt notification rather than polling the SRMT bit to determine when a transmission has completed.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

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## 28. Module: SQI

Read access to SQI SFRs stalls the CPU when REFCLKO2 is disabled.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 29. Module: Sleep

Multiple sleep attempts (WAIT instruction with OSCCON<4>=1) which occur within 20 µs of a wake event, before the CPU has fully awakened, can cause the CPU to stall until a Power-on Reset (POR) event.

**Work around**

Ensure that at least 20 µs elapse before attempting to put the CPU to sleep (WAIT instruction with OSCCON<4>=1) after it awakens from a previous sleep.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 30. Module: Security

The note at the end of the CFGPG register (Register no. 34-10) indicates that the CPU as a system bus initiator is controlled within the CPU core is incorrect. The CPU core internal state will not control the CPU system bus initiator permission group.

**Work around**

Use the CFGPG register reserved bits <1:0> to control the permission group ID of the CPU as a system bus initiator.

11 = Initiator is assigned to permission group 3

10 = Initiator is assigned to permission group 2

01 = Initiator is assigned to permission group 1

00 = Initiator is assigned to permission group 0

Also, the reserved bits <:14:12> of the DEVCFG0 and ADEVCFG0 registers can be used to control the permission group ID of the CPU in Debug mode, as in:

- 1xx = Allow CPU access to permission group 2 permission regions
- x1x = Allow CPU access to permission group 1 permission regions
- xx1 = Allow CPU access to permission group 0 permission regions
- 0xx = Deny CPU access to permission group 2 permission regions
- x0x = Deny CPU access to permission group 1 permission regions
- xx0 = Deny CPU access to permission group 0 permission regions

When the CPU is in Debug mode and CFGPG<1:0> are set to a denied permission group as defined by the DEVCFG0<14:12>, the transaction request is assigned Group 3 permissions.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

## 31. Module: UART

The UART TX Stop bit duration is shorter than the expected in High-Speed mode (BRGH (UxMODE<3>) = 1) for baud rates less than 7.5 Mbps.

**Work around**

For baud rates less than 7.5 Mbps, operate the UART in Standard-Speed mode, that is, BRGH (UxMODE<3>) =0. For baud rates greater than 7.5 Mbps operate the UART in High-Speed mode, that is, BRGH (UxMODE<3>) =1.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |


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## 32. Module: Reset

The NMICNT bit field in the RNMICON register is 8 bits instead of 16 bits. It has limited to values 0 through 255.

**Work around**

The user must update the NMICNT register immediately upon entry into NMI ISR in their code with an 8-bit value not to exceed 0xFF. If the user needs to extend the NMI reset event >257 clock counts, the NMICNT register can be updated many times as required inside the NMI to ensure users NMI routine can complete before the pending reset.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

## 33. Module: I2C3

I2C3 on the A3 revision is non functional.

**Work around**

Silicon revision A3 I2C3 must use a software “bit-bang” implementation.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| | X | | | | | | |

## 34. Module: USB

The USB Host module does not wake up CPU from sleep when a USB device is disconnected.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 35. Module: USB

The USB Link Power Management (LPM) feature is not functional.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 36. Module: USB

The USB Host module will send a correct resume signal on the first suspend or sleep sequence, but not on subsequent suspend or sleep sequences.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 37. Module: $I^2C$

The $I^2C$ host module does not meet low period of the SCL clock (tLOW) parameter from $I^2C$ specification for clock frequency >= 400 kHz.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 38. Module: System Bus

Device operation does not conform to published PROGRAM FLASH MEMORY WAIT STATES specification of the following:

| Required Flash Wait States | SYSCLK | Units |
|---|---|---|
| **With ECC:**<br>2 Wait states | 120 < SYSCLK ≤ 200 | MHz |
| **Without ECC:**<br>2 Wait states | 140 < SYSCLK ≤ 200 | MHz |

This may result in undetermined device operation.

**Work around**

Configure the device to the following specification:

| Required Flash Wait States | SYSCLK | Units |
|---|---|---|
| **With ECC:**<br>2 Wait states<br>3 Wait states | 120 < SYSCLK ≤ 184<br>184 < SYSCLK ≤ 200 | MHz |
| **Without ECC:**<br>2 Wait states<br>3 Wait states | 140 < SYSCLK ≤ 184<br>184 < SYSCLK ≤ 200 | MHz |

Increasing Flash wait states in the user application from 2 to 3 will impact the CPU performance by <2% if the cache is enabled.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| | | X | | | | | |

## 39. Module: ADC

Excessive current flows through the VREF- pin when the external voltage reference is used, and the voltage on the VREF- pin is greater than AVss.

**Work around**

Connect the VREF- pin to AVss. Input dynamic range can be changed after varying voltage on the VREF+ pin.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 40. Module: USB

Writing '1' to the FLUSH bit (USBIENCSRx <19>, where x = 1-7) does not flush the TX FIFO and reset the TX FIFO pointer. As a result, the TXPKTRDY bit (USBIENCSRx <16>, where x =1-7) is not cleared and the USB interrupt is not generated.

**Work around**

To clear the TX FIFO, simultaneously set the FLUSH bit (USBIENCSRx <19>, where x = 1-7) and clear the TXPKTRDY bit (USBIENCSRx <16>, where x = 1-7). This sequence must be repeated twice to flush the FIFO.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 41. Module: EBI

The EBIRDYEN1 bit (CFGEBIC <25>), EBIRDYEN2 bit (CFGEBIC <26>), EBIRDYEN3 bit (CFGEBIC <27>) are not functional and always set to '1'.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | | X | | | | | |

## 42. Module: DMA

If the DMA Channel Destination Half Full Interrupt Enable bit is set (DCHxINT.CHDIE = 1), the Channel Destination Half Full Interrupt Flag (DCHxINT.CHDHIF) bit can trigger twice. When the DCHxINT.CHDHIF bit triggers at n/2 byte and is cleared immediately by software, the DCHxINT.CHDHIF bit can trigger at ((n/2) + 1) byte also.

**Work around**

Clear the DCHxINT.CHDHIF bit along with the Channel Block Transfer Complete Interrupt Flag (DCHxINT.CHBCIF) bit.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |


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## 43. Module: Device

When the Peripheral Bus x Clock Divisor Control bits (PBxDIV.PBDIV) are greater or equal to three and the device is set in Sleep mode, the device cannot be woken up by a pin change interrupt.

**Work around**

Change the PBxDIV.PBDIV bits to equal or less than two before entering Sleep mode, then return PBxDIV.PBDIV to the required value after waking up from sleep mode.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 44. Module: Timer2-9

If timer match coincides with entry into Sleep mode, timer event triggers and interrupt may not occur.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A3 | B2 | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001320G):

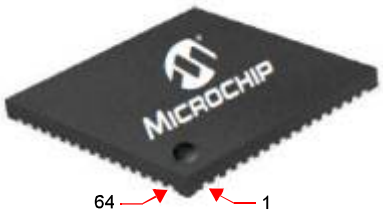
**Note:** Corrections in tables are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

### 1. Module: Ethernet

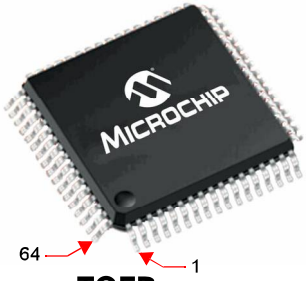
In Table 2. "*Pin Names for 64-pin QFN and TQFP Devices*" of the current data sheet, the AECRSDV signal was erroneously omitted from the pin number 44 and added to the pin number 62. The correct assignment is shown in bold type in the following table.

**64-PIN QFN(4) AND TQFP (TOP VIEW)**

**PIC32MZ0512EF(E/F/K)064**
**PIC32MZ1024EF(G/H/M)064**
**PIC32MZ1024EF(E/F/K)064**
**PIC32MZ2048EF(G/H/M)064**




QFN(4)




TQFP

| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 1 | AN17/ETXEN/RPE5/PMD5/RE5 | 33 | VBUS |
| 2 | AN16/ETXD0/PMD6/RE6 | 34 | VUSB3V3 |
| 3 | AN15/ETXD1/PMD7/RE7 | 35 | VSS |
| 4 | AN14/C1IND/RPG6/SCK2/PMA5/RG6 | 36 | D- |
| 5 | AN13/C1INC/RPG7/SDA4/PMA4/RG7 | 37 | D+ |
| 6 | AN12/C2IND/RPG8/SCL4/PMA3/RG8 | 38 | RPF3/USBID/RF3 |
| 7 | VSS | 39 | VDD |
| 8 | VDD | 40 | VSS |
| 9 | $\overline{\text{MCLR}}$ | 41 | RPF4/SDA5/PMA9/RF4 |
| 10 | AN11/C2INC/RPG9/PMA2/RG9 | 42 | RPF5/SCL5/PMA8/RF5 |
| 11 | AN45/C1INA/RPB5/RB5 | 43 | AERXD0/ETXD2/RPD9/SDA1/PMCS2/PMA15/RD9 |
| 12 | AN4/C1INB/RB4 | 44 | **AECRSDV/ECOL/RPD10/SCL1/SCK4/RD10** |
| 13 | AN3/C2INA/RPB3/RB3 | 45 | AERXCLK/AEREFCLK/ECRS/RPD11/PMCS1/PMA14/RD11 |
| 14 | AN2/C2INB/RPB2/RB2 | 46 | AERXD1/ETXD3/RPD0/RTCC/INT0/RD0 |
| 15 | PGEC1/VREF-/CVREF-/AN1/RPB1/RB1 | 47 | SOSCI/RPC13/RC13 |
| 16 | PGED1/VREF+/CVREF+/AN0/RPB0/PMA6/RB0 | 48 | SOSCO/RPC14/T1CK/RC14 |
| 17 | PGEC2/AN46/RPB6/RB6 | 49 | EMDIO/AEMDIO/RPD1/SCK1/RD1 |
| 18 | PGED2/AN47/RPB7/RB7 | 50 | ETXERR/AETXEN/RPD2/SDA3/RD2 |
| 19 | AVDD | 51 | AERXERR/ETXCLK/RPD3/SCL3/RD3 |
| 20 | AVss | 52 | $\overline{\text{SQICS0}}$/RPD4/PMWR/RD4 |
| 21 | AN48/RPB8/PMA10/RB8 | 53 | $\overline{\text{SQICS1}}$/RPD5/PMRD/RD5 |
| 22 | AN49/RPB9/PMA7/RB9 | 54 | VDD |
| 23 | TMS/CVREFOUT/AN5/RPB10/PMA13/RB10 | 55 | VSS |
| 24 | TDO/AN6/PMA12/RB11 | 56 | ERXD3/AETXD1/RPF0/RF0 |
| 25 | VSS | 57 | TRCLK/SQICLK/ERXD2/AETXD0/RPF1/RF1 |
| 26 | VDD | 58 | TRD0/SQID0/ERXD1/PMD0/RE0 |
| 27 | TCK/AN7/PMA11/RB12 | 59 | VSS |
| 28 | TDI/AN8/RB13 | 60 | VDD |

**Note**
1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.4 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RBx-RGx) can be used as a change notification pin (CNBx-CNGx). See **Section 12.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.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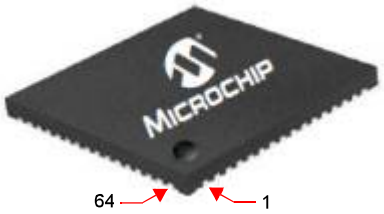
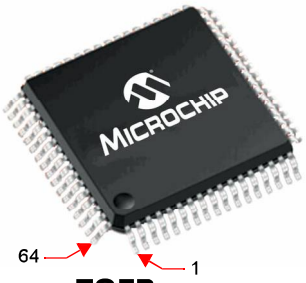
**64-PIN QFN(4) AND TQFP (TOP VIEW)**

**PIC32MZ0512EF(E/F/K)064**
**PIC32MZ1024EF(G/H/M)064**
**PIC32MZ1024EF(E/F/K)064**
**PIC32MZ2048EF(G/H/M)064**




**QFN(4)**




**TQFP**

| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 29 | AN9/RPB14/SCK3/PMA1/RB14 | 61 | TRD1/SQID1/ERXD0/PMD1/RE1 |
| 30 | AN10/EMDC/AEMDC/RPB15/OCFB/PMA0/RB15 | 62 | TRD2/SQID2/ERXDV/ECRSDV/PMD2/RE2 |
| 31 | OSC1/CLKI/RC12 | 63 | TRD3/SQID3/ERXCLK/EREFCLK/RPE3/PMD3/RE3 |
| 32 | OSC2/CLKO/RC15 | 64 | AN18/ERXERR/PMD4/RE4 |

**Note 1:** The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.4 "Peripheral Pin Select (PPS)"** for restrictions.
**2:** Every I/O port pin (RBx-RGx) can be used as a change notification pin (CNBx-CNGx). See **Section 12.0 "I/O Ports"** for more information.
**3:** Shaded pins are 5V tolerant.
**4:** The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

## 2. Module: Ethernet

In 64-pin QFN/TQFP column of Table 1-19. "Alternate Ethernet RMII Pinout I/O Descriptions" of the current data sheet, the AECRSDV signal was erroneously assigned to the pin number 62 instead of the pin number 44. The correct assignment is shown in bold type in the following table.

| Pin Name | Pin Number | | | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|---|---|
| | 64-pin QFN/ TQFP | 100-pin TQFP | 100-pin TFBGA | 124-pin VTLA | 144-pin TQFP/ LQFP | 144-pin TFBGA | | | |
| AERXD0 | 43 | 18 | A3 | — | — | — | I | ST | Alternate Ethernet Receive Data 0 |
| AERXD1 | 46 | 19 | A4 | — | — | — | I | ST | Alternate Ethernet Receive Data 1 |
| AERXERR | 51 | 1 | A9 | — | — | — | I | ST | Alternate Ethernet Receive Error Input |
| AETXD0 | 57 | 47 | J2 | — | — | — | O | — | Alternate Ethernet Transmit Data 0 |
| AETXD1 | 56 | 48 | J1 | — | — | — | O | — | Alternate Ethernet Transmit Data 1 |
| AEMDC | 30 | 70 | K8 | — | — | — | O | — | Alternate Ethernet Management Data Clock |
| AEMDIO | 49 | 71 | J8 | — | — | — | I/O | — | Alternate Ethernet Management Data |
| AETXEN | 50 | 67 | J6 | — | — | — | O | — | Alternate Ethernet Transmit Enable |
| AEREFCLK | 45 | 16 | D4 | — | — | — | I | ST | Alternate Ethernet Reference Clock |
| AECRSDV | **44** | 12 | C5 | — | — | — | I | ST | Alternate Ethernet Carrier Sense Data Valid |

**Legend:** CMOS = CMOS-compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = Transistor-transistor Logic input buffer; Analog = Analog input; O = Output; PPS = Peripheral Pin Select; P = Power; I = Input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## 3. Module: EBI

The minimum values from Table 37-47. "EBI Timing Requirements" in the current product Data Sheet was erroneous. The correct values are listed in the table below:

**TABLE 3-1: EBI TIMING REQUIREMENTS(1)**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| EB10 | TEBICLK | Internal EBI Clock Period (PBCLK8) | **10** | — | — | ns | — |
| EB11 | TEBIRC | EBI Read Cycle Time (TRC<5:0>) | **30** | — | — | ns | — |
| EB12 | TEBIPRC | EBI Page Read Cycle Time (TPRC<3:0>) | **30** | — | — | ns | — |
| EB13 | TEBIAS | EBI Write Address Setup (TAS<1:0>) | **15** | — | — | ns | — |
| EB14 | TEBIWP | EBI Write Pulse Width (TWP<5:0>) | **25** | — | — | ns | — |
| EB15 | TEBIWR | EBI Write Recovery Time (TWR<1:0>) | **15** | — | — | ns | — |
| EB16 | TEBICO | EBI Output Control Signal Delay | — | — | 5 | ns | See **Note 2** |
| EB17 | TEBIDO | EBI Output Data Signal Delay | — | — | 5 | ns | See **Note 2** |
| EB18 | TEBIDS | EBI Input Data Setup | **10** | — | — | ns | See **Note 2** |
| EB19 | TEBIDH | EBI Input Data Hold | **3** | — | — | ns | See **Note 2, 3** |

**Note 1:** EBI Timings Requirements data are from simulation.

**2:** Maximum pin capacitance = 10 pF.

**3:** Hold time from EBI Address change is 0 ns.

## APPENDIX A: REVISION HISTORY

Rev A Document (7/2015)

Initial release of this document issued for revision A1 silicon, which includes silicon issues 1. Module: (Oscillator), 2. Module: (Oscillator), 3. Module: (Oscillator), 4. Module: (Secondary Oscillator), 5. Module: (Power-Saving), 6. Module: ($I^2C$), 7. Module: (UART), 8. Module: (UART), 9. Module: (USB), and Power-Saving Modes.

Rev B Document (4/2016)

Added silicon issues 11. Module: (ADC) and 12. Module: (ADC).

Updated silicon issues 2. Module: (Oscillator) and 10. Module: (Power-Saving Modes).

Rev C Document (7/2016)

Updated to include silicon revision A3.

Updated silicon issues 2. Module: (Oscillator), 6. Module: ($I^2C$), and 11. Module: (ADC).

Added silicon issues 13. Module: (ADC), 14. Module: (ADC), 15. Module: (ADC), and 16. Module: (USB).

Added data sheet clarifications 1. Module: (Resets) and 2. Module: (Interrupt Controller).

Rev D Document (9/2016)

Updated Figure 1 and Table 3 in silicon issue 2. Module: (Oscillator).

Added silicon issues 17. Module: (Oscillator) and 18. Module: (Temperature Sensor).

Added data sheet clarification 3. Module: (External Clock Timing Requirements).

Rev E Document (3/2018)

Internal release, minor content edits gone into this release.

Rev F Document (4/2018)

Added silicon issues: 19. Module: (ICSP), 20. Module: (DMA), 21. Module: (PMP), 22. Module: (Sleep), 23. Module: (SQI), 24. Module: (POR), 25. Module: (Crypto), 26. Module: (Crypto), 27. Module: (SPI), 28. Module: (SQI), and 29. Module: (Sleep).

All data sheet clarifications were removed.

Rev G Document (6/2018)

Updated to include silicon revision B2.

Added silicon issue 30. Module:Security.

Rev H Document (9/2018)

Added Silicon issues: 31. Module:UART.

Rev J Document (2/2019)

Added Silicon Issue 32. Module:Reset.

Added Data Sheet Clarifications: 1. Module:Ethernet, Appendix A:Revision History, and 33. Module:I2C3.

Updated Silicon Issue 2. Module:Oscillator.

Rev K Document (01/2020)

Added Silicon Issues 34. Module:USB, 35. Module:USB, 36. Module:USB, and 37. Module:I2C

Updated Silicon issue 28. Module:SQI.

All data sheet clarifications were removed.

Rev. L Document (06/2020)

Added silicon Issue 38. Module:System Bus.

Updated silicon issue 24. Module:POR.

Rev. M Document (09/2020)

Added Data Sheet Clarifications 1. Module:Ethernet, and 2. Module:Ethernet.

Updated TABLE 2:Silicon Issue Summary for issue 1 to include revision B2 silicon


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Rev. N Document (05/2021)

Terminology for “Master” and “Slave” was updated to “Host” and “Client” respectively. This change may not be reflected in all associated Microchip documentation. For more information, contact a Microchip sales representative.

Added a new Data Sheet Clarification for 3. Module:EBI.

Added the following new silicon issues:

- 39. Module: (ADC)
- 40. Module: (USB)
- 41. Module: (EBI)
- 42. Module: (DMA)
- 43. Module: (Device)
- 44. Module: (Timer2-9)

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