Product Change Notification / SYST-25LGPN222

Date:

26-Mar-2021

Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ERRATA - PIC16(L)F15324/44 Family Silicon Errata and Data Sheet Clarification Errata Document Revision

Affected CPNs:

SYST-25LGPN222_Affected_CPN_03262021.pdf
SYST-25LGPN222_Affected_CPN_03262021.csv

Notification Text:

SYST-25LGPN222

Microchip has released a new Product Documents for the PIC16(L)F15324/44 Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at PIC16(L)F15324/44 Family Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change: 1) Updated Table 2 and 37-1 and Section 1.3 Minimum VDD Specifications. Other minor corrections.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 26 Mar 2021

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

PIC16(L)F15324/44 Family Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

PIC16F15325-E/JQ
PIC16F15325-E/JQVAO
PIC16F15325-E/P
PIC16F15325-E/SL
PIC16F15325-E/SLVAO
PIC16F15325-E/ST
PIC16F15325-I/JQ
PIC16F15325-I/P
PIC16F15325-I/SL
PIC16F15325-I/SLVAO
PIC16F15325-I/ST
PIC16F15325T-E/7NVAO
PIC16F15325T-E/JQ
PIC16F15325T-E/JQVAO
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PIC16F15345-E/GZVAO
PIC16F15345-E/P
PIC16F15345-E/SO
PIC16F15345-E/SS
PIC16F15345-I/GZ
PIC16F15345-I/P
PIC16F15345-I/SO
PIC16F15345-I/SS
PIC16F15345-I/SSVAO
PIC16F15345T-E/6NV05
PIC16F15345T-E/6NVAO
PIC16F15345T-E/GZVAO
PIC16F15345T-E/MLVAO
PIC16F15345T-E/SSVAO
PIC16F15345T-I/GZ
PIC16F15345T-I/SO
PIC16F15345T-I/SS
PIC16F15345T-I/SSV06
PIC16F15345T-I/SSVAO
PIC16LF15325-E/JQ
PIC16LF15325-E/P
PIC16LF15325-E/SL
PIC16LF15325-E/ST
PIC16LF15325-I/JQ
PIC16LF15325-I/P
PIC16LF15325-I/SL

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PIC16LF15325T-E/JQV02
PIC16LF15325T-E/JQVAO
PIC16LF15325T-E/STV03
PIC16LF15325T-E/STVAO
PIC16LF15325T-I/JQ
PIC16LF15325T-I/SL
PIC16LF15325T-I/ST
PIC16LF15345-E/6NVAO
PIC16LF15345-E/GZ
PIC16LF15345-E/P
PIC16LF15345-E/SO
PIC16LF15345-E/SS
PIC16LF15345-I/GZ
PIC16LF15345-I/P
PIC16LF15345-I/SO
PIC16LF15345-I/SS
PIC16LF15345-I/SSVAO
PIC16LF15345T-E/6NVAO
PIC16LF15345T-E/GZVAO
PIC16LF15345T-E/SS
PIC16LF15345T-I/GZ
PIC16LF15345T-I/SO
PIC16LF15345T-I/SS
PIC16LF15345T-I/SSV04
PIC16LF15345T-I/SSVAO

PIC16(L)F15325/45

PIC16(L)F15325/45 Family
Silicon Errata and Data Sheet Clarification

The PIC16(L)F15325/45 family devices that you have received conform functionally to the current Device Data Sheet (DS40001865**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F15325/45 silicon.

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A2**).

Data Sheet clarifications and corrections start on page 6, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® X IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB X IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB X IDE project.
3. Configure the MPLAB X IDE project for the appropriate device and hardware debugger.
4. For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

> **Note:** If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F15325/45 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)	
		A1	A2
PIC16F15325	30C6h	2001h	2002h
PIC16LF15325	30C7h	2001h	2002h
PIC16F15345	30C8h	2001h	2002h
PIC16LF15345	30C9h	2001h	2002h

Note 1: The Device IDs (DEVID and DEVREV) are located at addresses 8006h and 8005h, respectively. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC16(L)F153XX Memory Programming Specification"* (DS40001838) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)	
				A1	A2
Analog-to-Digital Converter (ADC)	ADC Positive Voltage Reference	1.1	Using FVR as the positive voltage reference to the ADC can cause missing codes in the conversion result.	X	X
Development Support	Data Breakpoints	2.1	Data breakpoints are not available on Banks 59 through 63.	X	
Windowed Watchdog Timer (WWDT)	Watchdog Timer Clock Source	3.1	WWDT does not work with SOSC as the clock source.	X	
	Window Operation in DOZE Mode	3.2	Window feature of the WWDT does not operate correctly in DOZE mode.	X	X
I/O Ports	SMBus Mode	4.1	SMBus levels are not functional on RB4 and RB6 PORT pins.	X	
	Slew Rate Control	4.2	Slew Rate Control feature does not exist on RB4 and RB6 PORT pins.	X	
Electrical Specifications	SMBus V_{IL}	5.1	The maximum V_{IL} level changes when V_{DD} is below 4.0V.	X	
	Fixed Voltage Reference (FVR) Accuracy	5.2	FVR output tolerance may be higher than specified at temperatures below -20°C.	X	X
	Minimum V_{DD} Specification for LF Devices	5.3	V_{DDMIN} specifications are changed for LF devices only.	X	X
	ADC Offset Error	5.4	ADC Offset Error specification changed.	X	X
Host Synchronous Serial Port (MSSP)	SPI Client Mode	6.1	SSPBUF transmit shift register may be corrupted under certain conditions.	X	X
Nonvolatile Memory (NVM)	WRERR Bit Operation	7.1	When performing an NVM high-voltage operation, if a Reset is issued in the middle of the operation, the WRERR bit is set. Then, if the user clears the WRERR bit and a Reset occurs again, this sets the WRERR bit because the internal latch has not been cleared earlier.	X	X
Digital-to-Analog (DAC)	Debug Mode	8.1	FVR as the positive voltage source is not functional in Debug mode.	X	X
Reference Clock Output Module (CLKR)	CLKR Output	9.1	First output pulse of Reference Clock Output module is incorrect when CLKREN is enabled.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A2**).

1. Module: Analog-to-Digital Converter (ADC)

1.1 ADC Positive Voltage Reference

Using the FVR as the positive voltage reference to the ADC can cause an increase in missing codes.

Work around

1. Increase the bit conversion time, known as TAD, to 8 us.
2. Use VDD as the positive voltage reference to the ADC.

Affected Silicon Revisions

A1	A2						
X	X						

2. Module: Development Support

2.1 Data Breakpoints

Data breakpoints are not available on Banks 59 through 63. Any breakpoints that are placed in Banks 59 through 63 will fail to be recognized.

Work around

None.

Affected Silicon Revisions

A1	A2						
X							

3. Module: Windowed Watchdog Timer (WWDT)

3.1 WWDT Clock Source Selection

When the WDTCS [2:0] bits of the WDTCON1 register are set to 'b010', selecting the Secondary Oscillator SOSC 32 kHz, as the clock source, the WWDT does not operate.

Work around

Use the LFINTOSC or MFINTOSC clock sources for the WWDT.

Affected Silicon Revisions

A1	A2						
X							

3.2 Window Feature of the WWDT Does Not Operate Correctly in DOZE Mode

When the Windowed mode of operation is enabled in DOZE mode, a window violation error is issued even though the window is open and has been armed. This condition occurs only when the window size is set to a value other than 100% open.

Work around

1. Use the Windowed mode of operation in any other mode than DOZE. If disabling the DOZE mode is not an option, use the WWDT module without the window being enabled.
2. If the device is in DOZE mode, perform the arming process for the window in NORMAL mode, and return to the DOZE mode.
3. If there is an ISR in the application code, the arming within the window can be done inside the ISR with the ROI bit of the CPUDOZE register being set.

Affected Silicon Revisions

A1	A2						
X	X						

4. Module: I/O Ports

4.1 SMBus Mode

The SMBus signal levels are not available for the I^2C functions of pins RB4 and RB6.

Standard ST and TTL levels are still available for these pins, which are configurable through the INLVLB register settings.

Work around

Use the Peripheral Pin Select (PPS) feature and move the required I^2C functions to PORTC where the SMBus levels are still available.

Affected Silicon Revisions

A1	A2						
X							

4.2 Slew Rate Control

The Slew Rate Control feature is not available on pins RB4 and RB6.

Work around

Use other available PORT pins when slew rate control is required.

Affected Silicon Revisions

A1	A2						
X							

5. Module: Electrical Specifications

5.1 SMBus VIL Level

When the VDD voltage level supplied to the device is 4.0V and above, the maximum SMBus voltage level for the VIL parameter is 0.8V. When VDD drops below 4.0V, the maximum SMBus voltage level for VIL drops to 0.7V.

Work around

None.

Affected Silicon Revisions

A1	A2						
X							

5.2 Fixed Voltage Reference (FVR) Accuracy

At temperatures below -20°C, the output voltage for the FVR may be greater than the level specified in the data sheet. This will apply to all three gain amplifier settings (1X, 2X, 4X). The affected parameter numbers found in the data sheet are: FVR01 (1X gain setting), FVR02 (2X gain setting), and FVR03 (4X gain setting).

Work around

None.

Affected Silicon Revisions

A1	A2						
X	X						

5.3 Minimum VDD Specifications for LF Devices

VDDMIN at -40°C and +25°C = 2.3V. (See **TABLE 37-1: Supply Voltage** on the following page for reference.)

Work around

None.

Affected Silicon Revisions

A1	A2						
X	X						

5.4 ADC Offset Error

The table containing the Offset Error specification (AD04:EOFF) for the Analog-to-Digital Converter is modified. The updated value for Offset Error specification is +/- 3.0 LSb.

Work around

None.

Affected Silicon Revisions

A1	A2						
X	X						

6. Module: Host Synchronous Serial Port (MSSP)

6.1 SSPBUF May Become Corrupted

When operating in SPI Client mode, if the incoming SCK clock signal arrives during any of the conditions below, the SSPBUF transmit shift register may become corrupted. The transmitted client byte cannot be ensured to be correct, and the state of the WCOL bit may or may not indicate a write collision.

These conditions include:

- A write to an SFR
- A write to RAM following an SFR read
- A write to RAM prior to an SFR read

Work around

Method 1 (Interrupt Based Using $\overline{SS}$):

1. Connect the $\overline{SS}$ line to both the $\overline{SS}$ input and either an INT or IOC input pin.
2. Enable INT or IOC interrupts (interrupt on falling edge if available, otherwise check that $\overline{SS}$ == 0 when the interrupt occurs).
3. Load SSPBUF with the data to be transmitted.
4. Continue program execution.
5. When the Interrupt Service Routine (ISR) is invoked, do either of the following:

   • Add a delay that ensures the first SCK clock will be complete, or

   • Poll SSPSTAT.BF (while(BF == 0)) and wait for the transmission/reception to complete.

   Once either of these is complete, it is safe to return to program execution.

Method 2 (Bit Polling Based Using $\overline{SS}$):

1. Load SSPBUF with the data to be transmitted.
2. Poll the $\overline{SS}$ line and wait for the $\overline{SS}$ to go active (while(!PORTx.nSS == 0)).
3. When $\overline{SS}$ is active ($\overline{SS}$ == 0), do either of the following:

   • Add a delay that ensures the first SCK clock will be complete, or

   • Poll SSPSTAT.BF (while(BF == 0)) and wait for the transmission/reception to complete.

   Once one of these two methods is complete, it is safe to return to program execution.

Method 3 ($\overline{SS}$ Not Available):

1. Load SSPBUF with the data to be transmitted.
2. Poll SSPSTAT.BF (while(BF == 0)), and wait for the transmission/reception to complete.

Affected Silicon Revisions

A1	A2						
X	X						

7. Module: Nonvolatile Memory (NVM)

7.1 WRERR Bit Operation

When a Reset is issued while an NVM high-voltage operation is in progress, the WRERR bit in the NVMCON1 register is set as expected. After clearing the WRERR bit, if a Reset reoccurs, the WRERR bit is set again regardless of whether an NVM operation is in progress or not. A successful write operation will clear the WRERR condition.

Work around

None.

Affected Silicon Revisions

A1	A2						
X	X						

8. Module: Digital-to-Analog (DAC)

8.1 FVR as the Positive Voltage Source Is Not Functional in Debug Mode

When using the DAC module while in Debug mode, and selecting the FVR as the positive voltage source, DAC1PSS = 10, the DAC is not functional and unexpected results can be seen on the output.

Work around

None.

Affected Silicon Revisions

A1	A2						
X	X						

9. Module: Reference Clock Output Module (CLKR)

9.1 First Output Pulse of Reference Clock Output Module Is Incorrect When CLKREN Is Enabled

If CLKREN bit is set by the user, the number of input clock cycles taken to generate the reference clock output might vary by one cycle due to a race condition. This condition occurs only if LCx_out or NCOx_out are the inputs (CLKRCLK bits) to the CLKR module.

Work around

Ignore the first output pulse of the CLKR output signal.

Affected Silicon Revisions

A1	A2						
X	X						

TABLE 37-1: SUPPLY VOLTAGE

PIC16LF15325/45			Standard Operating Conditions (Unless Otherwise Stated)				
Param. No.	Sym.	Characteristic	Min.	Typ.†	Max.	Units	Conditions
D002	VDD		1.8	—	3.6	V	FOSC ≤ 16 MHz, +25°C ≤ TA ≤ +125°C
			2.3	—	3.6	V	FOSC ≤ 16 MHz, -40°C ≤ TA ≤ +25°C
			2.5	—	3.6	V	FOSC > 16 MHz

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001865**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

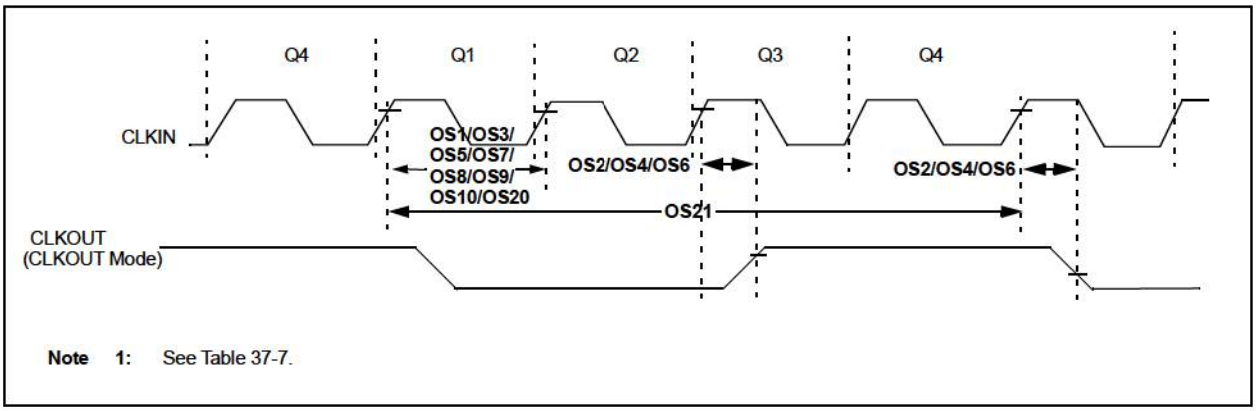
1. Module: Table 36.3 Instruction Set Literal Operations

LITERAL OPERATIONS									
ADDLW	k	Add literal and W	1	11	1110	kkkk	kkkk	C, DC, Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLB	**k**	**Move literal to BSR**	**1**	**00**	**0001**	**01kk**	**kkkk**		
MOVLP	k	Move literal to PCLATH	1	11	0001	1kkk	kkkk		
MOVLW	k	Move literal to W	1	11	0000	kkkk	kkkk		
SUBLW	k	Subtract W from literal	1	11	1100	kkkk	kkkk	C, DC, Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

2. Module: Electrical Specifications

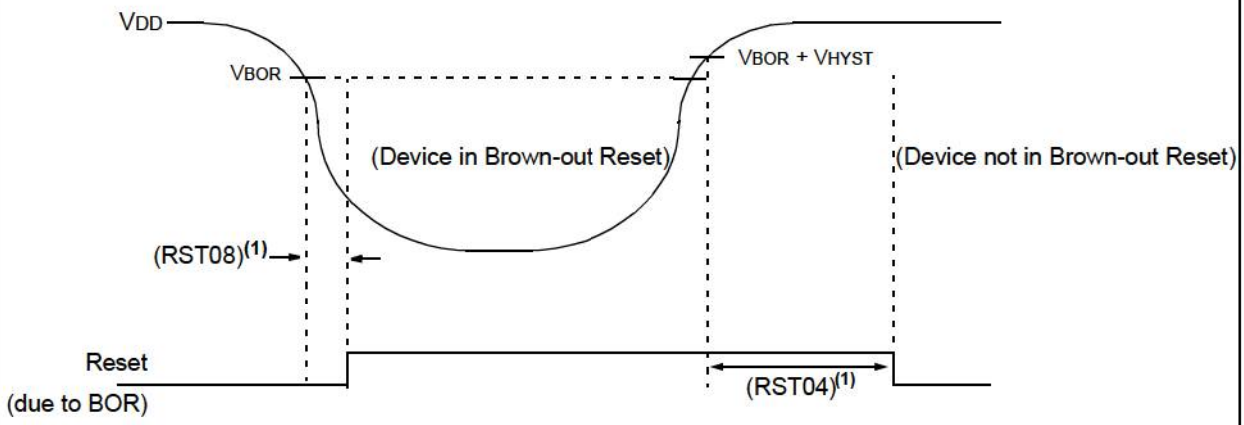
2.1 Figure 37-5: Clock Timing

Figure 37-5 incorrectly shows the location of parameters OS1, OS2, OS3, OS4, OS5, OS6, OS7, OS8, OS9, OS10, OS20 and OS21. The correct location for the above-mentioned parameters is depicted in the following figure.



2.2 Figure 37-9: Brown-Out Reset Timing and Characteristics

Note 1 in Figure 37-9 is incorrect. The correct note along with the figure is depicted below.



Note 1: 64 ms delay only if $\overline{\text{PWRTE}}$ bit in the Configuration Word register is programmed to '**0**'.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev D Document (03/2021)

Updated Table 2 and 37-1 and Section 5.3 Minimum V_{DD} Specifications. Other minor corrections.

Data Sheet Clarifications:
Added Module 2: Electrical Specifications.

Rev C Document (11/2020)

Updated Table 2 and Section 5.3 Minimum V_{DD} Specification for LF Devices; Added Table 3 and Section 5.4 ADC Offset Error.

Rev B Document (07/2019)

Updated Table 2, Section 3. Module: Windowed Watchdog Timer (WWDT), Section 5. Module: Electrical Specifications; Added Section 6. Module: Host Synchronous Serial Port (MISSP), Section 8.1 Digital-to-Analog, and Section 9.1 Reference Clock Output Module.

Data Sheet Clarifications:
Added Module 1: Table 36.3 Instruction Set.

Rev A Document (12/2016)

Initial release of this document.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
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