Product Change Notification / SYST-07ATNE052

Date:

08-Jan-2021

Product Category:

32-bit Microcontrollers

PCN Type:

Silicon Die Revision

Notification Subject:

ERRATA - SAM L10/L11 Family Silicon Errata and Data Sheet Clarification

Affected CPNs:

SYST-07ATNE052_Affected_CPN_01082021.pdf
SYST-07ATNE052_Affected_CPN_01082021.csv

Notification Text:

SYST-07ATNE052

Microchip has released a new Product Documents for the SAM L10/L11 Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at SAM L10/L11 Family Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change: This revision contains numerous typographical updates, and formatting updates.
The following errata were updated with new verbiage:
• DMAC: 2.4.1 Concurrent Channels Trigger
• EIC: 2.5.1 PAC Protection
• OPAMP: 2.8.1 Reference Buffer
• SERCOM I2C: 2.10.8 Status Flags
• SERCOM I2C: 2.10.9 Status Flags
• SERCOM SPI: 2.11.1 Data Preload
• SERCOM USART: 2.12.5
The following errata were added in this revision:
• ADC: 2.1.2 Offset Correction
• Device: 2.3.2 Standby Entry

• RTC: 2.9.9 Tamper Detection
• RTC: 2.9.10 Tamper Detection
• RTC: 2.9.11 General Purpose Registers
• SERCOM I2C: 2.10.10 Status Flags
• SERCOM SPI: 2.11.2 Hardware Slave Select Control
• SERCOM SPI: 2.11.3 Slave Data Preload
• SERCOM SPI: 2.11.4 Wakeup Interrupt
• SERCOM USART: 2.12.6 Overconsumption in Standby Mode
• SERCOM USART: 2.12.7 Wakeup Interrupt
• TC: 2.13.3 Retrigger
• OSC32KCTRL: 2.16.2 1024 Hz Clock Output
• OSC32KCTRL: 2.16.3 Clock Failure Detection
• OSC32KCTRL: 2.16.4 XOSC32K Ready Bit
• EVSYS: 2.18.1 Synchronous and Resynchronized Modes
• EVSYS: 2.18.2 Synchronous Mode
• OSCCTRL: 2.19.1 Clock Failure Detection
• OSCCTRL: 2.19.2 Clock Failure Detection
• OSCCTRL: 2.19.3 XOSC Ready Bit
• PORT: 2.20.1 IOBUS
• TRAM: 2.21.1 PAC Protection

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 08 Jan 2021

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

SAM L10/L11 Family Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

Terms and Conditions:

If you wish to receive Microchip PCNs via email please register for our PCN email service at our PCN home page select register then fill in the required fields. You will find instructions about registering for Microchips PCN email service in the PCN FAQ section.

If you wish to change your PCN profile, including opt out, please go to the PCN home page select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.

Affected Catalog Part Numbers (CPN)

ATSAML10D14A-MF
ATSAML10D14A-MFT
ATSAML10D14A-MU
ATSAML10D14A-MUT
ATSAML10D14A-YF
ATSAML10D14A-YFT
ATSAML10D14A-YU
ATSAML10D14A-YUT
ATSAML10D15A-MF
ATSAML10D15A-MFT
ATSAML10D15A-MU
ATSAML10D15A-MUT
ATSAML10D15A-MZ
ATSAML10D15A-MZT
ATSAML10D15A-YF
ATSAML10D15A-YFT
ATSAML10D15A-YU
ATSAML10D15A-YUT
ATSAML10D16A-MF
ATSAML10D16A-MFT
ATSAML10D16A-MU
ATSAML10D16A-MUT
ATSAML10D16A-MZ
ATSAML10D16A-MZT
ATSAML10D16A-MZTV01
ATSAML10D16A-MZTVAO
ATSAML10D16A-YF
ATSAML10D16A-YFT
ATSAML10D16A-YU
ATSAML10D16A-YUT
ATSAML10E14A-AF
ATSAML10E14A-AFT
ATSAML10E14A-AU
ATSAML10E14A-AUT
ATSAML10E14A-MF
ATSAML10E14A-MFT
ATSAML10E14A-MU
ATSAML10E14A-MUT
ATSAML10E14A-UUT
ATSAML10E15A-AF
ATSAML10E15A-AFT
ATSAML10E15A-AU
ATSAML10E15A-AUT
ATSAML10E15A-AZ
ATSAML10E15A-AZT
ATSAML10E15A-MF

ATSAML10E15A-MFT
ATSAML10E15A-MU
ATSAML10E15A-MUT
ATSAML10E15A-MZ
ATSAML10E15A-MZT
ATSAML10E15A-UUT
ATSAML10E16A-AF
ATSAML10E16A-AFT
ATSAML10E16A-AU
ATSAML10E16A-AUT
ATSAML10E16A-AZ
ATSAML10E16A-AZT
ATSAML10E16A-MF
ATSAML10E16A-MFT
ATSAML10E16A-MU
ATSAML10E16A-MUT
ATSAML10E16A-MZ
ATSAML10E16A-MZT
ATSAML10E16A-MZTV02
ATSAML10E16A-UUT
ATSAML11D14A-MF
ATSAML11D14A-MFT
ATSAML11D14A-MU
ATSAML11D14A-MUT
ATSAML11D14A-YF
ATSAML11D14A-YFT
ATSAML11D14A-YU
ATSAML11D14A-YUT
ATSAML11D15A-MF
ATSAML11D15A-MFKPH
ATSAML11D15A-MFT
ATSAML11D15A-MFTKPH
ATSAML11D15A-MU
ATSAML11D15A-MUKPH
ATSAML11D15A-MUT
ATSAML11D15A-MUTKPH
ATSAML11D15A-MZ
ATSAML11D15A-MZT
ATSAML11D15A-YF
ATSAML11D15A-YFT
ATSAML11D15A-YU
ATSAML11D15A-YUT
ATSAML11D16A-MF
ATSAML11D16A-MFKPH
ATSAML11D16A-MFT
ATSAML11D16A-MFTKPH
ATSAML11D16A-MU
ATSAML11D16A-MUKPH
ATSAML11D16A-MUT

ATSAML11D16A-MUTKPH
ATSAML11D16A-MZ
ATSAML11D16A-MZT
ATSAML11D16A-YF
ATSAML11D16A-YFT
ATSAML11D16A-YU
ATSAML11D16A-YUT
ATSAML11E14A-AF
ATSAML11E14A-AFT
ATSAML11E14A-AU
ATSAML11E14A-AUT
ATSAML11E14A-MF
ATSAML11E14A-MFT
ATSAML11E14A-MU
ATSAML11E14A-MUT
ATSAML11E14A-UUT
ATSAML11E15A-AF
ATSAML11E15A-AFKPH
ATSAML11E15A-AFT
ATSAML11E15A-AFTKPH
ATSAML11E15A-AU
ATSAML11E15A-AUKPH
ATSAML11E15A-AUT
ATSAML11E15A-AUTKPH
ATSAML11E15A-AZ
ATSAML11E15A-AZT
ATSAML11E15A-MF
ATSAML11E15A-MFKPH
ATSAML11E15A-MFT
ATSAML11E15A-MFTKPH
ATSAML11E15A-MU
ATSAML11E15A-MUKPH
ATSAML11E15A-MUT
ATSAML11E15A-MUTKPH
ATSAML11E15A-MZ
ATSAML11E15A-MZT
ATSAML11E15A-UUT
ATSAML11E16A-AF
ATSAML11E16A-AFKPH
ATSAML11E16A-AFT
ATSAML11E16A-AFTKPH
ATSAML11E16A-AU
ATSAML11E16A-AUKPH
ATSAML11E16A-AUT
ATSAML11E16A-AUTKPH
ATSAML11E16A-AZ
ATSAML11E16A-AZT
ATSAML11E16A-MF
ATSAML11E16A-MFKPH

ATSAML11E16A-MFT
ATSAML11E16A-MFTKPH
ATSAML11E16A-MU
ATSAML11E16A-MUKPH
ATSAML11E16A-MUT
ATSAML11E16A-MUTKPH
ATSAML11E16A-MZ
ATSAML11E16A-MZT
ATSAML11E16A-MZTVAO
ATSAML11E16A-UUT

SAM L10/L11 Family

Silicon Errata and Data Sheet Clarification

SAM L10/L11 Family

The SAM L10/L11 family of devices that you have received conform functionally to the current Device Data Sheet (DS60001513F), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the following tables. The silicon issues are summarized in the Silicon Issue Summary.

The errata described in this document will be addressed in future revisions of the SAM L10/L11 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Data Sheet clarifications and corrections (if applicable) are located in 3. Data Sheet Clarifications, following the discussion of silicon issues.

Table 1. SAM L10 Family Silicon Device Identification

Part Number	Device ID (DID[31:0])	Revision (DID.REVISION[3:0])
		B
SAML10E16A	0x2084xx00	0x1
SAML10E15A	0x2084xx01	
SAML10E14A	0x2084xx02	
SAML10D16A	0x2084xx03	
SAML10D15A	0x2084xx04	
SAML10D14A	0x2084xx05	

Table 2. SAM L11 Family Silicon Device Identification

Part Number	Device ID (DID[31:0])	Revision (DID.REVISION[3:0])
		B
SAML11E16A	0x2083xx00	0x1
SAML11E15A	0x2083xx01	
SAML11E14A	0x2083xx02	
SAML11D16A	0x2083xx03	
SAML11D15A	0x2083xx04	
SAML11D14A	0x2083xx05	

Note: Refer to the “Device Service Unit” chapter in the current Device Data Sheet (DS60001513F) for detailed information on Device Identification and Revision IDs for your specific device.

© 2021 Microchip Technology Inc.

Table of Contents

SAM L10/L11 Family 1

1. Silicon Issue Summary 3

2. SAM L10/L11 Errata Issues 7
   - 2.1. Analog-to-Digital Converter (ADC) 7
   - 2.2. Configurable Custom Logic (CCL) 7
   - 2.3. DEVICE 8
   - 2.4. Direct Memory Access Controller (DMAC) 9
   - 2.5. External Interrupt Controller (EIC) 9
   - 2.6. Frequency Meter (FREQM) 10
   - 2.7. Main Clock (MCLK) 10
   - 2.8. Operational Amplifier Controller (OPAMP) 11
   - 2.9. Real Time Clock (RTC) 12
   - 2.10. Serial Communication Interface Inter-Integrated Circuit (SERCOM I^2C) 15
   - 2.11. Serial Communication Serial Peripheral Interface (SERCOM SPI) 18
   - 2.12. Serial Communication Interface USART (SERCOM USART) 19
   - 2.13. Timer Counter (TC) 21
   - 2.14. True Random Number Generator (TRNG) 22
   - 2.15. Supply Controller (SUPC) 23
   - 2.16. OSC32KCTRL 23
   - 2.17. Boot ROM 25
   - 2.18. Event System (EVSYS) 25
   - 2.19. Oscillator Controller (OSCCTRL) 26
   - 2.20. PORT I/O Controller (PORT) 27
   - 2.21. Trust Ram (TRAM) 27

3. Data Sheet Clarifications 28

4. Revision History 33

The Microchip Web Site 35

Customer Change Notification Service 35

Customer Support 35

Microchip Devices Code Protection Feature 35

Legal Notice 36

Trademarks 36

Quality Management System Certified by DNV 36

Worldwide Sales and Service 37

1. Silicon Issue Summary

Table 1-1. Silicon Issue Summary

Module	Feature	Errata Number	Summary	Device	Affected Silicon Revisions
					B
ADC	Reference Buffer Offset Compensation	2.1.1	First ADC conversions are incorrect when using Reference Buffer Offset Compensation.	SAM L10	X
				SAM L11	X
ADC	Offset Correction	2.1.2	Offset correction is not supported in the 8-bit and 10-bit conversion resolution.	SAM L10	X
				SAM L11	X
CCL	PAC protection	2.2.1	Writing the Software Reset bit in the Control A register will trigger a PAC protection error.	SAM L10	X
				SAM L11	X
CCL	Enable-protected Registers	2.2.2	The SEQCTRL0 and LUCTRL0/1 registers are enable-protected by the CTRL.ENABLE bit.	SAM L10	X
				SAM L11	X
CCL	Sequential logic	2.2.3	LUT Output is corrupted after enabling CCL when sequential logic is used.	SAM L10	X
				SAM L11	X
Device	Temperature sensor	2.3.1	Temperature sensor is not functional.	SAM L10	X
				SAM L11	X
Device	Standby Entry	2.3.2	Potential hard fault upon standby entry when Systick interrupt is enabled	SAM L10	X
				SAM L11	X
DMAC	Concurrent Channels Trigger	2.4.1	When using concurrent channel triggers, DMA write-back descriptors may get corrupted.	SAM L10	X
				SAM L11	X
EIC	PAC protection	2.5.1	8-bit and 16-bit reads/writes on the reserved areas of the EIC registers mapping starting from EVCTRL register do not generate a PAC protection error.	SAM L10	X
				SAM L11	X
FREQM	PAC protection	2.6.1	FREQM reads on the Control B register generate a PAC protection error.	SAM L10	X
				SAM L11	X
MCLK	PAC protection	2.7.1	Writes to the MCLK Control A register do not generate a PAC protection error even if this register has been write-protected using the PAC.	SAM L10	X
				SAM L11	X
MCLK	DFLLULP clock	2.7.2	Hardfault exception after having selected DFLLULP clock as main clock.	SAM L10	X
				SAM L11	X
OPAMP	Reference buffer	2.8.1	The internal reference REFBUF is not generated when the voltage doubler is disabled.	SAM L10	X
				SAM L11	X
OPAMP	High Gain Instrumentation Amplifier	2.8.2	High Gain Instrumentation Amplifier is not functional.	SAM L10	X
				SAM L11	X
RTC	Tamper detection	2.9.1	Tamper detection limitation when CTRLB.SEPTO = 0.	SAM L10	X
				SAM L11	X
RTC	Event generation	2.9.2	Periodic Daily Event (PERD) Event Generator never occurs in Clock/ Calendar mode.	SAM L10	X
				SAM L11	X
RTC	Write corruption	2.9.3	RTC COUNT and CLOCK registers write corruption.	SAM L10	X
				SAM L11	X

.....continued

Module	Feature	Errata Number	Summary	Device	Affected Silicon Revisions
					B
RTC	Tamper Detection Timestamp	2.9.4	If an external reset occurs during a tamper detection, the TIMESTAMP register will not be updated when next tamper detection is triggered.	SAM L10	X
				SAM L11	X
RTC	Prescaler	2.9.5	When the tamper or debouncing features (TAMPCTRL) are enabled, periodic interrupts and events are generated when the prescaler is OFF (CTRLA.PRESCALER=0).	SAM L10	X
				SAM L11	X
RTC	Active Layer Protection	2.9.6	Active Layer Protection feature is limited to one tamper channel n (i.e. one RTC INn/OUTn pair).	SAM L10	X
				SAM L11	X
RTC	Tamper Detection Timestamp	2.9.7	The INTFLAG.TAMPER bit is not reset by reading the TIMESTAMP register.	SAM L10	X
				SAM L11	X
RTC	Tamper Detection Timestamp	2.9.8	A wrong timestamp value can be returned if more than one CPU and DMA accesses to the TIMESTAMP register are performed upon a INTFLAG.TAMPER assertion.	SAM L10	X
				SAM L11	X
RTC	Tamper Detection	2.9.9	If the Tamper Channel n Action is set to WAKE or CAPTURE and the Active Layer Protection is enabled for this channel, no tampers are detected on this channel n.	SAM L10	X
				SAM L11	X
RTC	Tamper Detection	2.9.10	False tamper detections may occur when configuring the RTC INn and OUTn pins.	SAM L10	X
				SAM L11	X
RTC	General Purpose Registers	2.9.11	General Purpose Registers n (GPn) are reset on tamper detection even if GPTRST = 0.	SAM L10	X
				SAM L11	X
SERCOM I^2C	High-speed mode	2.10.1	When configured in HS or Fast-Mode Plus, SDA and SCL fall times are shorter than I^2C specification requirement and can lead to reflection.	SAM L10	X
				SAM L11	X
SERCOM I^2C	Repeated start	2.10.2	Bus error is generated during a Repeated Start (when QCEN = 1 and SCLSM = 1).	SAM L10	X
				SAM L11	X
SERCOM I^2C	Repeated Start / Master mode 10-bit	2.10.3	Repeated Start in 10-bit addressing mode for Master Write operations does not work.	SAM L10	X
				SAM L11	X
SERCOM I^2C	Repeated Start / Master mode 10-bit	2.10.4	Repeated Start is not supported for High-Speed mode Master Read operations.	SAM L10	X
				SAM L11	X
SERCOM I^2C	Repeated Start / High-Speed mode	2.10.5	Repeated Start is not supported for High-Speed mode Master Write operations.	SAM L10	X
				SAM L11	X
SERCOM I^2C	Slave Mode with DMA	2.10.6	Character lost in I^2C Slave mode with DMA when a NACK occurs.	SAM L10	X
				SAM L11	X
SERCOM I^2C	Slave mode 10-bit	2.10.7	I^2C Slave 10-bit addressing mode is not functional.	SAM L10	X
				SAM L11	X
SERCOM I^2C	Status Flags	2.10.8	BUSERR, COLL, LOWTOUT, SEXTTOUT and LENERR Status register bits are not automatically cleared.	SAM L10	X
				SAM L11	X
SERCOM I^2C	Status Flags	2.10.9	The CLKHOLD Status bit is not read only.	SAM L10	X
				SAM L11	X
SERCOM I^2C	Status Flags	2.10.10	When an unexpected STOP occurs on the I^2C bus the STATUS.BUSERR & INTFLAG.ERROR bits are set but may not wake the system from sleep mode.	SAM L10	X
				SAM L11	X

.....continued

Module	Feature	Errata Number	Summary	Device	Affected Silicon Revisions
					B
SERCOM SPI	Data Preload	2.11.1	In SPI Slave mode with Slave Data Preload Enabled, the slave transmitter may discard some data if the master cannot keep the Slave Select pin low until the end of transmission.	SAM L10	X
				SAM L11	X
SERCOM SPI	Hardware Slave Select Control	2.11.2	When Hardware Slave Select Control is enabled, the Slave Select (SS) pin goes high after each byte transfer.	SAM L10	X
				SAM L11	X
SERCOM SPI	Slave Data Preload	2.11.3	Preloading a new SPI data before going into Standby Sleep mode, may lead to extra power consumption.	SAM L10	X
				SAM L11	X
SERCOM SPI	Wakeup Interrupt	2.11.4	The Data Register Empty (DRE) wake-up interrupt is not de-asserted when the register interrupt is cleared (INTFLAG.DRE=0).	SAM L10	X
				SAM L11	X
SERCOM USART	Inverted Bits	2.12.1	The TXINV and RXINV bits in the CTRLA register have inverted functionality.	SAM L10	X
				SAM L11	X
SERCOM USART	ISO7816 Mode	2.12.2	In ISO7816 mode, the SERCOM bus clock continues to run in Stand-by Sleep mode causing an extra power consumption.	SAM L10	X
				SAM L11	X
SERCOM USART	Debug Mode	2.12.3	Debug mode is not functional.	SAM L10	X
				SAM L11	X
SERCOM USART	Collision Detection	2.12.4	Collision Detection does not stop Data Transfer.	SAM L10	X
				SAM L11	X
SERCOM USART	Wakeup	2.12.5	The USART does not wake up the device on Error (INTFLAG.ERROR=1) interrupt.	SAM L10	X
				SAM L11	X
SERCOM USART	Overconsumption in Standby Mode	2.12.6	Unexpected over-consumption in standby mode	SAM L10	X
				SAM L11	X
SERCOM USART	Wakeup Interrupt	2.12.7	The Data Register Empty (DRE) wake-up interrupt is not de-asserted when the register interrupt is cleared (INTFLAG.DRE = 0).	SAM L10	X
				SAM L11	X
TC	Flags Synchronization	2.13.1	The SYNCBUSY.PER/SYNCBUSY.CCx flags are released before the PERBUF/CCBUFx registers are restored to their expected value.	SAM L10	X
				SAM L11	X
TC	Capture mode / Over consumption	2.13.2	Over consumption in Capture mode when entering Standby mode.	SAM L10	X
				SAM L11	X
TC	Retrigger	2.13.3	If a Retrigger event occurs at the Channel Compare Match [n] time, the next Waveform Output [n] is missing or disturbed.	SAM L10	X
				SAM L11	X
TRNG	Over consumption	2.14.1	When TRNG is disabled, some internal logic could continue to operate causing an over consumption.	SAM L10	X
				SAM L11	X
SUPC	Buck Converter Mode	2.15.1	Digital Phase-Locked Loop FDPLL96M cannot be used with main voltage regulator in Buck Converter mode.	SAM L10	X
				SAM L11	X
OSC32KCTRL	External 32.768KHz Crystal Oscillator	2.16.1	External 32.768KHz crystal oscillator operation is not supported over the full temperature range of -40°C to +125°C.	SAM L10	X
				SAM L11	X
OSC32KCTRL	1024 Hz Clock Output	2.16.2	1024 Hz clock output spikes can lead to wrong RTC or Watchdog counting.	SAM L10	X
				SAM L11	X

.....continued

Module	Feature	Errata Number	Summary	Device	Affected Silicon Revisions
					B
OSC32KCTRL	Clock Failure Detection	2.16.3	Re-enabling the Clock Failure Detector when the XOSC32K is enabled can lead to a false Clock Failure Detection.	SAM L10	X
				SAM L11	X
OSC32KCTRL	XOSC32K Ready bit	2.16.4	The XOSC32K Ready bit of the STATUS register is not cleared when disabling the XOSC32K bit at the same time as the Crystal Oscillator	SAM L10	X
				SAM L11	X
Boot ROM	GCM API	2.17.1	GCM API does not follow the Procedure Call Standard for the ARM Architecture (AAPCS)	SAM L10	X
				SAM L11	X
EVSYS	Synchronous and Resynchronised Modes	2.18.1	Spurious Overrun Interrupt following a software event.	SAM L10	X
				SAM L11	X
EVSYS	Synchronous Mode	2.18.2	Spurious Overrun Interrupt when the generic clock for a channel is always on.	SAM L10	X
				SAM L11	X
OSCCTRL	Clock Failure Detection	2.19.1	When the XOSC Clock Failure Detector is enabled and a failure is detected, the XOSC Ready bit is not cleared.	SAM L10	X
				SAM L11	X
OSCCTRL	Clock Failure Detection	2.19.2	Re-enabling the Clock Failure Detector when the XOSC is enabled can lead to a false Clock Failure Detection.	SAM L10	X
				SAM L11	X
OSCCTRL	XOSC Ready Bit	2.19.3	The XOSC Ready bit of the STATUS register is not cleared when disabling the XOSC at the same time as the Crystal Oscillator.	SAM L10	X
				SAM L11	X
PORT	IOBUS	2.20.1	Concurrent accesses on the PORT peripheral registers between the ARM APB and the ARM CPU IOBUS are not supported.	SAM L10	X
				SAM L11	X
TRAM	PAC Protection	2.21.1	Security RAM n registers (RAMn) are not PAC Write-Protected.	SAM L10	X
				SAM L11	X

2. SAM L10/L11 Errata Issues

The following issues apply to the SAM L10/L11 Family devices.

2.1 Analog-to-Digital Converter (ADC)

2.1.1 Reference Buffer Offset Compensation

TUE of the ADC conversion result is out of specification when,

- Using the reference source as REFCTRL.REFSEL ≠ VDDANA
  and
- Reference Buffer Offset Compensation is enabled (REFCTRL.REFCOMP = 1)

Workaround

The first five conversions after enabling ADC must be ignored. All further ADC conversions are within the specification.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.1.2 Offset Correction

Offset correction using the OFFSETCORR register is not supported in the 8-bit and 10-bit conversion resolution.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.2 Configurable Custom Logic (CCL)

2.2.1 PAC Protection

Writing the Software Reset bit in the Control A register (CTRLA.SWRST) will trigger a PAC protection error.

Workaround

Clear the CCL PAC error each time a CCL software reset is executed.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.2.2 Enable Protected Registers

The SEQCTRL0 and LUCTRL0/1 registers are enable-protected by the CTRL.ENABLE bit whereas they should be enable-protected by the LUTCTRL0/1.ENABLE bits.

Workaround
None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.2.3 Sequential Logic

LUT Output is corrupted after enabling CCL when sequential logic is used.

Workaround
Write the CTRL register twice when enabling the CCL.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.3 DEVICE

2.3.1 Temperature Sensor

Temperature Sensor is not functional.

Workaround
None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.3.2 Standby Entry

When the Systick interrupt is enabled and the standby back-bias option is set (STDBYCFG.BBIAS = 1), a hard fault can occur when the Systick interrupt coincides with the standby entry.

Workaround

Disable the Systick interrupt before entering standby and re-enable it after wake up.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.4 Direct Memory Access Controller (DMAC)

2.4.1 Concurrent Channels Trigger

When using concurrent channels triggers, DMAC write-back descriptors may get corrupted.

Workaround

Multiple transfers must only be sequenced using linked descriptors on a single channel.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.5 External Interrupt Controller (EIC)

2.5.1 PAC Protection

8-bit and 16-bit reads/writes on the reserved areas of the EIC registers mapping starting from the EVCTRL register do not generate a PAC protection error.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.6 Frequency Meter (FREQM)

2.6.1 PAC Protection

FREQM reads on the Control B register (FREQM.CTRLB) generate a PAC protection error.

Workaround
None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.7 Main Clock (MCLK)

2.7.1 PAC Protection

Writes to the MCLK Control A register (MCLK.CTRLA) do not generate a PAC protection error even if this register has been write-protected using the PAC.

Workaround
None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.7.2 DFLLULP Clock

A Hard fault exception can occur after selecting the DFLLULP clock as main clock source (CTRLA.CKSEL = 1).

Workaround
Add 6 NOP instructions after writing the CTRAL.CKSEL bit.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.8 Operational Amplifier Controller (OPAMP)

2.8.1 Reference Buffer

The internal reference REFBUF is not generated when the Low-Power Mux feature is enabled (CTRLA.LPMUX = 1).

Workaround

Disable the Low-Power Mux feature (CTRLA.LPMUX = 0) when the internal REFBUF is used.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.8.2 High Gain Instrumentation Amplifier

High Gain Instrumentation Amplifier is not functional.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9 Real Time Clock (RTC)

2.9.1 Tamper Detection

When the RTC Separate Tamper Outputs (SEPTO) bit of the CTRLB register is cleared (CTRLB.SEPTO = 0) and the Active layer protection 0 (ALSI0) bit of the TAMPCTRLB register is set (TAMCTRLB.ALSI0 = 1), the RTC pseudo random pattern is only generated on the TrustRAM Active layer.

Workaround

Set the CTRLB.SEPTO bit to '1' if Tamper Detection is required on the RTC Tamper pins.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9.2 Event Generation

In RTC Clock mode or Calendar mode (CTRLA.MODE = 2), the Periodic Daily Event (PERD) is not generated.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9.3 Write Corruption

A 8-bit or 16-bit write access for a 32-bit register, or 8-bit write access for a 16-bit register can fail for the following registers:

- COUNT register in COUNT32 mode
- COUNT register in COUNT16 mode
- CLOCK register in CLOCK mode

Workaround

Write the registers with:

- A 32-bit write access for:
  - COUNT register in COUNT32 mode
  - CLOCK register in CLOCK mode
- A 16-bit write access for:
  - COUNT register in COUNT16 mode

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9.4 Tamper Detection Timestamp

If an external reset occurs during a tamper detection, the TIMESTAMP register will not be updated when next tamper detection is triggered.

Workaround

Enable RTC tamper interrupt and copy the timestamp from the RTC CLOCK register to one of the following locations:

- SRAM
- GPx register in RTC

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9.5 Prescaler

When the tamper or debouncing features (TAMPCTRL) are enabled, periodic interrupts and events are generated when the prescaler is OFF (CTRLA.PRESCALER = 0).

Workaround

When the prescaler is OFF (CTRLA.PRESCALER = 0), clear the Periodic Interval n Event Output Enable bits (EVCTRL.PEREOn [n = 7...0]) and the respective Periodic Interval n Interrupt Enable (INTENCLR.PERn [n = 7...0]) bits.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9.6 Active Layer Protection

Active Layer Protection feature is limited to one tamper channel n (i.e. one RTC INn/OUTn pair). Any other tamper channels can be used either in Wake mode or Capture mode.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9.7 Tamper Detection Timestamp

The INTFLAG.TAMPER bit is not reset by reading the TIMESTAMP register.

Workaround

Clear the INTFLAG.TAMPER bit by writing a '1' to this bit when the Timestamp value has been read from the TIMESTAMP register.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9.8 Tamper Detection Timestamp

A wrong timestamp value can be returned if more than one CPU and DMA accesses to the TIMESTAMP register are performed upon a INTFLAG.TAMPER assertion.

Workaround

The timestamp value captured in the TIMESTAMP register must be retrieved as described below:

- If RTC can trigger a DMA request when the timestamp value is available (CTRLB.DMAEN = 1):
  - Wait for DMA transfer completion to read the timestamp value from the DMA buffers
  - Clear the INTFLAG.TAMPER bit.

Note: Do not read the timestamp value from the TIMESTAMP register.

- If RTC cannot trigger a DMA request when the timestamp value is available (CTRLB.DMAEN = 0):
  - Wait for the INTFLAG.TAMPER bit to read the timestamp value from the TIMESTAMP register
  - Clear the INTFLAG.TAMPER bit

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9.9 Tamper Detection

If the Tamper Channel n Action (TAMPCTRL.INnACT) is set to WAKE or CAPTURE and the Active Layer Protection is enabled for this channel (TAMPCTRLB.ALSIn = 1), no tampers are detected on this channel n.

Workaround

Clear the TAMPCTRLB.ALSIn bits for the channels configured in WAKE or CAPTURE modes.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9.10 Tamper Detection

False tamper detections may occur when configuring the RTC INn and OUTn pins.

Workaround

First configure the different RTC registers, and then select the RTC INn and OUTn peripheral functions on the PORT peripheral (PMUX registers).

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9.11 General Purpose Registers

General Purpose Registers n (GPn) are reset on tamper detection even if GPTRST = 0.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10 Serial Communication Interface Inter-Integrated Circuit (SERCOM I^{2}C)

2.10.1 High-Speed Mode

When configured in HS or Fast-Mode Plus, SDA and SCL fall times are shorter than I^{2}C specification requirement and can lead to reflection.

Workaround

When reflection is observed, a 100 ohm serial resistor can be added on the impacted line.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.2 Repeated Start

When Quick command is enabled (CTRLB.QCEN = 1), the software can issue a Repeated Start by either writing the CTRLB.CMD or ADDR.ADDR bit fields. If in these conditions, SCL Stretch Mode is CTRLA.SCLSM = 1, a bus error will be generated.

Workaround
Use Quick Command mode (CTRLB.QCEN = 1) only if SCL Stretch mode is CTRLA.SCLSM = 0.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.3 Repeated Start

For Master Write operations (excluding High-Speed mode), in 10-bit addressing mode, writing CTRLB.CMD = 0x1 does not issue correctly a Repeated Start command.

Workaround
Write the same 10-bit address with the same direction bit to the ADDR.ADDR register to generate properly a Repeated Start.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.4 Repeated Start

For High-Speed Master Read operations, sending a NACK (CTRLB.CMD = 0x2) forces a STOP to be issued making repeated start not possible in that mode.

Workaround
None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.5 Repeated Start

For High-Speed Master Write operations, writing CTRLB.CMD = 0x1 issues a STOP command instead of a Repeated Start making repeated start not possible in that mode.

Workaround
None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.6 Slave Mode with DMA

In I^2C Slave Transmitter mode, at the reception of a NACK, if there is still data to be sent in the DMA buffer, the DMA will push a data to the DATA register. Because a NACK was received, the transfer on the I^2C bus will not occur causing the loss of this data.

Workaround
Configure the DMA transfer size to the number of data to be received by the I^2C master. DMA cannot be used if the number of data to be received by the master is not known.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.7 Slave Mode 10-bit

I^2C slave 10-bit addressing mode is not functional.

Workaround
None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.8 Status Flags

In Slave mode, the BUSERR, COLL, LOWTOUT, SEXTTOUT and LENERR STATUS register bits are not automatically cleared when INTFLAG.AMATCH is cleared.

Workaround
Clear the STATUS register bits, BUSERR, COLL, LOWTOUT, SEXTTOUT and LENERR, by writing these STATUS bits to '1' when INTFLAG.AMATCH is cleared.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.9 Status Flags

The STATUS.CLKHOLD bit in master and slave modes can be written whereas it is a read-only status bit.

Workaround

Do not clear the STATUS.CLKHOLD bit to preserve the current clock hold state.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.10 Status Flags

When an unexpected STOP occurs on the I^2C bus, the STATUS.BUSERR and INTFLAG.ERROR bits are set, but may not wake the system from Sleep mode. An unexpected START will not produce this issue.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.11 Serial Communication Serial Peripheral Interface (SERCOM SPI)

2.11.1 Data Preload

In SPI Slave mode with Slave Data Preload Enabled (CTRLB.PLOADEN = 1), the slave transmitter may discard some data if the master cannot keep the Slave Select pin low until the end of transmission.

Workaround

In SPI Slave mode, the Slave Select (SS) pin must be kept low by the master until the end of the transmission if the Slave Data Preload feature is used (CTRLB.PLOADEN = 1).

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.11.2 Hardware Slave Select Control

When Hardware Slave Select Control is enabled (CTRLB.MSSEN = 1), the Slave Select (SS) pin goes high after each byte transfer even if a new data is ready to be sent.

Workaround

Set CTRLB.MSSEN = 0 and handle the Slave Select (SS) pin by software.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.11.3 Slave Data Preload

Preloading a new SPI data (CTRLB.PLOADEN = 1) before going into Standby Sleep mode, may lead to extra power consumption.

Workaround
None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.11.4 Wake-up Interrupt

The Data Register Empty (DRE) wake-up interrupt is not de-asserted when the register interrupt is cleared (INTFLAG.DRE = 0).

The issue occurs if the DRE interrupt is enabled (INTSET.DRE = 1) when the device enters in Standby Sleep mode.

Workaround
Write DATA register before going back to Standby mode.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.12 Serial Communication Interface USART (SERCOM USART)

2.12.1 Inverted Bits

The TXINV and RXINV bits in the CTRLA register have inverted functionality.

Workaround
In software, interpret the TXINV bit as a functionality of RXINV, and conversely, interpret the RXINV bit as a functionality of TXINV.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.12.2 ISO7816 Mode

When the SERCOM USART is in ISO7816 mode, the SERCOM bus clock continues to run in Standby Sleep mode causing extra power consumption.

Workaround

Disable the USART before entering Standby Sleep mode.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.12.3 Debug Mode

In USART operating mode, if DBGCTRL.DBGSTOP = 1, data transmission is not halted when entering Debug mode.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.12.4 Collision Detection

In USART operating mode with Collision Detection enabled (CTRLB.COLDEN = 1), the SERCOM will not abort the current transfer as expected if a collision is detected and if the SERCOM APB clock is lower than the SERCOM generic clock.

Workaround

The SERCOM APB clock must always be higher than the SERCOM generic clock to support collision detection.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.12.5 Wakeup

The USART does not wake up the device on Error Interrupt (INTFLAG.ERROR = 1).

Workaround
Configure the USART to wake up the device on the RX Complete Interrupt (INTENSET.RXC = 1) to check the PERR/FERR status (STATUS.PERR = 1 or STATUS.FERR = 1).

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.12.6 Overconsumption in Standby Mode

When SERCOM USART CTRLA.RUNSTDBY = 0 and the Receiver is disabled (CTRLB.RXEN = 0), the clock request to the GCLK generator feeding the SERCOM will stay asserted during Standby mode, leading to unexpected overconsumption.

Workaround
Configure CTRLA.RXPO and CTRLA.TXPO to use the same SERCOM PAD for RX and TX, or add an external pull-up on the RX pin.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.12.7 Wake-up Interrupt

The Data Register Empty (DRE) wake-up interrupt is not de-asserted when the register interrupt is cleared (INTFLAG.DRE = 0).

The issue occurs if the DRE interrupt is enabled (INTSET.DRE = 1) when the device enters in Standby Sleep mode.

Workaround
Write DATA register before going back to Standby mode.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.13 Timer Counter (TC)

2.13.1 Flags Synchronization

When clearing the STATUS.PERBUFV/STATUS.CCBUFVx flags, the SYNCBUSY.PER/SYNCBUSY.CCx flags are released before the PERBUF/CCBUFx registers are restored to their expected value.

Workaround
Successively, clear the STATUS.PERBUFV/STATUS.CCBUFVx flags twice to ensure that the PERBUF/CCBUFx registers value is properly restored before updating it.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.13.2 Capture Mode / Over consumption

If the Time Counter x (TCx) is in Capture mode (TC.CTRLA.CAPTENx=1) and TC.CTRLA.RUNSTBY=0, the clock source driving GCLK_TCx can be kept running in Standby mode causing extra power consumption.

Workaround
Disable the Time Counter x (TCx) (TC.CTRLA.ENABLE=0) which has a channel configured in Capture mode before going to Standby mode.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.13.3 Retrigger

If a Retrigger event (EVCTRL.EVACTn = 0x1, RETRIGGER) occurs at the Channel Compare Match [n] time, the next Waveform Output [n] is corrupted.

Workaround
Use two channels to store their two successive (n and n+1) CC register values and combine their related waveform outputs to make signal redundancy.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.14 True Random Number Generator (TRNG)

2.14.1 Over consumption

When TRNG is disabled, some internal logic could continue to operate causing an over consumption.

Workaround
Disable the TRNG module twice:

- CTRLA.ENABLE = 0;

- CTRLA.ENABLE = 0;

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.15 Supply Controller (SUPC)

2.15.1 Buck Converter Mode

Buck Converter mode is not supported when using FDPLL96M. As a result, the data provided in Tables 46-8 and 47-2 “Active Current Consumption for Buck converter mode with FDPLL96M at Performance Level 2 (PL2) setting” is not valid and must be disregarded.

Workaround
Use the LDO Regulator mode when using FDPLL96M.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.16 OSC32KCTRL

2.16.1 External 32.768 kHz Crystal Oscillator

External 32.768 kHz crystal oscillator operation is not supported over the full temperature range of -40°C to +125°C.

Workaround
Limit external 32.768 kHz crystal oscillator operation temperature range from 0°C to 125°C with a crystal ESR <70 kΩ.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.16.2 1024 Hz Clock Output

When the XOSC32K is configured for 1024 Hz clock output and is used to clock the Watchdog (OSCULP32K.ULP32KSW = 1) or the RTC (RTCCTRL.RTCSEL = 4), the 1024 Hz clock can generate spikes in Standby Low-Power mode if the XOSC32K is not always ON, leading to incorrect RTC/WDT counting.

Workaround
Set XOSC32K.RUNSTBY = 1 and clear XOSC32K.ONDEMAND = 0 to force the XOSC32K to be always ON in Standby Low-Power mode.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.16.3 Clock Failure Detection

Disabling the Clock Failure Detector (CFDCTRL.CFDEN = 0) and re-enabling it (CFDCTRL.CFDEN = 1) when the XOSC32K is enabled (XOSC32K.ENABLE = 1) can lead to a false Clock Failure Detection.

Workaround
Re-enable the Clock Failure Detector as follows:

1. Disable the XOSC32K (XOSC32K.ENABLE = 0).
2. Disable the Clock Failure Detector (CFDCTRL.CFDEN = 0).
3. Re-enable the Clock Failure Detector (CFDCTRL.CFDEN = 1).
4. Re-enable the XOSC32K (XOSC32K.ENABLE = 1).

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.16.4 XOSC32K Ready Bit

The XOSC32K Read bit of the STATUS register (STATUS.XOSC32KRDY) is not cleared when disabling the XOSC32K (XOSC32K.ENABLE = 0) at the same time as the Crystal Oscillator Enable bit (XOSC32K.XTALEN = 0).

Workaround
Disable the XOSC32K as follows:

1. Disable the XOSC32K (XOSC32K.ENABLE = 0).
2. Disable the Crystal Oscillator (XOSC32K.XTALEN = 0).

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.17 Boot ROM

2.17.1 GCM API

The GCM API function crya_gf_mult128_t does not save and restore the core register r8 on return, thereby violating the Procedure Call Standard for the ARM® Architecture (AAPCS).

Workaround

The ARM core register r8 must be saved before calling the crya_gf_mult128_t function and must be restored when returning from it.

Affected Silicon Revisions

Device Family	B						
SAM L10							
SAM L11	X						

2.18 Event System (EVSYS)

2.18.1 Synchronous and Resynchronized Modes

In synchronous or resynchronized modes, generating a software event can generate a spurious overrun interrupt.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.18.2 Synchronous Mode

In Synchronous mode, spurious overrun interrupts can be generated when the generic clock for a channel is always ON (CHANNEL.ONDEMAND = 0).

Workaround

Set Generic Clock on Demand feature by setting CHANNEL.ONDEMAND = 1.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.19 Oscillator Controller (OSCCTRL)

2.19.1 Clock Failure Detection

When the XOSC Clock Failure Detector is enabled (XOSCCTRL.CFDEN = 1) and a failure is detected (STATUS.XOSCFAIL = 1), the XOSC Ready bit is not cleared (STATUS.XOSCRDY = 1).

Workaround

STATUS.XOSCFAIL must always be checked before STATUS.XOSCRDY, and STATUS.XOSCRDY must always be ignored when STATUS.XOSCFAIL = 1.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.19.2 Clock Failure Detection

Disabling the Clock Failure Detector (XOSCCTRL.CFDEN = 0) and re-enabling it (XOSCCTRL.CFDEN = 1) when the XOSC is enabled (XOSCCTRL.ENABLE = 1) can lead to a false Clock Failure Detection.

Workaround

Re-enable the Clock Failure Detector as follows:

1. Disable the XOSC (XOSCCTRL.ENABLE = 0).
2. Disable the Clock Failure Detector (XOSCCTRL.CFDEN = 0).
3. Re-enable the Clock Failure Detector (XOSCCTRL.CFDEN = 1).
4. Re-enable the XOSC (XOSCCTRL.ENABLE = 1).

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.19.3 XOSC Ready Bit

The XOSC Read bit of the STATUS register (STATUS.XOSCRDY) is not cleared when disabling the XOSC bit (XOSCCTRL.ENABLE = 0) at the same time as the Crystal Oscillator Enable bit (XOSCCTRL.XTALEN = 0) .

Workaround

Disable the XOSC Ready bit as follows:

1. Disable the XOSC (XOSCCTRL.ENABLE = 0).
2. Disable the Crystal Oscillator (XOSCCTRL.XTALEN = 0).

Affected Silicon Revisions

Device Family	B						
SAM L10	X						

.....continued

Device Family	B						
SAM L11	X						

2.20 PORT I/O Controller (PORT)

2.20.1 IOBUS

Concurrent accesses on the PORT peripheral registers between the ARM APB and the ARM CPU IOBUS are not supported.

Workaround

Use exclusively the ARM APB or the ARM CPU IOBUS to access PORT peripheral registers.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.21 Trust Ram (TRAM)

2.21.1 PAC Protection

Security RAM n registers (RAMn) are not PAC Write-Protected.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001513F):

Note: Corrections in tables, registers, and texts are shown in **bold.** Where possible, the original bold text formatting has been removed for clarity.

- Table 46-8 Active Current Consumption was updated:

Table 3-1. Active Current Consumption

Mode	Conditions	Regulator	PL	CPU Clock	Vcc	Ta	Typ.	Max.	Units
ACTIVE	COREMARK/ FIBONACCI	LDO	PL0	DFLLULP at 8MHz	1.8V	Max at 85°C Typ at 25°	64.1	82	µA/Mhz
					3.3V		64.4	84	
				OSC 8MHz	1.8V		66.6	81	
					3.3V		70.3	83	
				OSC 4MHz	1.8V		74.1	102	
					3.3V		77.8	106	
			PL2	FDPLL96M at 32MHz	1.8V		82.0	89	
					3.3V		82.5	89	
				DFLLULP at 32MHz	1.8V		75.8	99	
					3.3V		75.8	96	
		BUCK	PL0	**DFLLULP at 4.88MHz**	1.8V		**44**	**60**	
					3.3V		**29.9**	**41**	
				OSC 8MHz	1.8V		43.8	53	
					3.3V		32.1	39	
				OSC 4MHz	1.8V		50.3	68	
					3.3V		38.9	52	
			PL2	FDPLL96M at 32MHz	1.8V	Max at 85°C Typ at 25°	59.9	66	
					3.3V		35.3	39	
				DFLLULP at 26.78MHz	1.8V		**55.8**	**70**	
					3.3V		**33.7**	**42**	
	WHILE1	LDO	PL0	DFLLULP at 8MHz	1.8V		44.3	61	
					3.3V		44.4	62	
				OSC 8MHz	1.8V		47.6	60	
					3.3V		50.1	63	
				OSC 4MHz	1.8V		54.6	83	
					3.3V		57.7	86	
			PL2	FDPLL96M at 32MHz	1.8V		56.9	61	
					3.3V		57.2	62	
				DFLLULP at 32MHz	1.8V		50.8	66	
					3.3V		51.0	64	

.....continued

Mode	Conditions	Regulator	PL	CPU Clock	Vcc	Ta	Typ.	Max.	Units
ACTIVE	WHILE1	BUCK	PL0	**DFLLULP at 4.88MHz**	1.8V	Max at 85°C Typ at 25°	**32.4**	**49**	µA/Mhz
					3.3V		**22.8**	**34**	
				OSC 8MHz	1.8V		32.2	41	
					3.3V		25.3	32	
				OSC 4MHz	1.8V		38.4	57	
					3.3V		31.9	45	
			PL2	FDPLL96M at 32MHz	1.8V		41.5	46	
					3.3V		24.6	28	
				DFLLULP at 26.78MHz	1.8V		**38.3**	**48**	
					3.3V		**23.1**	**29**	
IDLE	-	LDO	PL0	DFLLULP at 8MHz	1.8V		16.0	32	
					3.3V		16.2	33	
				OSC 8MHz	1.8V		19.8	33	
					3.3V		22.0	36	
				OSC 4MHz	1.8V		26.2	55	
					3.3V		29.2	59	
			PL2	FDPLL96M at 32MHz	1.8V		20.3	25	
					3.3V		20.4	26	
				DFLLULP at 32MHz	1.8V		14.3	19	
					3.3V		14.4	19	
		BUCK	PL0	**DFLLULP at 4.88MHz**	1.8V		**15.1**	**32**	
					3.3V		**12.3**	**24**	
				OSC 8MHz	1.8V		15.5	24	
					3.3V		15.2	21	
				OSC 4MHz	1.8V		21.3	39	
					3.3V		21.6	35	
			PL2	FDPLL96M at 32MHz	1.8V		14.9	19	
					3.3V		9.1	12	
				DFLLULP at 26.7MHz	1.8V		**11.2**	**16**	
					3.3V		**7.2**	**10**	

- Table 46-54 is a new table which was added to the SAM L10/L11 Data Sheet.

Table 3-2. Digital Frequency Locked Loop Characteristics (Buck Converter mode only)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
FIN	Input Clock Frequency		32		33	KHz
FOUT	Output Clock Frequency	PL0	-	-	4.88	MHz
		PL2	-	-	26.78	
FOUT drift	Output Clock Frequency drift (2)	PL0, FIN = 32KHz, FOUT = 4.88MHz	-16.3		38.9	%
		PL2, FIN = 32KHz, FOUT = 26.78MHz	-8.7		16.3	

.....continued

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Jp	Period Jitter(2) (cycle to cycle jitter)	PL0, FIN = 32KHz, FOUT = 4.88MHz	-7.8	-	8.1	%
		PL2, FIN = 32KHz, FOUT = 26.78MHz	-5.0	-	4.6	
tLOCK	Lock Time	After startup, time to get lock signal FIN = 32KHz, FOUT = 4.88MHz, PL0 Binary Search mode enabled	-	362	-	µs
		After startup, time to get lock signal FIN = 32KHz, FOUT = 26.78MHz, PL2 Binary Search mode enabled	-	362	-	µs
Duty	Duty Cycle (1)		40	50	60	%

Note:

1. These characteristics are only applicable in Buck Converter mode.

- Table 47-2 was updated to reflect a new data:

Table 3-3. Active Current Consumption

Mode	Conditions	Regulator	PL	CPU Clock	Vcc	Ta	Typ.	Max.	Units
ACTIVE	COREMARK / FIBONACCI	LDO	PL0	DFLLUP at 8 MHz	1.8V	Max at 125°C Typ at 25°C	64.1	129	uA/MHz
					3.3V		64.4	131	
				OSC 8 MHz	1.8V		66.6	130	
					3.3V		70.3	132	
				OSC 4 MHz	1.8V		74.1	203	
					3.3V		77.8	206	
			PL2	FDPLL96 at 32 MHz	1.8V		82.0	98	
					3.3V		82.5	99	
				DFLLULP at 32 MHz	1.8V		75.8	109	
					3.3V		75.8	107	
		BUCK	PL0	**DFLLUP at 4.88 MHz**	1.8V		**44**	**103**	
					3.3V		**29.9**	**69**	
				OSC 8 MHz	1.8V		43.8	84	
					3.3V		32.1	58	
				OSC 4 MHz	1.8V		50.3	131	
					3.3V		38.9	92	
			PL2	FDPLL96 at 32 MHz	1.8V		59.9	70	
					3.3V		35.3	43	
				DFLLULP at 26.78 MHz	1.8V		**55.8**	**80**	
					3.3V		**33.7**	**48**	
	WHILE1	LDO	PL0	DFLLUP at 8 MHz	1.8V		44.3	110	
					3.3V		44.4	111	
				OSC 8 MHz	1.8V		47.6	111	
					3.3V		50.1	113	
				OSC 4 MHz	1.8V		54.6	184	
					3.3V		57.7	187	
			PL2	FDPLL96 at 32 MHz	1.8V		56.9	79	
					3.3V		57.2	80	
				DFLLULP at 32 MHz	1.8V		50.8	72	
					3.3V		51.0	72	

.....continued

Mode	Conditions	Regulator	PL	CPU Clock	Vcc	Ta	Typ.	Max.	Units
ACTIVE	WHILE1	BUCK	PL0	**DFLLUP at 4.88 MHz**	1.8V	Max at 125°C Typ at 25°C	**32.4**	**90**	uA/MHz
					3.3V		**22.8**	**62**	
				OSC 8 MHz	1.8V		32.2	73	
					3.3V		25.3	51	
				OSC 4 MHz	1.8V		38.4	121	
					3.3V		31.9	86	
			PL2	FDPLL96 at 32 MHz	1.8V		41.5	55	
					3.3V		24.6	34	
				DFLLULP at 26.78 MHz	1.8V		**38.3**	**58**	
					3.3V		**23.1**	**36**	
IDLE	-	LDO	PL0	DFLLUP at 8 MHz	1.8V		16.0	81	
					3.3V		16.2	82	
				OSC 8 MHz	1.8V		19.8	82	
					3.3V		22.0	85	
				OSC 4 MHz	1.8V		26.2	152	
					3.3V		29.2	157	
			PL2	FDPLL96 at 32 MHz	1.8V		20.3	54	
					3.3V		20.4	54	
				DFLLULP at 32 MHz	1.8V		14.3	32	
					3.3V		14.4	33	
		BUCK	PL0	**DFLLUP at 4.88 MHz**	1.8V		**15.1**	**68**	
					3.3V		**12.3**	**48**	
				OSC 8 MHz	1.8V		15.5	55	
					3.3V		15.2	40	
				OSC 4 MHz	1.8V		21.3	100	
					3.3V		21.6	73	
			PL2	FDPLL96 at 32 MHz	1.8V		14.9	30	
					3.3V		9.1	19	
				DFLLULP at 26.78 MHz	1.8V		**11.2**	**26**	
					3.3V		**7.2**	**17**	

4. Revision History

Revision D - 01/2021
This revision contains numerous typographical updates, and formatting updates.

The following errata were updated with new verbiage:

- DMAC: 2.4.1 Concurrent Channels Trigger
- EIC: 2.5.1 PAC Protection
- OPAMP: 2.8.1 Reference Buffer
- SERCOM I2C: 2.10.8 Status Flags
- SERCOM I2C: 2.10.9 Status Flags
- SERCOM SPI: 2.11.1 Data Preload
- SERCOM USART: 2.12.5 Wakeup

The following errata were added in this revision:

- ADC: 2.1.2 Offset Correction
- Device: 2.3.2 Standby Entry
- RTC: 2.9.9 Tamper Detection
- RTC: 2.9.10 Tamper Detection
- RTC: 2.9.11 General Purpose Registers
- SERCOM I2C: 2.10.10 Status Flags
- SERCOM SPI: 2.11.2 Hardware Slave Select Control
- SERCOM SPI: 2.11.3 Slave Data Preload
- SERCOM SPI: 2.11.4 Wakeup Interrupt
- SERCOM USART: 2.12.6 Overconsumption in Standby Mode
- SERCOM USART: 2.12.7 Wakeup Interrupt
- TC: 2.13.3 Retrigger
- OSC32KCTRL: 2.16.2 1024 Hz Clock Output
- OSC32KCTRL: 2.16.3 Clock Failure Detection
- OSC32KCTRL: 2.16.4 XOSC32K Ready Bit
- EVSYS: 2.18.1 Synchronous and Resynchronized Modes
- EVSYS: 2.18.2 Synchronous Mode
- OSCCTRL: 2.19.1 Clock Failure Detection
- OSCCTRL: 2.19.2 Clock Failure Detection
- OSCCTRL: 2.19.3 XOSC Ready Bit
- PORT: 2.20.1 IOBUS
- TRAM: 2.21.1 PAC Protection

Revision C - 05/2019
The following new errata were added:

- RTC:
  - 2.9.5 Prescaler
  - 2.9.6 Active Layer Protection
  - 2.9.7 Tamper Detection Timestamp
  - 2.9.8 Tamper Detection Timestamp
- SERCOM USART:
  - 2.12.5 Wakeup

Revision B - 02/2019

The following new errata were added:

- RTC: 2.9.4 Tamper detection Timestamp
- SUPC: 2.15.1 Buck Converter Mode
- OSC32KCTRL: 2.16.1 External 32.768kHz Crystal Oscillator
- Boot ROM: 2.17.1 GMC API

The following errata is updated:

- ADC: 2.1.1 Reference Buffer Offset Compensation

The following Data Sheet clarifications were added:

- Updates to Electrical Specifications Tables:
  - Table 46-8
  - Table 46-54
  - Table 47-2

Revision A - 5/2018

This is the initial release of this document.

The Microchip Web Site

Microchip provides online support via our web site at www.microchip.com/. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support –** Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support –** Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip –** Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Customer Change Notification Service

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com/. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: www.microchip.com/support

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Legal Notice

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks

The Microchip name and logo, the Microchip logo, AnyRate, AVR, AVR logo, AVR Freaks, BeaconThings, BitCloud, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, Heldo, JukeBlox, KeeLoq, KeeLoq logo, Kleer, LANCheck, LINK MD, maXStylus, maXTouch, MediaLB, megaAVR, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, Prochip Designer, QTouch, RightTouch, SAM-BA, SpyNIC, SST, SST Logo, SuperFlash, tinyAVR, UNI/O, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, EtherSynch, Hyper Speed Control, HyperLight Load, IntelliMOS, mTouch, Precision Edge, and Quiet-Wire are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BodyCom, chipKIT, chipKIT logo, CodeGuard, CryptoAuthentication, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, Inter-Chip Connectivity, JitterBlocker, KleerNet, KleerNet logo, Mindi, MiWi, motorBench, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PureSilicon, QMatrix, RightTouch logo, REAL ICE, Ripple Blocker, SAM-ICE, Serial Quad I/O, SMART-I.S., SQI, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2017, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

ISBN: 978-1-5224-7430-2

Quality Management System Certified by DNV

ISO/TS 16949

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
Corporate Office	**Asia Pacific Office**	**China - Xiamen**	**Austria - Wels**
2355 West Chandler Blvd.	Suites 3707-14, 37th Floor	Tel: 86-592-2388138	Tel: 43-7242-2244-39
Chandler, AZ 85224-6199	Tower 6, The Gateway	Fax: 86-592-2388130	Fax: 43-7242-2244-393
Tel: 480-792-7200	Harbour City, Kowloon	**China - Zhuhai**	**Denmark - Copenhagen**
Fax: 480-792-7277	**Hong Kong**	Tel: 86-756-3210040	Tel: 45-4450-2828
Technical Support:	Tel: 852-2943-5100	Fax: 86-756-3210049	Fax: 45-4485-2829
http://www.microchip.com/	Fax: 852-2401-3431	**India - Bangalore**	**Finland - Espoo**
support	**Australia - Sydney**	Tel: 91-80-3090-4444	Tel: 358-9-4520-820
Web Address:	Tel: 61-2-9868-6733	Fax: 91-80-3090-4123	**France - Paris**
www.microchip.com	Fax: 61-2-9868-6755	**India - New Delhi**	Tel: 33-1-69-53-63-20
Atlanta	**China - Beijing**	Tel: 91-11-4160-8631	Fax: 33-1-69-30-90-79
Duluth, GA	Tel: 86-10-8569-7000	Fax: 91-11-4160-8632	**France - Saint Cloud**
Tel: 678-957-9614	Fax: 86-10-8528-2104	**India - Pune**	Tel: 33-1-30-60-70-00
Fax: 678-957-1455	**China - Chengdu**	Tel: 91-20-3019-1500	**Germany - Garching**
Austin, TX	Tel: 86-28-8665-5511	**Japan - Osaka**	Tel: 49-8931-9700
Tel: 512-257-3370	Fax: 86-28-8665-7889	Tel: 81-6-6152-7160	**Germany - Haan**
Boston	**China - Chongqing**	Fax: 81-6-6152-9310	Tel: 49-2129-3766400
Westborough, MA	Tel: 86-23-8980-9588	**Japan - Tokyo**	**Germany - Heilbronn**
Tel: 774-760-0087	Fax: 86-23-8980-9500	Tel: 81-3-6880- 3770	Tel: 49-7131-67-3636
Fax: 774-760-0088	**China - Dongguan**	Fax: 81-3-6880-3771	**Germany - Karlsruhe**
Chicago	Tel: 86-769-8702-9880	**Korea - Daegu**	Tel: 49-721-625370
Itasca, IL	**China - Guangzhou**	Tel: 82-53-744-4301	**Germany - Munich**
Tel: 630-285-0071	Tel: 86-20-8755-8029	Fax: 82-53-744-4302	Tel: 49-89-627-144-0
Fax: 630-285-0075	**China - Hangzhou**	**Korea - Seoul**	Fax: 49-89-627-144-44
Dallas	Tel: 86-571-8792-8115	Tel: 82-2-554-7200	**Germany - Rosenheim**
Addison, TX	Fax: 86-571-8792-8116	Fax: 82-2-558-5932 or	Tel: 49-8031-354-560
Tel: 972-818-7423	**China - Hong Kong SAR**	82-2-558-5934	**Israel - Ra'anana**
Fax: 972-818-2924	Tel: 852-2943-5100	**Malaysia - Kuala Lumpur**	Tel: 972-9-744-7705
Detroit	Fax: 852-2401-3431	Tel: 60-3-6201-9857	**Italy - Milan**
Novi, MI	**China - Nanjing**	Fax: 60-3-6201-9859	Tel: 39-0331-742611
Tel: 248-848-4000	Tel: 86-25-8473-2460	**Malaysia - Penang**	Fax: 39-0331-466781
Houston, TX	Fax: 86-25-8473-2470	Tel: 60-4-227-8870	**Italy - Padova**
Tel: 281-894-5983	**China - Qingdao**	Fax: 60-4-227-4068	Tel: 39-049-7625286
Indianapolis	Tel: 86-532-8502-7355	**Philippines - Manila**	**Netherlands - Drunen**
Noblesville, IN	Fax: 86-532-8502-7205	Tel: 63-2-634-9065	Tel: 31-416-690399
Tel: 317-773-8323	**China - Shanghai**	Fax: 63-2-634-9069	Fax: 31-416-690340
Fax: 317-773-5453	Tel: 86-21-3326-8000	**Singapore**	**Norway - Trondheim**
Tel: 317-536-2380	Fax: 86-21-3326-8021	Tel: 65-6334-8870	Tel: 47-7289-7561
Los Angeles	**China - Shenyang**	Fax: 65-6334-8850	**Poland - Warsaw**
Mission Viejo, CA	Tel: 86-24-2334-2829	**Taiwan - Hsin Chu**	Tel: 48-22-3325737
Tel: 949-462-9523	Fax: 86-24-2334-2393	Tel: 886-3-5778-366	**Romania - Bucharest**
Fax: 949-462-9608	**China - Shenzhen**	Fax: 886-3-5770-955	Tel: 40-21-407-87-50
Tel: 951-273-7800	Tel: 86-755-8864-2200	**Taiwan - Kaohsiung**	**Spain - Madrid**
Raleigh, NC	Fax: 86-755-8203-1760	Tel: 886-7-213-7830	Tel: 34-91-708-08-90
Tel: 919-844-7510	**China - Wuhan**	**Taiwan - Taipei**	Fax: 34-91-708-08-91
New York, NY	Tel: 86-27-5980-5300	Tel: 886-2-2508-8600	**Sweden - Gothenberg**
Tel: 631-435-6000	Fax: 86-27-5980-5118	Fax: 886-2-2508-0102	Tel: 46-31-704-60-40
San Jose, CA	**China - Xian**	**Thailand - Bangkok**	**Sweden - Stockholm**
Tel: 408-735-9110	Tel: 86-29-8833-7252	Tel: 66-2-694-1351	Tel: 46-8-5090-4654
Tel: 408-436-4270	Fax: 86-29-8833-7256	Fax: 66-2-694-1350	**UK - Wokingham**
Canada - Toronto			Tel: 44-118-921-5800
Tel: 905-695-1980			Fax: 44-118-921-5820
Fax: 905-695-2078			