Product Change Notification / RMES-20NCGX846

Date:

20-Oct-2020

Product Category:

Crypto Authentication

PCN Type:

Manufacturing Change

Notification Subject:

Memo # ML102020003S Information Notice: Introduction of new ATECC608B device family available in 3L CONTACT, 8L UDFN and 8L SOIC packages as replacement to an existing ATECC508A and ATECC608A device families that are currently available in DICE, WAFER, 3L CONTACT, 8L UDFN and 8L SOIC packages.

Affected CPNs:

RMES-20NCGX846_Affected_CPN_10202020.pdf
RMES-20NCGX846_Affected_CPN_10202020.csv

Notification Text:

PCN Status: Information notification

PCN Type: Manufacturing Change

Microchip Parts Affected: Please open one of the icons found in the Affected CPNs section above.

NOTE: For your convenience Microchip includes identical files in two formats (.pdf and .xls)

Description of Change: Introduction of new ATECC608B device family available in 3L CONTACT, 8L UDFN and 8L SOIC packages as replacement to an existing ATECC508A and ATECC608A device families that are currently available in DICE, WAFER, 3L CONTACT, 8L UDFN and 8L SOIC packages.

Microchip has setup the ATECC508A and ATECC608A as “not recommended for new designs” on

microchip.com. The newly launched ATECC608B is the recommended solution as it provides a few improvements.

Pre Change:
Device families ATECC508A and ATECC608A available in DICE, WAFER, 3L CONTACT, 8L UDFN and 8L SOIC packages

Post Change:
Device families ATECC608B available in 3L CONTACT, 8L UDFN and 8L SOIC packages

Pre and Post Change Summary:

	Pre Change	Post Change
Affected Device Families	ATECC508A and ATECC608A	ATECC608B
Package type	DICE, WAFER, 3L CONTACT,8L UDFN and 8L SOIC	3L CONTACT,8L UDFN and 8L SOIC
Device Comparison of ATECC508A and ATECC608B	Refer to Application Notes AN3539	
Device Comparison of ATECC608A and ATECC608B	Refer to Application Notes AN2237	

Note: Production support will continue for all ATECC508A and ATECC608A for existing customers

Impacts to Data Sheet: None. Refer to this link for ATECC608B datasheet.

Change Impact: None

Reason for Change: The ATECC608B provides its users with a chance to implement some enhanced functional security features to improve their overall system security and performance.

Also, the new ATECC608B fixes a bug in the I2C performances present on both the ATECC508A and ATECC608A occurring at low frequency when multiple devices are on the bus. It will improve physical protection against physical attacks.

Change Implementation Status: In Progress

New products availability date: *October 19, 2020 (date code: 2043) – For 3L CONTACT and 8L UDFN package
*October 31, 2020 (date code: 2044) – For 8L SOIC package

Note: See attachments section for the list of product availability per catalog part number in Affected_CPN list.

Time Table Summary:

	October 2020				
Workweek	40	41	42	43	44
Final PCN Issue Date				X	
Qual Report Availability				X	
* Earliest date the new products availability				See products availability date above and identified in affected CPN list	

Method to Identify Change: Traceability code

Qualification Report: Please open the attachments included with this PCN labeled as PCN_#_Qual_Report.

Revision History: October 20, 2020: Issued Information notification. Attached is the qualification report and added new products availability date.

The change described in this PCN does not alter Microchip's current regulatory compliance regarding the material content of the applicable products.

Attachments:

PCN_RMES-12QLUN125_Qual_Report.pdf
PCN_RMES-20NCGX846_Affected_CPN.pdf
PCN_RMES-20NCGX846_Affected_CPN.xlsx

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If you wish to change your PCN profile, including opt out, please go to the PCN home page select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.

QUALIFICATION REPORT SUMMARY

PCN #: RMES-12QLUN125

Date:
October 1, 2020

Introduction of new ATECC608B device family available in 3L CONTACT, 8L UDFN and 8L SOIC packages as replacement to an existing ATECC508A and ATECC608A device families that are currently available in DICE, WAFER, 3L CONTACT, 8L UDFN and 8L SOIC packages.

Purpose: **Introduction of new ATECC608B device family available in 3L CONTACT, 8L UDFN and 8L SOIC packages as replacement to an existing ATECC508A and ATECC608A device families that are currently available in DICE, WAFER, 3L CONTACT, 8L UDFN and 8L SOIC packages.**

Memo No.: **ML102020003S**

Test / Evaluation	Test Conditions / Parameters	Test Result
Temperature Characterization	• Wafer level characterization across temperature	All parameters within specification - **PASSED**

This is a summary document. A complete document is available under NDA. For more information, please contact your local Microchip sales office.

MICROCHIP

ATECC608B

CryptoAuthentication™ Device Summary Data Sheet

Features

- Cryptographic Co-Processor with Secure Hardware-Based Key Storage:
  - Protected storage for up to 16 keys, certificates or data
- Hardware Support for Asymmetric Sign, Verify, Key Agreement:
  - ECDSA: FIPS186-3 Elliptic Curve Digital Signature
  - ECDH: FIPS SP800-56A Elliptic Curve Diffie-Hellman
  - NIST Standard P256 Elliptic Curve Support
- Hardware Support for Symmetric Algorithms:
  - SHA-256 & HMAC Hash including off-chip context save/restore
  - AES-128: Encrypt/Decrypt, Galois Field Multiply for GCM
- Networking Key Management Support:
  - Turnkey PRF/HKDF calculation for TLS 1.2 & 1.3
  - Ephemeral key generation and key agreement in SRAM
  - Small message encryption with keys entirely protected
- Secure Boot Support:
  - Full ECDSA code signature validation, optional stored digest/signature
  - Optional communication key disablement prior to secure boot
  - Encryption/Authentication for messages to prevent on-board attacks
- Internal High-Quality NIST SP 800-90A/B/C Random Number Generator (RNG)
- Two High-Endurance Monotonic Counters
- Unique 72-Bit Serial Number
- Two Interface Options Available:
  - High-Speed Single Wire Interface with One GPIO Pin
  - 1 MHz Standard I^2C Interface
- 1.8V to 5.5V IO Levels, 2.0V to 5.5V Supply Voltage
- Two Temperature Ranges Available:
  - Standard Industrial Temperature Range: -40°C to +85°C
  - Extended Industrial Temperature Range: -40°C to +100°C
- <150 nA Sleep Current
- Packaging Options
  - 8-pad UDFN, 8-lead SOIC and 3-Lead Contact Package Options
  - Die-on-Tape and Reel and WLCSP for Qualified Customers (Contact Microchip Sales)

Applications

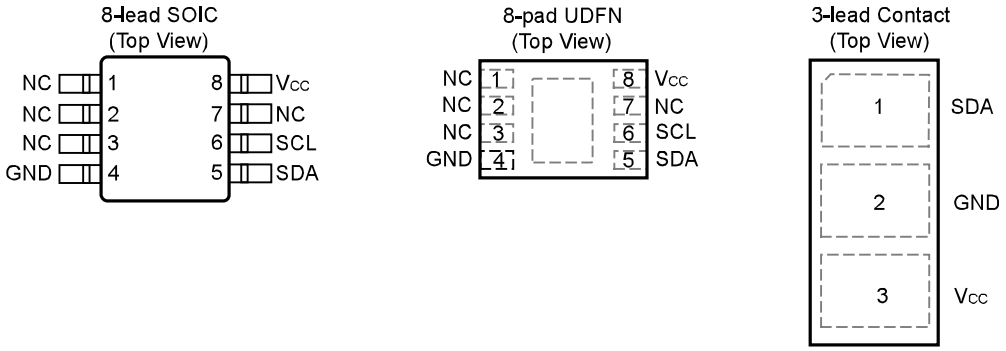
- IoT network endpoint key management & exchange
- Encryption for small messages and PII data
- Secure Boot and Protected Download
- Ecosystem Control, Anti-cloning

Pin Configuration and Pinouts

Table 1. Pin Configuration

Pin	Function I^2C Interface	Function SWI Interface
NC	No Connect	No Connect
GND	Ground	Ground
SDA	Serial Data	Serial Data
SCL	Serial Clock Input	GPIO
V_{CC}	Power Supply	Power Supply

Figure 1. Package Types



Note: The UDFN backside paddle is recommended to be connected to GND.

Table of Contents

1. Introduction

The ATECC608B is a member of the Microchip CryptoAuthentication™ family of high-security cryptographic devices, which combine world-class, hardware-based key storage with hardware cryptographic accelerators to implement various authentication and encryption protocols.

The ATECC608B provides security enhancements over that of the ATECC608A, while providing complete backwards compatibility. All configuration settings, commands, packages and functionality of the ATECC608A are still available in the ATECC608B, making migration from the ATECC608A a simple process. For new designs, it is recommended that customers start directly with the ATECC608B device. For designs that are being upgraded and currently use the ATECC508A or the ATECC608A, it is recommended that they move to the ATECC608B. For designs not planned to be upgraded, it is recommended that customers review their designs to see if they would benefit from the enhanced security of the ATECC608B. For assistance with migrating a design to the ATECC608B, see the Migrations References section.

For more information on compatibility with other Microchip CryptoAuthentication products, please see Section 3. Compatibility.

Migration References:

1. AN3539: Provides guidance on migrating from the ATECC508A to the ATECC608B
2. AN2237: Provides guidance on migrating from the ATECC608A to the ATECC608B

1.1 Applications

The ATECC608B has a flexible command set that allows use in many applications, including the following:

- **Network/IoT Node Endpoint Security**
  Manages node identity authentication and session key creation and management. Supports the entire ephemeral session key-generation flow for multiple protocols, including TLS 1.2 (and earlier) and TLS 1.3.
- **Secure Boot**
  Supports the MCU host by validating code digests and optionally enabling communication keys on success. Various configurations to offer enhanced performance are available.
- **Small Message Encryption**
  Contains a hardware AES engine to encrypt and/or decrypt small messages or data such as PII information. Supports the AES-ECB mode directly. Other modes can be implemented with the help of the host microcontroller. There is an additional GFM calculation function to support AES-GCM.
- **Key Generation for Software Download**
  Supports local protected key generation for downloaded images. Both broadcast of one image to many systems, each with the same decryption key, or point-to-point download of unique images per system are supported.
- **Ecosystem Control and Anti-Counterfeiting**
  Validates that a system or component is authentic and came from the OEM shown on the nameplate.

1.2 Device Features

The ATECC608B includes an EEPROM array which can be used for storage of up to 16 keys, certificates, miscellaneous read/write, read-only or secret data, consumption logging and security configurations. Access to the various sections of memory can be restricted in a variety of ways and then the configuration can be locked to prevent changes.

Access to the device is made through a standard I^2C Interface at speeds of up to 1 Mbps. The interface is compatible with standard Serial EEPROM I^2C interface specifications. The device also supports a Single-Wire Interface (SWI), which can reduce the number of GPIOs required on the system processor, and/or reduce the number of pins on connectors. If the Single-Wire Interface is enabled, the remaining pin is available for use as a GPIO, an authenticated output or tamper input.

Each ATECC608B ships with an ensured unique 72-bit serial number. Using the cryptographic protocols supported by the device, a host system or remote server can verify a signature of the serial number to prove that the serial

number is authentic and not a copy. Serial numbers are often stored in a standard Serial EEPROM; however, these can be easily copied with no way for the host to know if the serial number is authentic or if it is a clone.

The ATECC608B features a wide array of defense mechanisms specifically designed to prevent physical attacks on the device itself, or logical attacks on the data transmitted between the device and the system. Hardware restrictions on the ways in which keys are used or generated provide further defense against certain styles of attack.

1.3 Cryptographic Operation

The ATECC608B implements a complete asymmetric (public/private) key cryptographic signature solution based upon Elliptic Curve Cryptography and the ECDSA signature protocol. The device features hardware acceleration for the NIST standard P256 prime curve and supports the complete key life cycle from high quality private key generation, to ECDSA signature generation, ECDH key agreement and ECDSA public key signature verification.

The hardware accelerator can implement such asymmetric cryptographic operations from ten to one-thousand times faster than software running on standard microprocessors, without the usual high risk of key exposure that is endemic to standard microprocessors.

The ATECC608B also implements AES-128, SHA256 and multiple SHA derivatives such as HMAC(SHA), PRF (the key derivation function in TLS) and HKDF in hardware. Support is included for the Galois Field Multiply (aka Ghash) to facilitate GCM encryption/decryption/authentication.

The device is designed to securely store multiple private keys along with their associated public keys and certificates. The signature verification command can use any stored or an external ECC public key. Public keys stored within the device can be configured to require validation via a certificate chain to speed up subsequent device authentications.

Random private key generation is supported internally within the device to ensure that the private key can never be known outside of the device. The public key corresponding to a stored private key is always returned when the key is generated and it may optionally be computed at a later time.

The ATECC608B can generate high-quality random numbers using its internal random number generator. This sophisticated function includes runtime health testing designed to ensure that the values generated from the internal noise source contain sufficient entropy at the time of use. The random number generator is designed to meet the requirements documented in the NIST 800-90A, 800-90B and 800-90C documents.

These random numbers can be employed for any purpose, including as part of the device's cryptographic protocols. Because each random number is ensured to be essentially unique from all numbers ever generated on this or any other device, their inclusion in the protocol calculation ensures that replay attacks (i.e., re-transmitting a previously successful transaction) will always fail.

The ATECC608B also supports a standard hash-based challenge-response protocol to allow its use across a wide variety of additional applications. In its most basic instantiation, the system sends a challenge to the device, which combines that challenge with a secret key via the MAC command and then sends the response back to the system. The device uses a SHA-256 cryptographic hash algorithm to make that combination so that an observer on the bus cannot derive the value of the secret key. At the same time, the recipient can verify that the response is correct by performing the same calculation with a stored copy of the secret on the recipient's system. There are a wide variety of variations possible on this symmetric challenge/response theme.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Operating Temperature	-40°C to +100°C
Storage Temperature	-65°C to +150°C
Maximum Operating Voltage	6.0V
DC Output Current	5.0 mA
Voltage on any pin -0.5V to (V_{CC} + 0.5V)	-0.5V to (V_{CC} + 0.5V)
ESD Ratings:	
Human Body Model(HBM) ESD	>4kV
Charge Device Model(CDM) ESD	>1kV

Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2.2 Reliability

The ATECC608B is fabricated with Microchip's high reliability CMOS EEPROM manufacturing technology.

Table 2-1. EEPROM Reliability

Parameter	Min.	Typ.	Max.	Units
Write Endurance at +85°C (Each Byte)	400,000	—	—	Write Cycles
Data Retention at +55°C	10	—	—	Years
Data Retention at +35°C	30	50	—	Years
Read Endurance	Unlimited			Read Cycles

2.3 AC Parameters: All I/O Interfaces

Figure 2-1. AC Timing Diagram: All Interfaces

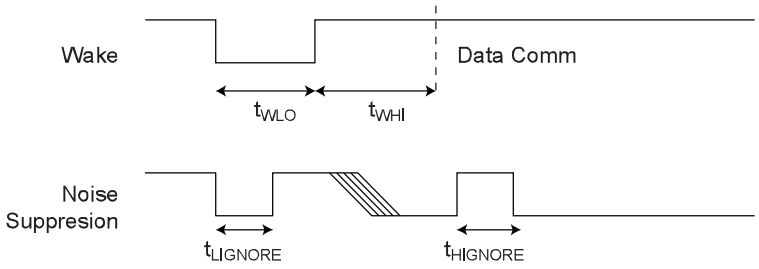


Table 2-2. AC Parameters: All I/O Interfaces

Parameter	Sym.	Direction	Min.	Typ.	Max.	Units	Conditions
Power-Up Delay(2)	t_{PU}	To Crypto Device	100	—	—	µs	Minimum time between V_{CC} > V_{CC} min prior to start of t_{WLO}.
Wake Low Duration	t_{WLO}	To Crypto Device	60	—	—	µs	
Wake High Delay to Data Comm	t_{WHI}	To Crypto Device	1500	—	—	µs	SDA should be stable high for this entire duration unless polling is implemented. SelfTest is not enabled at power-up.
Wake High Delay when SelfTest is Enabled	t_{WHIST}	To Crypto Device	20	—	—	ms	SDA should be stable high for this entire duration unless polling is implemented.
High-Side Glitch Filter at Active	$t_{HIGNORE\_A}$	To Crypto Device	45(1)	—	—	ns	Pulses shorter than this in width will be ignored by the device, regardless of its state when active.
Low-Side Glitch Filter at Active	$t_{LIGNORE\_A}$	To Crypto Device	45(1)	—	—	ns	Pulses shorter than this in width will be ignored by the device, regardless of its state when active.
Low-Side Glitch Filter at Sleep	$t_{LIGNORE\_S}$	To Crypto Device	15(1)	—	—	µs	Pulses shorter than this in width will be ignored by the device when in Sleep mode.
Watchdog Time-out	$t_{WATCHDOG}$	To Crypto Device	0.7	1.3	1.7	s	Time from wake until device is forced into Sleep mode if Config.ChipMode[2] is 0.

Notes:

1. These parameters are characterized, but not production tested.
2. The power-up delay will be significantly longer if power-on self test is enabled in the Configuration zone.

2.3.1 AC Parameters: Single-Wire Interface

Figure 2-2. AC Timing Diagram: Single-Wire Interface

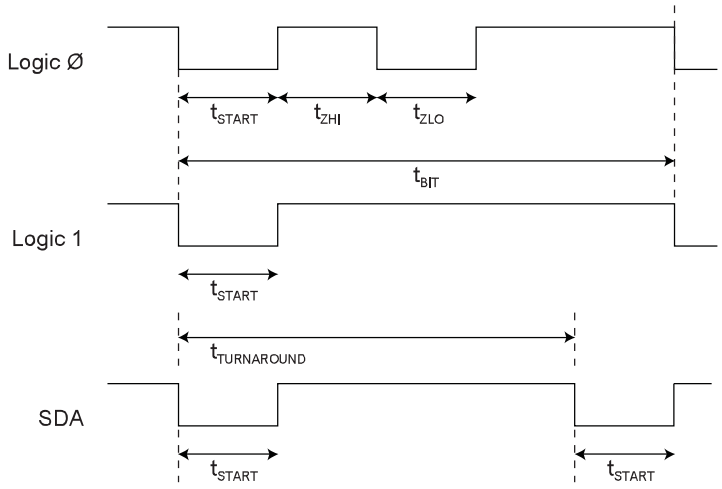


Table 2-3. AC Parameters: Single-Wire Interface

Unless otherwise specified, applicable from T_A = -40°C to +100°C, V_{CC} = +2.0V to +5.5V, C_L = 100 pF.

Parameter	Symbol	Direction	Min.	Typ.	Max.	Unit	Conditions
Start Pulse Duration	t_{START}	To Crypto Device	4.10	4.34	4.56	µs	—
		From Crypto Device	4.60	6	8.60	µs	—
Zero Transmission High Pulse	t_{ZHI}	To Crypto Device	4.10	4.34	4.56	µs	—
		From Crypto Device	4.60	6	8.60	µs	—
Zero Transmission Low Pulse	t_{ZLO}	To Crypto Device	4.10	4.34	4.56	µs	—
		From Crypto Device	4.60	6	8.60	µs	—
Bit Time(1)	t_{BIT}	To Crypto Device	37	39	—	µs	If the bit time exceeds $t_{TIMEOUT}$, ATECC608B may enter Sleep mode.
		From Crypto Device	41	54	78	µs	—
Turn Around Delay	$t_{TURNAROUND}$	From Crypto Device	64	96	131	µs	ATECC608B will initiate the first low going transition after this time interval following the initial falling edge of the start pulse of the last bit of the transmit flag.
		To Crypto Device	93	—	—	µs	After ATECC608B transmits the last bit of a group, the system must wait this interval before sending the first bit of a flag. It is measured from the falling edge of the start pulse of the last bit transmitted by ATECC608B.
IO Timeout	$t_{TIMEOUT}$	To Crypto Device	45	65	85	ms	ATECC608B may transition to the Sleep mode if the bus is inactive longer than this duration.

Note:

1. t_{START}, t_{ZLO}, t_{ZHI} and t_{BIT} are designed to be compatible with a standard UART running at 230.4 kBaud for both transmit and receive. The UART must be set to seven data bits, no parity and one Stop bit.

2.3.2 AC Parameters: I²C Interface

Figure 2-3. I²C Synchronous Data Timing

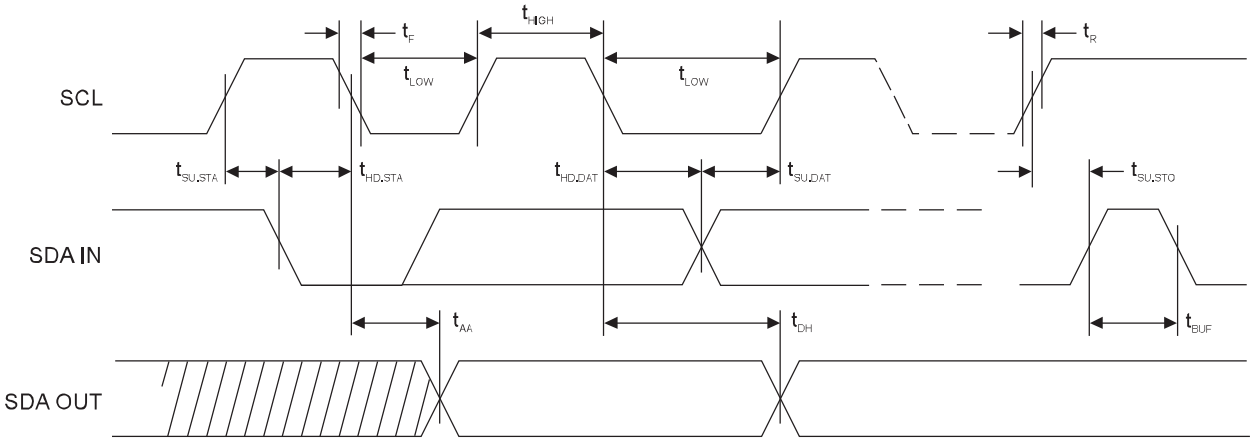


Table 2-4. AC Characteristics of I²C Interface(2)

Unless otherwise specified, applicable over recommended operating range from T_A = -40°C to +100°C, V_{CC} = +2.0V to +5.5V, C_L = 1 TTL Gate and 100 pF.

Parameter	Sym.	Min.	Max.	Units
SCL Clock Frequency	f_{SCL}	0	1	MHz
SCL High Time	t_{HIGH}	400	—	ns
SCL Low Time	t_{LOW}	400	—	ns
Start Setup Time	$t_{SU.STA}$	250	—	ns
Start Hold Time	$t_{HD.STA}$	250	—	ns
Stop Setup Time	$t_{SU.STO}$	250	—	ns
Data In Setup Time	$t_{SU.DAT}$	100	—	ns
Data In Hold Time	$t_{HD.DAT}$	0	—	ns
Input Rise Time[1]	t_R	—	300	ns
Input Fall Time[1]	t_F	—	100	ns
Clock Low to Data Out Valid	t_{AA}	50	550	ns
Data Out Hold Time	t_{DH}	50	—	ns
SMBus Time-Out Delay	$t_{TIMEOUT}$	25	75	ms
Time bus must be free before a new transmission can start[1]	t_{BUF}	500	—	ns

Notes:

1. Values are based on characterization and are not tested.
2. AC measurement conditions:
   - R_L (connects between SDA and V_{CC}): 1.2 kΩ (for V_{CC} = +2.0V to +5.0V)
   - Input pulse voltages: $0.3V_{CC}$ to $0.7V_{CC}$
   - Input rise and fall times: ≤ 50 ns
   - Input and output timing reference voltage: $0.5V_{CC}$

2.4 DC Parameters: All I/O Interfaces

Table 2-5. DC Parameters on All I/O Interfaces

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Ambient Operating Temperature	T_A	-40	—	+85	°C	Standard Industrial Temperature Range
		-40	—	+100	°C	Extended Industrial Temperature Range
Power Supply Voltage	V_{CC}	2.0	—	5.5	V	—
Active Power Supply Current	I_{CC}	—	2	3	mA	Waiting for I/O during I/O transfers or execution of non-ECC commands. Independent of Clock Divider value.
		—	—	14	mA	During ECC command execution. Clock divider = 0x0
		—	—	6	mA	During ECC command execution. Clock divider = 0x5
		—	—	3	mA	During ECC command execution. Clock divider = 0xD
Idle Power Supply Current	I_{IDLE}	—	800	—	µA	When device is in Idle mode, V_{SDA} and V_{SCL} < 0.4V or > V_{CC} – 0.4
Sleep Current	I_{SLEEP}	—	30	150	nA	When device is in Sleep mode, V_{CC} ≤ 3.6V, V_{SDA} and V_{SCL} < 0.4V or > V_{CC} – 0.4, T_A ≤ +55°C
		—	—	2	µA	When device is in Sleep mode. Over full V_{CC} and temperature range.
Output Low Voltage	V_{OL}	—	—	0.4	V	When device is in Active mode, V_{CC} = 2.5 to 5.5V
Output Low Current	I_{OL}	—	—	4	mA	When device is in Active mode, V_{CC} = 2.5 to 5.5V, V_{OL} = 0.4V
Theta JA	Θ_{JA}	—	166	—	°C/W	SOIC (SSH)
		—	173	—	°C/W	UDFN (MAH)
		—	146	—	°C/W	RBH

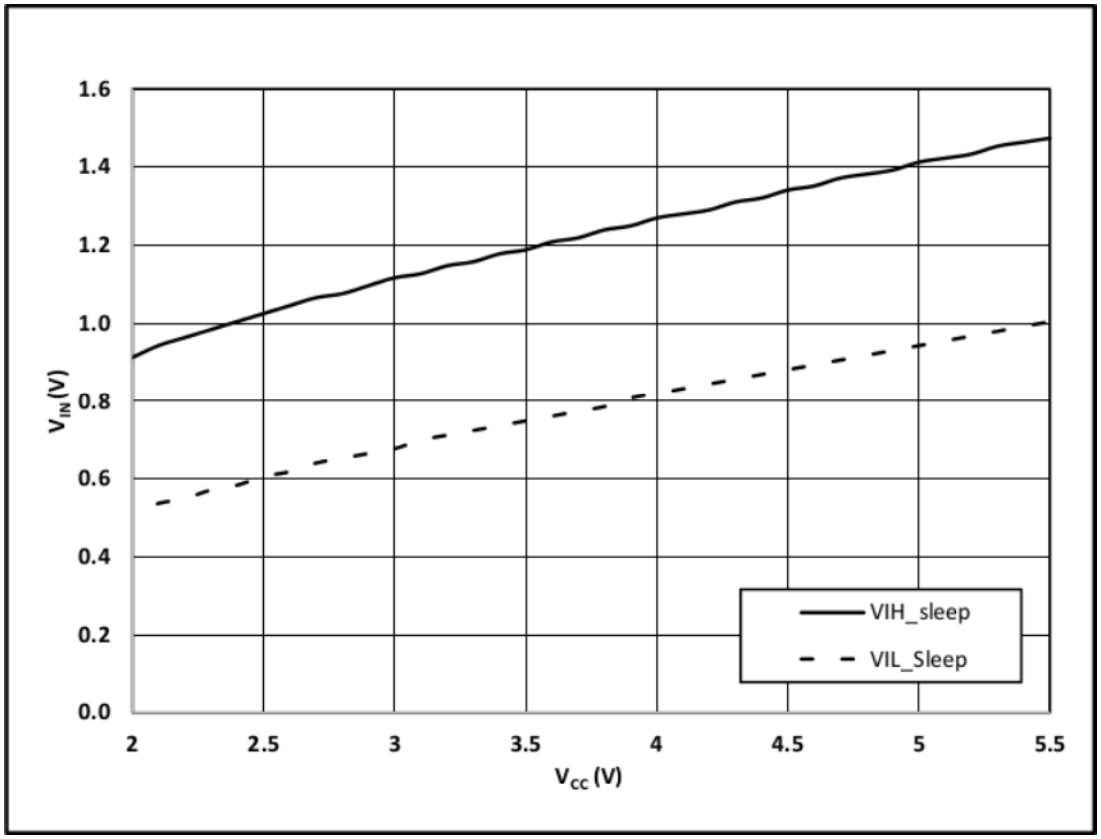
2.4.1 V_{IH} and V_{IL} Specifications

The input levels of the device will vary dependent on the mode and voltage of the device. The input voltage thresholds when in Sleep or Idle mode are dependent on the V_{CC} level as shown in Figure 2-4. When in Sleep or Idle mode the TTLenable bit has no effect.

Table 2-6. V_{IL}, V_{IH} on All I/O Interfaces (TTLenable = 0)

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Low Voltage	V_{IL}	-0.5	—	0.5	V	When device is active and TTLenable bit in Configuration memory is zero; otherwise, see above.
Input High Voltage	V_{IH}	1.5	—	V_{CC} + 0.5	V	When device is active and TTLenable bit in Configuration memory is zero; otherwise, see above.

Figure 2-4. V_{IH} and V_{IL} in Sleep and Idle Mode



3. Compatibility

3.1 Microchip ATECC608A

The ATECC608B is designed to provide an enhanced security profile over that of the ATECC608A while maintaining backwards compatibility. The following details the changes and enhancements to the device. No configuration bit fields have changed. Configurations defined for the ATECC608A will be functionally identical with the ATECC608B device.

Corrections, Enhancements

The following items have been corrected or enhanced in the ATECC608B device:

- Two temperature ranges are now available:
  - Standard Industrial Temperature Range: -40°C to +85°C
  - Standard Industrial Temperature Range: -40°C to +100°C
- Operating at a low I^2C Frequency with multiple devices on the bus will no longer create a bus contention issue.
- Modifications to Command Timings for `Verify`, `SecureBoot`, `Lock` and `Read` commands.
- New Packaging Options: 3-Lead Contact Package and WLCSP for qualified customers. (Contact Microchip Sales for the WLCSP Option.)

3.2 Microchip ATECC508A

The ATECC608B is designed to be fully compatible with the ATECC508A devices with the limited exception of the functions listed below. If the ATECC608B is properly configured, software written for the ATECC508A will work with the ATECC608B without any required changes, again with the exception of the functions listed below.

Note: Most elements of the configuration zone in the ATECC608B are identical in both location and value with the ATECC508A. However, the initial values that had been stored in the LastKeyUse field may need to be changed to conform to the new definition of those bytes which can be found in this document. That field contained the initial count for the Slot 15 limited use function which is supported in the ATECC608B via the monotonic counters.

⚠ CAUTION The execution times of commands have changed between the ATECC608B and the ATECC508A. These changes will not cause an issue if polling has been implemented. If fixed timing has been used, this must be evaluated and updated as required.

New Features in ATECC608B vs. ATECC508A

- Secure boot function with IO encryption and authentication
- `KDF` command, supporting PRF, HKDF, AES
- `AES` command, including encrypt/decrypt
- GFM calculation function for GCM AEAD mode of AES
- Updated NIST SP800-90 A/B/C Random Number Generator
- Flexible `SHA/HMAC` command with context save/restore
- `SHA` command execution time significantly reduced
- Volatile Key Permitting to prevent device transfer
- Transport Key Locking to protect programmed devices during delivery
- Counter Limit Match function
- Ephemeral key generation in SRAM, also supported with ECDH and KDF
- `Verify` command output can be validated with a MAC
- Encrypted output for ECDH

- Added self test command, optional automatic power-on self test
- Unaligned public key for built-in X.509 cert key validation
- Optional power reduction at increased execution time
- Programmable I^2C address after data (secret) zone lock

Features Eliminated in ATECC608B vs. ATECC508A

- HMAC command removed, replaced via new more powerful SHA command
- OTP consumption mode eliminated, now read only
- Pause command eliminated along with related Selector function in UpdateExtra
- Slot 15 special limited use eliminated, replaced with standard monotonic counter limited use
- SHA command no longer uses TempKey during the digest calculation and the result in TempKey is unchanged throughout the SHA operation. TempKey can however still be used to initialize the SHA for the HMAC_Start or to store the final digest.

3.3 Microchip ATSHA204A, ATECC108A

The ATECC608B is generally compatible with all ATSHA204/A and ATECC108/A devices. If properly configured, it can be used in most situations where these devices are currently employed. For ATSHA204A and ATECC108A compatibility restrictions, see the ATECC508A data sheet.

4. Package Marking Information

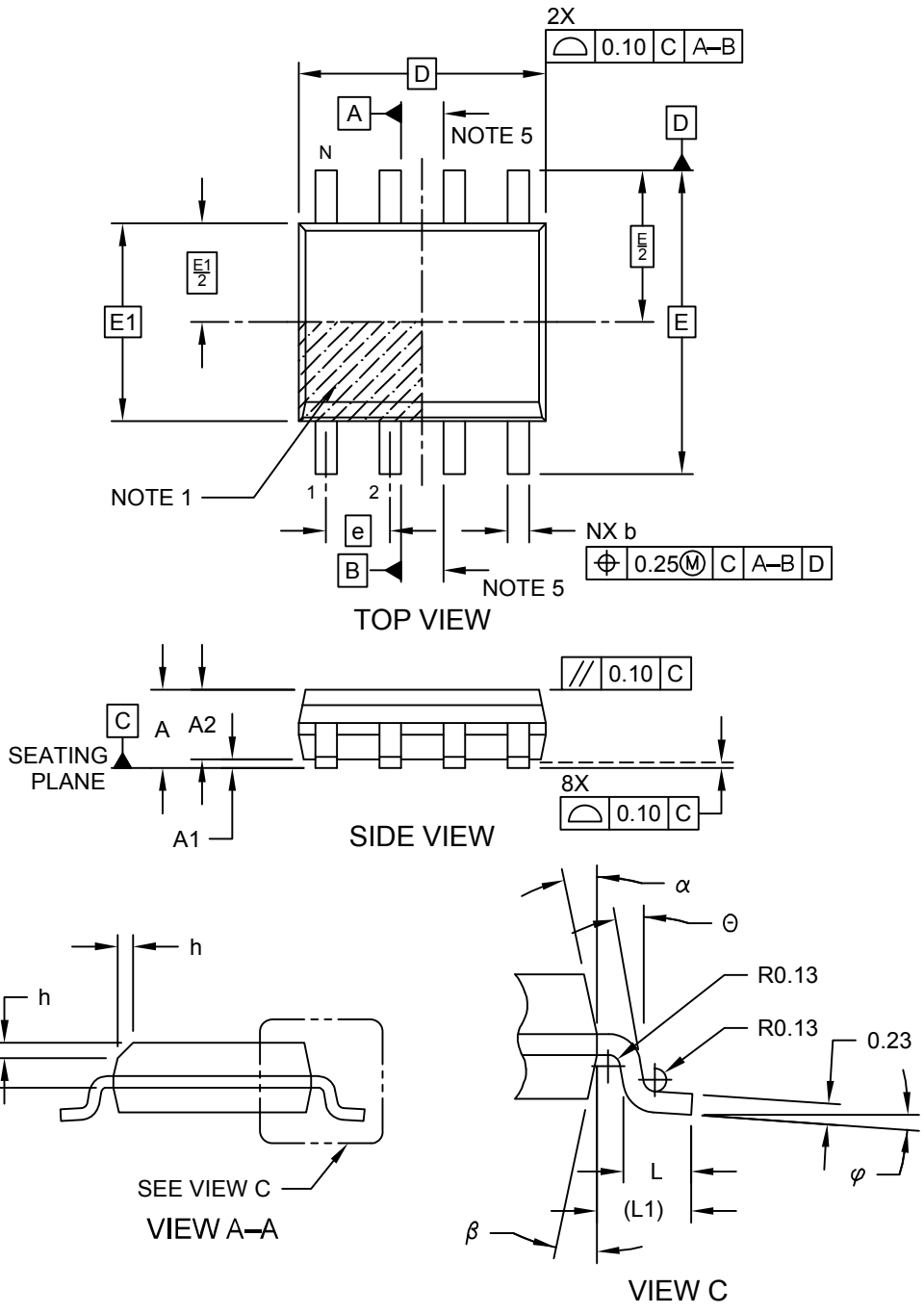
As part of Microchip's overall security features, the part marking for all crypto devices is intentionally vague. The marking on the top of the package does not provide any information as to the actual device type or the manufacturer of the device. The alphanumeric code on the package provides manufacturing information and will vary with assembly lot. The packaging mark should not be used as part of any incoming inspection procedure.

5. Package Drawings

5.1 8-lead SOIC

8-Lead Plastic Small Outline - Narrow, 3.90 mm (.150 In.) Body [SOIC]
Atmel Legacy Global Package Code SWB

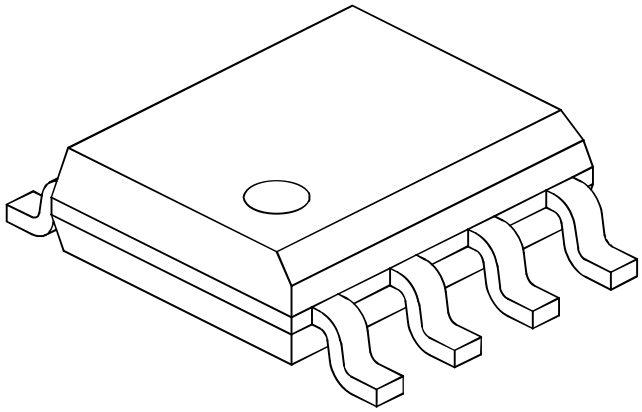
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-SWB Rev E Sheet 1 of 2

8-Lead Plastic Small Outline - Narrow, 3.90 mm (.150 In.) Body [SOIC]
Atmel Legacy Global Package Code SWB

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

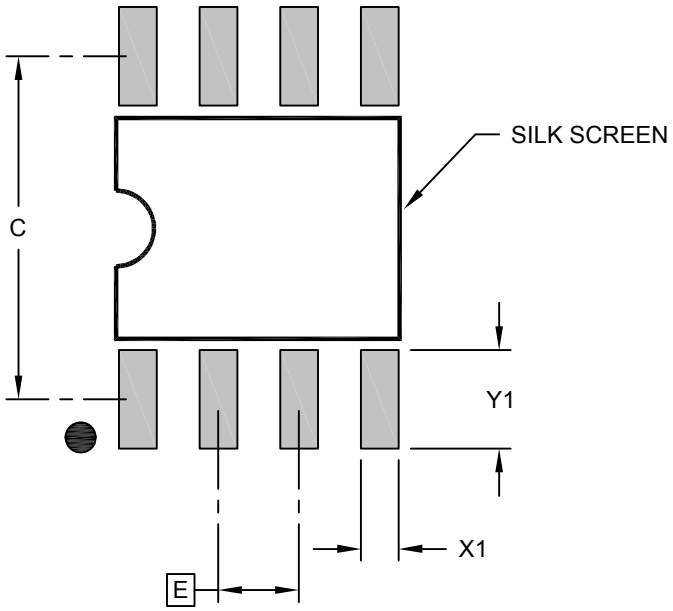
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SWB Rev E Sheet 2 of 2

8-Lead Plastic Small Outline - Narrow, 3.90 mm (.150 In.) Body [SOIC]
Atmel Legacy Global Package Code SWB

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

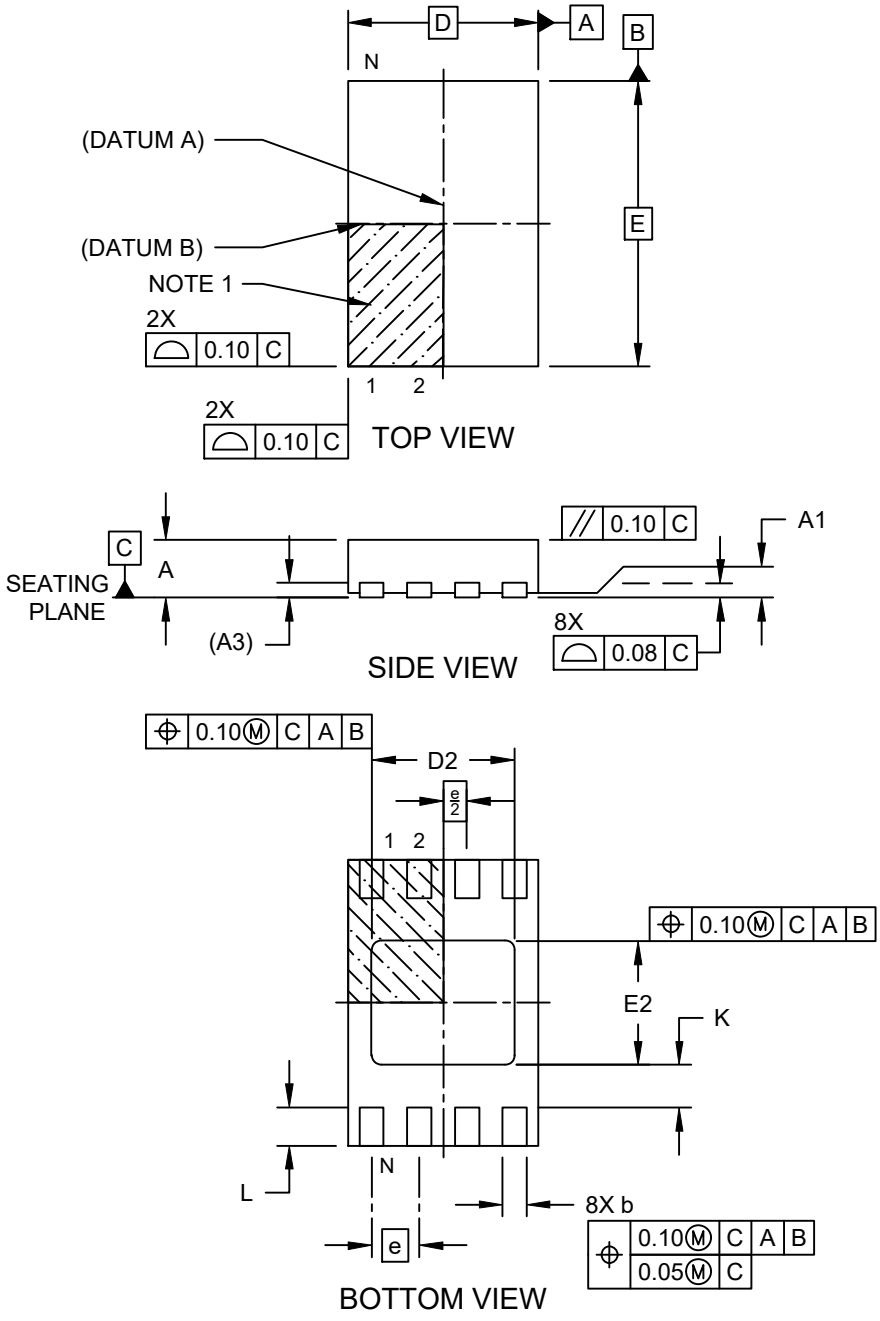
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SWB Rev E

5.2 8-pad UDFN

8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN]
Atmel Legacy Global Package Code YNZ

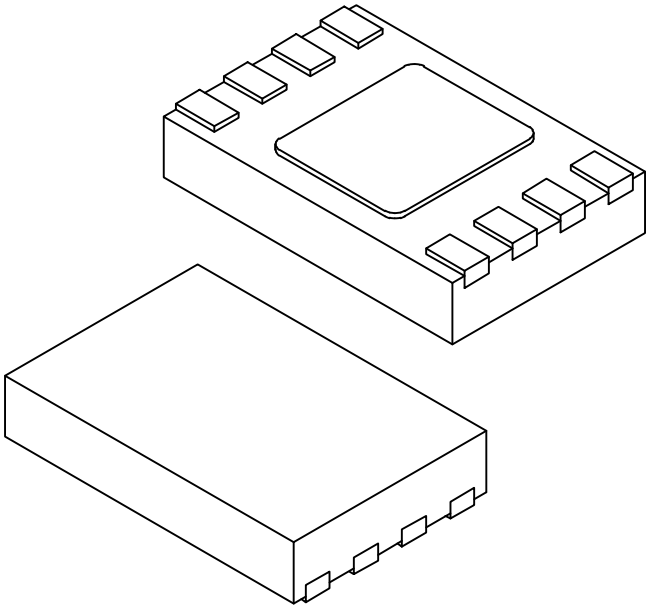
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-21355-Q4B Rev B Sheet 1 of 2

8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN]
Atmel Legacy Global Package Code YNZ

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.50	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.152 REF	
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	1.40	1.50	1.60
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.20	1.30	1.40
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

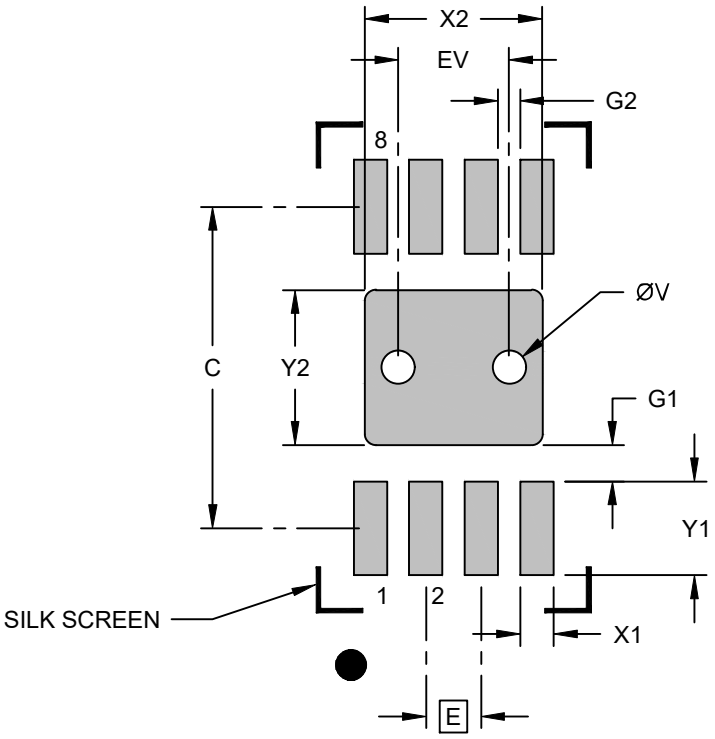
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21355-Q4B Rev B Sheet 2 of 2

8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN]
Atmel Legacy Global Package Code YNZ

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			1.60
Optional Center Pad Length	Y2			1.40
Contact Pad Spacing	C		2.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.85
Contact Pad to Center Pad (X8)	G1	0.33		
Contact Pad to Contact Pad (X6)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

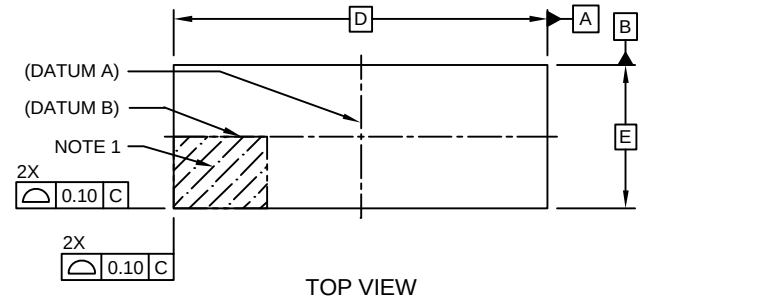
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23355-Q4B Rev B

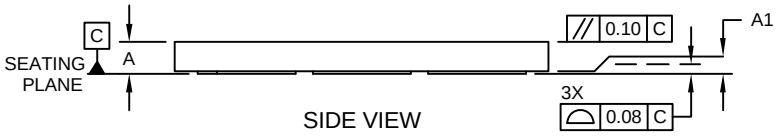
5.3 3 Lead Contact

3-Lead Contact Package (LAB) - 6.54x2.5 mm Body [Contact]
Atmel Legacy Global Package Code RHB

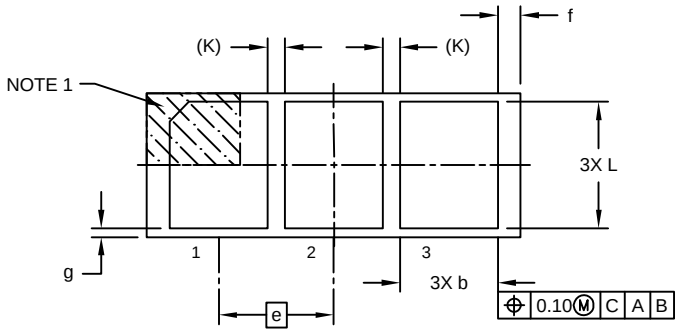
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

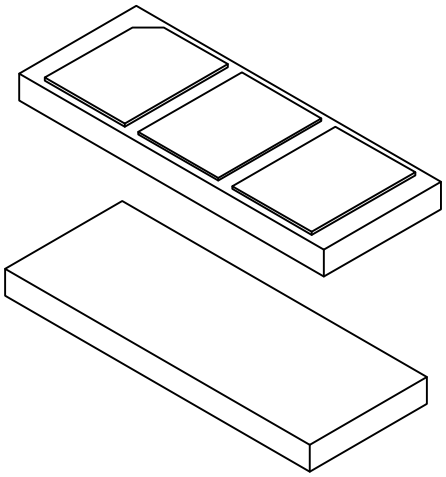


BOTTOM VIEW

Microchip Technology Drawing C04-21303 Rev A Sheet 1 of 2

3-Lead Contact Package (LAB) - 6.54x2.5 mm Body [Contact]
Atmel Legacy Global Package Code RHB

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		3	
Pitch	e		2.00 BSC	
Overall Height	A	0.45	0.50	0.55
Standoff	A1	0.00	0.02	0.05
Overall Length	D		6.50 BSC	
Overall Width	E		2.50 BSC	
Terminal Width	b	1.60	1.70	1.80
Terminal Length	L	2.10	2.20	2.30
Terminal-to-Terminal Spacing	K		0.30 REF	
Package Edge to Terminal Edge	f	0.30	0.40	0.50
Package Edge to Terminal Edge	g	0.05	0.15	0.25

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21303 Rev A Sheet 2 of 2

6. Revision History

Revision	Date	Description
A	July 2020	Original Release. Based on ATECC608A Summary Data Sheet Rev B. DS40001977B

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- **General Technical Support –** Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
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To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-XX	X	XX	-X
Device	Package	Temp Range	I/O Type	Tape and Reel

Device:	ATECC608B: Cryptographic Co-processor with Secure Hardware-based Key Storage	
Package Options(3)	SS	8-Lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)
	MA	8-Pad 2 x 3 x 0.6 mm Body, Thermally Enhanced Plastic Ultra Thin Dual Flat NoLead Package (UDFN)
	RB	3RB, 3-Lead 2x5 x 6.5mm Body, 2.0mm pin pitch, Contact Package (Sawn)
Temperature Range	H	Standard Industrial Temperature Range: -40 °C to 85 °C
	V	Extended Industrial Temperature Range: -40 °C to 100 °C
I/O Type	CZ	Single Wire Interface
	DA	I^2C Interface
Tape and Reel Options	B	Tube
	T	Large Reel (Size varies by package type)
	S	Small Reel (Only available for MA Package Type)

Device Ordering Codes

Temperature Range		Description
Standard Industrial	Extended Industrial	
ATECC608B-SSHCZ-T	ATECC608B-SSVCZ-T	8-Lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC), Single-Wire, Tape and Reel, 4,000 per Reel
ATECC608B-SSHCZ-B	ATECC608B-SSVCZ-B	8-Lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC), Single-Wire, Tube, 100 per Tube
ATECC608B-SSHDA-T	ATECC608B-SSVDA-T	8-Lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC), I^2C, Tape and Reel, 4,000 per Reel
ATECC608B-SSHDA-B	ATECC608B-SSVDA-B	8-Lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC), I^2C, Tube, 100 per Tube
ATECC608B-MAHCZ-T	ATECC608B-MAVCZ-T	8-Pad 2 x 3 x 0.6 mm Body, Thermally Enhanced Plastic Ultra Thin Dual Flat NoLead Package (UDFN), Single-Wire, Tape and Reel, 15,000 per Reel
ATECC608B-MAHDA-T	ATECC608B-MAVDA-T	8-Pad 2 x 3 x 0.6 mm Body, Thermally Enhanced Plastic Ultra Thin Dual Flat NoLead Package (UDFN), I^2C, Tape and Reel, 15,000 per Reel
ATECC608B-MAHCZ-S	ATECC608B-MAVCZ-S	Pad 2 x 3 x 0.6 mm Body, Thermally Enhanced Plastic Ultra Thin Dual Flat NoLead Package (UDFN), Single-Wire, Tape and Reel, 3,000 per Reel
ATECC608B-MAHDA-S	ATECC608B-MAVDA-S	8-Pad 2 x 3 x 0.6 mm Body, Thermally Enhanced Plastic Ultra Thin Dual Flat NoLead Package (UDFN), I^2C, Tape and Reel, 3,000 per Reel
ATECC608B-RBHCZ-T	ATECC608B-RBVCZ-T	Single-Wire, Tape and Reel, 5,000 per Reel, 3-Lead Contact Package
ATECC608B-RBHCZ-B	ATECC608B-RBVCZ-B	Single-Wire, Tube, 56 per Tube, 3-Lead Contact Package

Notes:

1. Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
2. Small form-factor packaging options may be available. Please check www.microchip.com/packaging for small-form factor package availability, or contact your local Sales Office.
3. Die-on-Tape and Reel and WLCSP packages are available for qualified customers. Ordering codes for these packages are not shown in this table. Please contact Microchip sales for more information on these package options.

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Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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Canada - Toronto			Fax: 44-118-921-5820
Tel: 905-695-1980			
Fax: 905-695-2078			

MICROCHIP

AN2237

Migrating from the ATECC608A to the ATECC608B

Introduction

Author: James Boomer – Microchip Technology Inc.

Over time, security capabilities and expectations evolve within the security world along with the capabilities of attacks that seek to compromise secure systems. Recognizing these changes, Microchip has developed a security-enhanced version of the ATECC608A, known as the ATECC608B. The security changes implemented in the device are largely behind the scenes and are not directly observable during normal operation. The ATECC608B has been designed to allow an easy migration from the ATECC608A, while improving the overall security.

For new designs, it is recommended that users start directly with the ATECC608B. For designs that are going through an upgrade or a revision, it is recommended that part of the upgrade include the ATECC608B. For other designs, users must do an overall security assessment and determine if they need to migrate to the ATECC608B.

The ATECC608B continues the line of security products developed as part of the Microchip CryptoAuthentication™ family of high-security cryptographic devices. These devices combine world-class hardware-based key storage with hardware cryptographic accelerators to implement various authentication and encryption protocols. All applications and use cases previously supported by the ATECC608A are also supported by the ATECC608B.

Applications Summary

- **Network/Internet of Things (IoT) Node Endpoint Security –** Manages node identity authentication and session key creation and management. Support is provided for the ephemeral session key generation flow for multiple protocols including TLS 1.2 and TLS 1.3.
- **Firmware Validation (Secure Boot) –** Supports the microcontroller (MCU) host by validating code digests and optionally enabling communication keys upon a successful secure boot. For an enhanced performance, various configurations are available.
- **Small Message Encryption –** Hardware Advanced Encryption Standard (AES) engine to encrypt and/or decrypt small messages or data such as Personally Identifiable Information (PII). The device supports the AES-ECB mode directly. Other AES modes are supported with help from the host. Additional Galois Field Multiply (GFM) calculation functions support the AES Galois Counter Mode (AES-GCM).
- **Secure Over-the-Air (OTA) Updates –** Supports local protected key generation for downloaded images. Both broadcasts of one image to many systems, each with the same decryption key, and point-to-point download of unique images per system are supported.
- **Accessory/Disposable Authentication –** Validates the authenticity of a system or component. This capability is often sought where disposable components are part of a system.

Table of Contents

1. Device Differences

The overall structure of the ATECC608B is identical to that of the ATECC608A. The ATECC608B does not introduce any new configuration bits and has the same number of data slots as that of the ATECC608A. All commands and command modes are still supported. The device supports both the I²C and SWI interface I/O protocols. The pinouts for the 8-pin SOIC and UDFN packages remain unchanged.

The following sections describe the differences between the ATECC608A and the ATECC608B devices.

Low-Frequency I²C Issue

The ATECC608A has an error in the I²C circuitry, where the device may respond incorrectly under the following conditions:

- Multiple I²C devices are on the same bus as the ATECC608A.
- The ATECC608A device was in Idle mode.
- The I²C operation frequency is ≤ 300 kHz.
- A data pattern from other devices on the I²C bus could be interpreted by the ATECC608A as a wake pulse.

Under the above conditions, the ATECC608A wakes up and may corrupt data being sent to other devices on the bus. Whether or not data are corrupted depends on the frequency of operation and the actual data being sent.

This issue has been corrected for the ATECC608B device by modifying the I²C circuitry to eliminate this issue. Note that the ATECC608B may still wake up at low frequency but it does not respond or cause data corruption.

Device Revision (DevRev) Differences

The package marking on Microchip security devices does not identify the device type. Therefore, the package marking cannot be used to identify the ATECC608B. The only way to identify the device is through use of the device revision. The hardware device revision of the device can be read by using the Revision mode (0x00) of the `Info` command. The output response of the `Info` command for each device is as follows:

Table 1-1. Revision Response

Device	Revision Response
ATECC608A	0x00 0x00 0x60 0x02
ATECC608B	0x00 0x00 0x60 0x03 (**Note**)

Note: The value of the fourth byte may change over time but it is 0x03 at the time of the initial product release.

Important: The value of the Revision mode response is not the same as the 4-byte RevNum (Bytes[4:7]) in the device configuration zone. Only the Revision mode response can be used for device identification.

Execution Time Differences

The implementation of security enhancements has resulted in changes to the execution times of a few commands. The variation depends on the actual Clock Divider mode as well as the specific mode of operation. The following table shows a list of commands and expected differences in execution times.

Notice: For a more detailed understanding of the execution times, refer to the complete data sheet.

Table 1-2. ATECC608A vs. ATECC608B Execution Time Differences

Command	Description of Changes
`Verify`	• The execution times of the `Verify` command will increase by no more than 10%. Actual variation may depend on the specific mode of the command. • The execution time increase will occur for all three Clock Divider modes.
`SecureBoot`	• The `SecureBoot` command includes a verify operation. The increase in execution time is due to the Verify portion of this command. • The execution times of the `SecureBoot` command will increase by no more than 10%. Actual variation may depend on the specific mode of the command. • The execution time increase will occur for all three Clock Divider modes.
`Read`	• The increase in read times is dependent on what is being read. • Reads of the configuration zone have increased by roughly 50% (0.8 ms to 1.2 ms) for a 32-byte read. • Reads of the data zone have approximately doubled. (0.9 ms to 1.8 ms) for a 32-byte read. • This does not apply to reading back a command response. This time will remain the same. • The execution time increase does not vary with the Clock Divider modes.
`Lock`	• The maximum lock time for either the configuration zone or the data zone increases by approximately 30%. • Since production units are shipped in a locked state, this does not impact normal device operation and is just observed by the user during the prototyping or development phase. • The execution time increase does not vary with the Clock Divider modes.

Enhanced Temperature Range

The ATECC608A is specified over the industrial temperature range of -40°C to +85°C.

The ATECC608B is specified over the standard industrial range of -40°C to +85°C and an extended range of -40°C to +100°C, for those users that need an upper ambient temperature value > +85°C. The enhanced temperature range devices have a unique ordering code that is found in the device's data sheet.

New Packages

The ATECC608B is now available in a 3-pin RBH contact package. This is in addition to the already existing 8-pin SOIC and UDFN packages. This package has been used previously for the ATSHA204A and the ATECC508A CryptoAuthentication devices. The RBH package is only available for devices in SWI interface mode.

The RBH package is a contact package that is typically mounted by gluing the package to an enclosure with the signal pads exposed. Contacts to the pads are usually made through pogo pins when the disposable unit is connected to the host system.

2. ATECC608B Migration

The ATECC608B has the same form, fit and function as the ATECC608A. The packages and pinouts are the same, the device structure is the same and so are the commands and command structure. This makes the ATECC608B a functional drop-in replacement of the ATECC608A. If the users implement their design utilizing the Microchip's software library (CryptoAuthLib), this further simplifies the migration process.

An additional factor that has to be considered is the timing differences between the ATECC608A and the ATECC608B for a specific design. This really depends on how the software was implemented. There are two cases that require consideration:

Fixed Timing Implementation
If the code is written assuming hardwired timing parameters, careful analysis must be undertaken to evaluate the impact of changing from the ATECC608A to the ATECC608B. Under this method, after a command is issued, the microcontroller will wait a fixed period of time before reading the response data back. If the delay required for the ATECC608B is significantly longer than the ATECC608A, this command may fail. Using an older version of CryptoAuthLib meant for the ATECC608A or a customer-generated library with the ATECC608B could cause some timing errors. Implementing the latest version of CryptoAuthLib correctly updates the timing information and, through just recompiling the code and reflashing the micro, the timing issues may be corrected. In general, the parameters used for fixed timing are broad enough that they will be conservative to actual worst-case timing values and may still not be an issue. As noted in **Section 1. Device Differences**, the timing changes of the ATECC608B and ATECC608A are relatively minor. Also, these are representative times for the specific command modes and there are other items (as noted in the data sheet) that could cause these values to step out further.

If timing is an issue, the following solutions can be considered:

1. Migrate the code to use the latest version of the CryptoAuthLib library.
2. Migrate the code to use polled timing. See **Section 2. Polled Timing Implementation** below.
3. If a custom library with fixed timing is used, update the library timing parameters needed for the ATECC608B.
4. Implement redundancy by trying to read back data a second time upon receiving a failure code that indicates the response was not yet ready.

Polled Timing Implementation
Polled timing is set as the default mode of operation when using the CryptoAuthLib library. If the code is written using polling, there will be no issues with migrating to the ATECC608B. In this scenario, the microcontroller would poll the ATECC608B to determine when data are available to be read. Minor timing differences would be absorbed by the polling command. These differences can be fully absorbed by the ATECC608B device because none of the execution times of the commands have stepped out significantly.

2.1 I^2C Low-Frequency ATECC608B Migration

Migrating an ATECC608A design that has to deal with the low-frequency I^2C issue requires no changes to either hardware or firmware. The changes implemented for a correct operation with the ATECC608A will not cause an issue with the fixed ATECC608B.

The user must consider if the operation of the system is better served by backing out the firmware changes implemented to correct the ATECC608A issues. Removing these changes would most likely result in reduced firmware size and improved system performance. Whether these are reasons valuable enough to modify the working code is up to the implementer.

3. Conclusion

Because the form, fit and function of the ATECC608B are nearly identical to those of the ATECC608A, the migration is typically a fairly minor task. The minor timing differences between the devices, in general, will not cause an issue and can be easily corrected if they do. The addition of the new RBH package and the enhanced temperature range also increase the market space for the ATECC608B secure element.

The changes implemented in the ATECC608B were primarily done to enhance device security and are largely transparent to the user. For new system designs and a refresh of the existing systems, it is strongly recommended to convert to the ATECC608B as a way to enhance overall system security.

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Migrating from the ATECC508A to the ATECC608B

Introduction

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The ATECC608B is a security enhanced version of the ATECC608A and a security enhanced and feature upgrade to the ATECC508A. All these devices are products in the Microchip CryptoAuthentication™ family of high-security cryptographic devices. The security changes implemented in the device are largely behind the scenes and are not directly observable during normal operation.

For new designs, it is recommended that users start directly with the ATECC608B. For designs that are going through an upgrade or a revision, it is recommended that part of the upgrade include the ATECC608B. For other designs, it is recommended that users do an overall security assessment and determine if they need to migrate to the ATECC608B.

The ATECC608B continues the line of security products developed as part of the Microchip CryptoAuthentication family of high-security cryptographic devices. These devices combine world-class hardware-based key storage with hardware cryptographic accelerators to implement various cryptographic functions and algorithms. All applications and use cases previously supported by the ATECC508A are also supported by the ATECC608B.

The ATECC608B device is compatible with the ATECC508A device and with some limited exceptions, allows for easy migration. If the ATECC608B is properly configured, the software written for the ATECC508A will work with the ATECC608B. For more information, see **Section 4. Migration from the ATECC508A to the ATECC608B**. This application note lists the features, commands and configuration differences between the ATECC608B and the ATECC508A. It provides high-level details about the differences. For detailed information on the commands and configurations, compare the ATECC608B and the ATECC508A data sheets.

References

- ATECC508A Product Page
- ATECC608B Product Page

Applications Summary

- **Network/Internet of Things (IoT) Node Endpoint Security –** Manages node identity authentication and session key creation and management. Support is provided for the ephemeral session key generation flow for multiple protocols including TLS 1.2 and TLS 1.3.
- **Firmware Validation (Secure Boot) –** Supports the microcontroller (MCU) host by validating code digests and optionally enabling communication keys upon a successful secure boot. For an enhanced performance, various configurations are available.
- **Small Message Encryption –** Contains a Hardware Advanced Encryption Standard (AES) engine to encrypt and/or decrypt small messages or data such as Personally Identifiable Information (PII). The device supports the AES-ECB mode directly. Other AES modes are supported with help from the host. Additional Galois Field Multiply (GFM) calculation functions support AES Galois Counter Mode (AES-GCM).
- **Secure Over-the-Air (OTA) Updates –** Supports local protected key generation for downloaded images. Both broadcasts of one image to many systems, each with the same decryption key, and point-to-point downloads of unique images per system are supported.
- **Accessory/Disposable Authentication –** Validates the authenticity of a system or component. This capability is often sought where disposable components are part of a system.

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1. Feature Differences

The overall architecture of the ATECC608B is very similar to that of the ATECC508A. The ATECC608B has some configuration mode changes but has the same number of data slots as the ATECC508A. The majority of commands are compatible but some new commands or modes have been introduced and a couple of commands of the ATECC508A are no longer supported.

Both devices support the I^2C and SWI interface I/O protocols. The pinouts and footprints for the 8-pin SOIC, 8-pad UDFN and 3-pin RBH contact packages remain unchanged, allowing a pin-to-pin compatibility between devices.

The following sections describe the various feature differences available for the ATECC608B compared to the ATECC508A.[1] This includes new features, updated features and features that have been removed from this device.

1.1 New Features

1.1.1 Secure Boot

The ATECC608B provides a mechanism to support secure boot operations in a connected MCU/MPU (microprocessor). This can help to identify situations in which fraudulent code has been installed on the host. On power-up, the boot code within the host MCU sends the code digest and/or signature to the ATECC608B. If the signature validates the digest using the public key stored in the ATECC608B or the digest is compared to the stored digest, a message is returned to the MCU host. It also enables a reduction in the execution time of the boot process with its different methods and thus provides the secure boot speed optimization. To mitigate the Man-in-the-Middle (MITM) attack, the ATECC608B returns the optional Message Authentication Code (MAC) value to the MCU host, where the MCU host verifies the returned MAC.

1.1.2 Key Derivation Function

The ATECC608B supports the key derivation function (KDF), which derives the KDF key from the premaster secret key. The final derived KDF key is mainly used in TLS transactions. The ATECC608B supports three key derivation functions: Pseudo Random Function (PRF), AES and HMAC-Based Extract-and-Expand KDF (HKDF). The PRF is used in TLS version 1.2 and the HKDF is used in TLS version 1.3.

1.1.3 AES

The ATECC608B supports a Hardware 128-bit AES engine to encrypt and/or decrypt small messages or data packets. It supports an Electronic Code Block (ECB) mode and a GFM calculation for AES-GCM.

1.1.4 Self-Test

The ATECC608B provides a mechanism to test the internal cryptographic algorithms. It supports the self validation testing of the Symmetric HASH Algorithm (SHA), AES, Random Number Generator (RNG), Elliptic Curve Diffie-Hellman (ECDH), Elliptic Curve Digital Signature Algorithm (ECDSA) verify and ECDSA sign functions. The self test can be run automatically on device power-up or wake-up or initiated by the `SelfTest` command from the host.

1.1.5 I/O Protection Key

The ATECC608B provides a method to protect the I/O transmissions between this device and the host MCU for `ECDH`, `KDF`, `Verify` and `Secure Boot` commands. The I/O protection key is a randomly-generated secret key stored in the slot and is shared between the host MCU and the device.

For example, the premaster key generated from ECDH or the generated KDF key are encrypted by the I/O protection key. The encrypted key is sent to the host and the host decrypts it with the I/O protection key. In the secure boot and the signature verification process, a MAC is sent to the host to provide additional security. This MAC is generated by including the I/O protection key.

[1] All differences described in this document are also applicable to the ATECC608A, with respect to the ATECC508A, except as noted.

1.1.6 Persistent Latch

The Persistent Latch is a single bit of volatile memory used to indicate to the device that an associated key has been enabled for use with cryptographic functions. It can retain its state as long as the V_{CC} remains above 2V. It is always set to low on power-up and can be manipulated using various operations. When the key in a slot is linked to the Persistent Latch, a Persistent Latch state activates/deactivates the key in the slot. There are four ways to control the Persistent Latch: volatile key usage, secure boot, authorization output and intrusion detection. When one of the above methods is run successfully, the Persistent Latch will be set, thus enabling the key in the designated slot.

Notice: The ATECC508A had a Persistent Latch, but it only supported the intrusion detection mode. Applications that utilize the intrusion detection latch can be implemented with the ATECC608B.

1.1.7 Volatile Key Usage Permission

The volatile key is used to control the state of the Persistent Latch. The volatile key must be the secret that is shared between the MCU and the device. The cryptographic operation is performed between the host and the device with the volatile key. If successful, the Persistent Latch can be set, thus enabling the keys in the slot that are attached to the Persistent Latch.

1.1.8 Programmable I^2C Address

The ATECC608B provides the flexibility to change the I^2C address after the configuration zone has been locked. It can only be changed once. This feature helps to update the device address dynamically after it has been provisioned in the factory. This allows for an additional configuration step in a user's manufacturing flow, where multiple devices may be deployed in a system, or it allows the address to be updated after the device is deployed in the field.

1.1.9 Counter Match

The counter match function provides a mechanism for altering the limit to which the first monotonic counter (Counter 0) can be incremented. The key usage can be connected to the counter to prevent its use when Counter 0 reaches the limit value of the counter match slot. The counter match value in the slot can be changed any number of times and, for each change, Counter 0 gets linked to the new limit.

1.1.10 Transport/UseLock

The general purpose usage of the device is prohibited until the device is cryptographically enabled. The cryptographic operation is performed with a shared secret, available from the host, and stored in the device slot. Once the operation is successful, the ATECC608B can be used normally.

1.1.11 Power Reduction

The ATECC608B provides an option for reducing power consumption. The power consumption is reduced at the cost of command execution times. The mode has been developed for applications where power is extremely critical and slower execution times can be tolerated. For more information, see **Section 3. Configuration Zone Updates**.

1.1.12 Additional Buffers for Improved Operation

The ATECC608B provides new SRAM buffers: Message Digest buffer, Alternate Key buffer and SHA Context buffer. The Message Digest buffer and Alternate Key buffer can be used when the TempKey register holds other information. Multiple buffers allow a reduction in transactions and in the transaction time between the device and the host, by allowing the execution of different commands directly from the buffers.

The ATECC608B supports multiple instances for the SHA calculation with SHA context. The SHA buffer helps the host to perform read and write operations on the SHA context, which enables the host to execute multiple instances of SHA calculations.

1.1.13 Enhanced Temperature Range

The ATECC508A is specified over the industrial temperature range of -40°C to +85°C.

The ATECC608B is specified over the standard industrial range of -40°C to +85°C and an extended range of -40°C to +100°C, for those users that need an upper ambient temperature value > +85°C. The enhanced temperature range devices have a unique ordering code that is found in the device's data sheet.

1.2 Updated Features

Updated features include an enhancement of the TempKey buffer, an enhancement of the RNG, a correction to a low-frequency I^2C issue and an update to the device revision identification information.

1.2.1 TempKey Buffer

The TempKey buffer size has been increased by 32 bytes for a total of 64 bytes, thus providing more storage and easy operation for other commands like `AES`, `KDF`, etc. Some commands can write to either the upper or the lower 32 bytes of the TempKey buffer.

1.2.2 Random Number Generator

The ATECC608B includes an enhanced high-quality cryptographic RNG, implemented by using a combination of non-deterministic noise (entropy) source (NRBG) and seeding a deterministic algorithm (DRBG) implemented according to the National Institute of Standards and Technology (NIST) standards. The NRBG is used in the instantiation and each time an RNG number is required.

1.2.3 Low Frequency I^2C Idle Issue

The ATECC508A has an error in the I^2C circuitry, where the device may respond incorrectly under the following conditions:

- Multiple I^2C devices are on the same bus as the ATECC508A.
- The ATECC508A device is in Idle mode.
- The I^2C frequency of operation is ≤ 300 kHz.
- A data pattern from other devices on the I^2C bus could be interpreted by the ATECC508A as a wake pulse.

Under the above conditions, the ATECC508A wakes up and may corrupt data being sent to other devices on the bus. Whether or not data are corrupted depends on the frequency of operation and the actual data being sent.

This issue has been corrected for the ATECC608B device by modifying the I^2C circuitry to eliminate this issue. Note that the ATECC608B may still wake up at low frequencies but it will not respond or cause data corruption.

1.2.4 Device Revision

The package marking on Microchip security devices does not identify the device type. Therefore, the package marking cannot be used to identify the ATECC608B device. The only way to identify the device is through use of the device revision. The hardware device revision can be read by using the Revision mode (0x00) of the `Info` command. The output response of the `Info` command for each device is as follows:

Device	`Info` Command Revision Mode Response[2]
ATECC508A	0x00 0x00 0x50 0x00
ATECC608B	0x00 0x00 0x60 0x03[1]

Notes:

1. The value of the fourth byte may change over time, but it is 0x03 at the time of the initial product release.
2. The value of the Revision mode response is not the same as the 4-byte RevNum (Bytes[4:7]) in the device configuration zone. Only the Revision mode response can be used for device identification.

1.3 Unsupported Features

The following sections detail the features that have been removed from the ATECC508A. While there is no ability to directly replace these features, some of them can be implemented in a slightly different way. Details are provided in the following sections for each feature removed from the device. For an alternate method to implement some of these features, see **Section 4.3 Migrating Applications with Unsupported Features**.

1.3.1 OTP Consumption Mode

The EEPROM One-Time-Programmable (OTP) Consumption mode has been eliminated from the ATECC608B. After the device configuration zone is locked, no change to the OTP zone is allowed. Only reading of the OTP zone data is allowed.

1.3.2 LastKeyUse

The LastKeyUse functionality for key 15 has been eliminated. Slot 15 of the ATECC608B has the same functionalities as other slots and can no longer support a limited use key through the LastKeyUse functionality.

1.3.3 Selector Byte

The functionality to select a device from multiple devices sharing the same medium, when operating in Single-Wire Interface (SWI) mode using the selector byte, has been removed.

2. Command Differences

The following section describes the various differences in the commands available for the ATECC608B, compared to the ATECC508A. This includes new commands, updated commands and commands that are no longer supported for this device.

2.1 New Commands

2.1.1 `SecureBoot` Command

The `SecureBoot` command verifies the user application code during booting. This command supports three modes:

Full Mode: The signature and the digest are passed to the ATECC608B. The public key in the slot verifies the sent signature and digest. The response may be a Boolean or a MAC, depending on the `SecureBoot` command.

FullStore Mode: In FullStore mode, the digest or the signature is stored in the slot. If the digest is stored in the slot, it is sent to the device for verification. If the signature is stored in the slot, the digest is transmitted to the device, which verifies it with the stored signature and the public key.

FullCopy Mode: This mode is run when the secure boot code updates the user application. Both the digest and the signature are sent to the device, which verifies them with the stored public key. Once the command is executed successfully, either the digest or the signature is copied to the slot, depending on the secure boot settings in the configuration zone.

In a scenario where wire(s) protection is needed, the command has the option to inform the device that the encrypted digest is sent. In this case, the digest is encrypted using the I/O protection key and TempKey. The value returned from the device is either the validating MAC or the status code based on the selection of the digest encryption. When the encrypted digest is sent, the MAC is returned from the device. The host also calculates the MAC using the I/O protection key, the nonce and the digest, and verifies the returned MAC. If the mode is FullStore Signature, the signature is also included for calculating the MAC, and the host verifies the returned MAC. The command has the option to prohibit the secure boot function until the next power cycle.

2.1.2 `SelfTest` Command

The `SelfTest` command is used for testing cryptographic engines like AES, SHA, ECDH, ECDSA Verify, Sign and RNG. This command has different modes that help in testing the individual cryptographic engines separately or they can be combined. The status returned from the device gives the individual cryptographic engine test results.

2.1.3 `AES` Command

The `AES` command supports a 128-bit Advanced Encryption Standard - Electronic Code Book (AES- ECB) encryption, AES-ECB decryption and calculates the GFM of the input data. An operation for encryption and decryption is performed for 16 bytes at a time.

This command supports the selection of a 16-byte AES key, which can be taken from any of the below sources:

- TempKey – A feature used to select one of the 16 bytes as a key from TempKey
- Data Slot – A feature used to select one of the 16 bytes as a key from a data slot

The value returned from the device is the encrypted/decrypted data, GFM data or an error code.

2.1.4 `KDF` Command

The `KDF` command is used to generate the KDF key from the premaster secret key and the input data.

The command supports three modes for creating the KDF key:

- AES – This mode selects the source of the 16-byte key location.

- PRF – This mode selects the length of the source key, Authenticated Encryption with Associated Data (AEAD). It also selects the length of the target key to be generated.
- HKDF – This mode provides the flexibility to select the source location input data and the zero key. There is an IV Special Function in HKDF that compares the strings of the input data with the predefined string in the configuration zone and generates the KDF key once they match.

The command selects the source location of the source key and can select the target KDF key location. This additional feature provides more security without the KDF key being returned to the device. The source and the target key location can be the EEPROM slot, TempKey or Alternate Key Buffer. The command also provides the option to send the KDF key in plain text or encrypted text to the host. The host decrypts the encrypted KDF key using the I/O protection key and nonce.

Depending on the mode, the return value from the command is either the plain/encrypted KDF key or the return status code. If the encrypted KDF key is returned, a random nonce is also returned for decrypting the KDF key in the host.

2.2 Updated Commands

2.2.1 `ECDH` Command

The `ECDH` command has been updated to allow the selection of the source private key location and target the premaster secret key location. The two possible sources for the private key location are the TempKey and the EEPROM key slot. The target premaster key location can have any of the following locations: output buffer, EEPROM or TempKey.

When the Encrypted mode is selected by the `ECDH` command, the output premaster secret is encrypted using the I/O protection key.

2.2.2 `GenKey` Command

The `GenKey` command supports a new private key generation to TempKey and the resulting private key is used only by the `ECDH` command. When the private key is stored in TempKey, it frees the slot for other uses. The generated private key is used for the premaster secret key generation.

2.2.3 `Info` Command

The `Info` command is updated to set and reset the state of the Persistent Latch. This command helps to read the current state of the Persistent Latch.

2.2.4 `Nonce` Command

The `Nonce` command allows for the input data to be stored in any of the following buffers: TempKey buffer, Message Digest buffer or Alternate Key buffer. The `Nonce` command also allows up to 64 bytes to be passed into the TempKey or the Message Digest buffer when in PassThrough mode.

2.2.5 `SHA` Command

The `SHA` command supports write and read context switching. This allows for multiple SHA digests to be calculated concurrently. The SHA mode is updated to support variable length data compared to earlier, fixed 64-byte data. The output of the command is directed to any of the following locations: output buffer and TempKey, output buffer and Message Digest buffer or output buffer only.

2.2.6 `Sign` Command

In addition to signing the message in TempKey, the `Sign` command provides the message in the Message Digest buffer for signing the data, freeing the TempKey for other operations.

2.2.7 `Verify` Command

In addition to verifying the message in TempKey, the `Verify` command provides the message in the Message Digest buffer for verifying the data, freeing the TempKey for other operations. It has an additional mode to send the MAC from the device to the host, where the MAC is calculated from the I/O protection key.

2.3 Unsupported Commands

2.3.1 `Pause` Command

For the ATECC508A, the `Pause` command is useful when using multiple devices on the SWI interface. This allows the ATECC508A to select only the device that matches the selector byte and to use it for further communication, while all the other devices in the same shared medium enter the Idle mode. The selector byte functionality has been removed from the ATECC608B.

2.3.2 `HMAC` Command

While the `HMAC` command no longer exists for the ATECC608B, the HMAC calculation can still be performed. The ATECC608B provides the feature for calculating the HMAC value using the `SHA` command. For both ATECC608B and ATECC508A, the resulting HMAC value from using the `SHA` command always matches. However, the ATECC608B HMAC value calculated using the `SHA` command does not match the HMAC value calculated using the `HMAC` command in the ATECC508A.

3. Configuration Zone Updates

Table 3-1 lists the new fields added in the ATECC608B configuration zone. It also describes the differences between the two devices.

Table 3-1. Configuration Zone Updates

Byte	ATECC608B	ATECC508A
13	AES_Enable – This byte enables/disables the AES functionalities for both AES and KDF commands.	Reserved for future use.
18	CountMatch – This byte enables/disables the CountMatch function and selects the slot to be used as the counter match key.	OTP mode – Used to set Read-Only or Consumption mode to the OTP zone.
19	The Chip mode has been redefined. The new byte helps to reduce the power consumption of the device with three possible power modes. It also selects the source of the I^2C address, either from the I2C_Address or the UserExtraAdd byte.	Chip mode
68	UseLock – This new byte controls the transport lock functionality. It enables/disables the transport lock function and the slot to be used as the transport key.	LastKeyUse (16 bytes) – This field controls the KeyID 15 limited-use functionality.
69	VolatileKeyPermission – This new byte enables/disables the volatile key functionality and selects the volatile key slot for volatile key functionalities.	
70-71	SecureBoot – This new byte configures the secure boot functionalities: • Selection of one of the Secure Boot modes. • Whether to set the Persistent Latch on a successfully `Secure Boot` command execution. • The slot to be used for digest/signature. • The slot to be used for public key. • The RNG to be used for the `Secure Boot` command.	
72	kdfIvLoc – Index within the KDF (HKDF) input string, where the two bytes stored below (KdfIvStr) are located.	
73	KdfIvStr – 2-byte KDF IV string that must be found in the KDF message for the KDF (HKDF) Special IV mode.	
85	UserExtraAdd – If nonzero, it is the I^2C address this device will respond to on the bus.	Selector byte – It selects which device will remain in Active mode after the execution of the `Pause` command.
90	ChipOptions The new byte provides the following features: • Whether to run the self-test automatically on power-on or wake-up. • Enables/disables the I/O protection key. • Enables/disables the KDF AES function. • Sets the ECDH and KDF protection functionality. • The slot to be used for the I/O protection key.	Reserved for future use.
96-127	KeyConfig – In KeyType, two new types (AES, SHA) and the function to enable the key based on the state of the Persistent Latch were added.	KeyConfig

4. Migration from the ATECC508A to the ATECC608B

In most cases, the migration from the ATECC508A to the ATECC608B is straightforward and uncomplicated. When migrating, several factors need to be considered:

1. Package and Pinout – All packages that are supported for the ATECC508A continue to be supported for the ATECC608B. This includes the 8-pad UDFN, 8-pin SOIC and 3-pin RBH contact package. Pinouts for each of these package are consistent between the devices.
2. Voltage and Temperature Ranges – Both devices are specified over the same operating supply voltage, 2.0V to 5.5V, and industrial temperature range, 0°C to 85°C. No issues exist over this range.
3. Configuration – A review of the configuration zone needs to be undertaken to determine if a design can be ported with minimal changes or if a change to the application code is required. A more detailed list of considerations is provided in **Section 4.1 Configuration Migration Considerations**.
4. Timing Differences – Significant timing differences exist between the ATECC508A and the ATECC608B. The difficulty of migrating to the new devices depends on the commands utilized and whether fixed timing or polled timing was implemented. For more information, see **Section 4.2 Timing Migration Considerations**.

4.1 Configuration Migration Considerations

To allow the ATECC608B to operate similarly to the ATECC508A, the configuration zone changes shown in Table 4-1 must be made. Note that this configuration does not take advantage of the new features or commands associated with the ATECC608B.

Table 4-1. ATECC508A to ATECC608B Migration

Byte	ATECC608B	ATECC508A
18	CountMatch – 0x00	OTP mode • 0xAA – Read-Only mode • 0x55 – Consumption mode (Note) • All other values are reserved
19	Chip mode – Bits 3-7 of the byte must be '0'.	Chip mode
68	UseLock – 0x00	LastKeyUse (Note) – generally initialized to 0xFF.
69	VolatileKey permission – 0x00	
70-71	SecureBoot – 0x0000	
72	kdfIvLoc – 0x00	
73	KdfIvStr – 0x00	
85	UserExtraAdd – 0x00	Selector byte (Note) – any value depending on the device configured for the `Pause` command.
90	ChipOptions – 0x00	Reserved for future use. 0x00

Important: If this mode is used on the ATECC508A, some application redefinition may be required for the implementation on the ATECC608B.

4.2 Timing Migration Considerations

The previous sections describe all the differences in features and commands for the ATECC608B compared to the ATECC508A. One additional factor that needs to be considered is if the timing differences between the ATECC508A and the ATECC608B matter for a specific design. The timing differences between the two devices are quite significant for many commands. For a detailed comparison of the differences, it is recommended that a comparison of the two data sheets be undertaken.

The difficulty in migrating from the ATECC508A to the ATECC608B depends on how the software was implemented. There are two cases that require consideration:

Fixed Timing Implementation

If the code is written assuming hardwired timing parameters, careful analysis must be undertaken to evaluate the impact of changing from the ATECC508A to the ATECC608B. Under this method, after a command has been issued, the microcontroller waits a fixed period of time before reading the response data back. If the delay required for the ATECC608B is significantly longer than that of the ATECC508A, this command may fail. Using an older version of CryptoAuthLib meant for the ATECC508A or a customer-generated library with the ATECC608B could cause some timing errors. Implementing the latest version of CryptoAuthLib updates the timing information correctly and, through just recompiling the code and reflashing the micro, correcting the timing issues.

If timing is an issue, the following solutions can be considered:

1. Migrate the code to use the latest version of the CryptoAuthLib library.
2. Migrate the code to use polled timing. For more information, see **Section 4.2 Polled Timing Implementation**.
3. If a custom library with fixed timing is used, update the library timing parameters needed for the ATECC608B.
4. Implement redundancy by trying to read back data a second time upon receiving a failure code that indicates the response is not yet ready.

Polled Timing Implementation

If the code was written using polling, there will be no issues with migrating to the ATECC608B. Under this scenario, the microcontroller polls the ATECC608B to determine when data are available to be read back. Most timing differences are absorbed by the polling command.

4.3 Migrating Applications with Unsupported Features

If any of the unsupported features of the ATECC508A are implemented in an application, some changes will be required to the application code in order to use the ATECC608B. The following sections describe possible alternate methods to implement these features.

OTP Consumption Mode

If the OTP Consumption mode was used in an ATECC508A design, it cannot be directly implemented by the ATECC608B. However, the capability can be implemented in an alternate method, through the use of the monotonic counters.

If the monotonic counters are not used, one of them can be configured to replicate the OTP Consumption mode. The number of bits set to '1' in the OTP zone must be converted into the equivalent count value for the monotonic counter. This value would be provisioned as the initial counter value. While any monotonic counter can be used for this purpose, monotonic counter 1 is recommended, as monotonic counter 0 could be connected to a key slot and used to limit key usage.

LastKeyUse

The LastKeyUse functionality was only implemented on slot 15 of the ATECC508A. An alternate method to implement this capability can be enabled on this slot through the use of the SlotConfig.LimitedUse bit and a monotonic counter.

To replicate the functionality to be as close as possible to that of the ATECC508A, the count value of the monotonic counter needs to be set to replicate the count implemented on the ATECC508A design, using the LastKeyUse field.

Important: If another slot contains a key that was previously using the limited key use functionality, implementing a limited use on slot 15 may not be feasible.

Selector Byte

The selector byte functionality was only available in the SWI mode of the ATECC508A. There is no capability within the ATECC608B to replicate or emulate this functionality.

4.4 I²C Low-Frequency ATECC608B Migration

Migrating an ATECC508A design that has to deal with the low-frequency I²C issue requires no changes to either hardware or firmware. The changes implemented for a correct operation with the ATECC508A will not cause an issue with the fixed ATECC608B.

The user must consider if the operation of the system is better served by backing out the firmware changes implemented to correct the ATECC508A issues. Removing these changes would most likely result in reduced firmware size and improved system performance. Whether these are reasons valuable enough to modify the working code is up to the implementer.

5. Conclusion

The form, fit and function of the ATECC608B are compatible with those of the ATECC508A. Device pinouts for all supported packages and voltage operating ranges are identical. The ATECC608B supports the standard industrial temperature range that the ATECC508A supports, but it also provides an extended temperature range of up to 100°C.

The functionality of the ATECC608B is largely a superset of the ATECC508A, with the exception of only a few commands. There are a few configuration zone bytes that must be changed in order to achieve compatible operation. While the timing differences are significant, they can be readily overcome in most scenarios. If polling was implemented, the timing differences will be relatively transparent.

The changes implemented for the ATECC608B were primarily done to enhance device security and are largely transparent to the user. For new system designs and a refresh of the existing systems, it is strongly recommended to use the ATECC608B as a way to enhance overall system security. The ATECC608B also provides its users with a chance to implement some enhanced functional security features to improve their overall system security and performance.

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ATECC508A-MAH1Q-T
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ATECC508A-MAHJ4-S
ATECC508A-MAHPH-T
ATECC508A-MAHQA-T
ATECC508A-MAHT1-T
ATECC508A-MAH1A-S
ATECC508A-MAH1B-S
ATECC508A-MAH1C-S
ATECC508A-MAH1Q-S
ATECC508A-MAH2F-S
ATECC508A-MAH3A-S
ATECC508A-MAH3B-S
ATECC508A-MAHGF-S
ATECC508A-MAHPH-S
ATECC508A-MAHQA-S
ATECC508A-MAHT1-S
ATECC608A-SSHMD-B
ATECC608A-SSHDA-B
ATECC608A-SSHCZ-B
ATECC608A-SSHHL-B
ATECC608A-MAHMD-B
ATECC608A-MAHA2-B
ATECC608A-MAHT2-B
ATECC608A-W07CZ-T
ATECC608A-W07DA-T
ATECC608A-SSHDA-T
ATECC608A-SSHCZ-T
ATECC608A-SSHHL-T
ATECC608A-SSH4P-T
ATECC608A-SSH4N-T
ATECC608A-SSH2P-T
ATECC608A-SSH3M-T
ATECC608A-MAHZN-S
ATECC608A-MAHDA-S
ATECC608A-MAHDA-T
ATECC608A-MAHCZ-S

ATECC608A-MAHCZ-T
ATECC608A-MAHHL-S
ATECC608A-MAHHL-T
ATECC608A-MAHA2-S
ATECC608A-MAH22-T
ATECC608A-MAHTN-T
ATECC608A-MAH1G-T
ATECC608A-MAH1W-T
ATECC608A-MAH2B-T
ATECC608A-MAH2G-T
ATECC608A-MAHAV-T
ATECC608A-MAHGX-T
ATECC608A-MAHLG-T
ATECC608A-MAH1G-S
ATECC608A-MAH1H-S
ATECC608A-MAH1K-S
ATECC608A-MAH1U-S
ATECC608A-MAH2G-S
ATECC608A-MAH2K-S
ATECC608A-MAH2M-S
ATECC608A-MAH2U-S
ATECC608A-MAH2V-S
ATECC608A-MAH2X-S
ATECC608A-MAH2Y-S
ATECC608A-MAH3Q-S
ATECC608A-MAHAA-S
ATECC608A-MAHAC-S
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ATECC608A-MAHGP-S
ATECC608A-MAHGX-S
ATECC608A-MAHLG-S
ATECC608A-MAH1H-T
ATECC608A-MAH2U-T
ATECC608A-MAH3J-T
ATECC608A-MAH3P-T
ATECC608A-MAH4K-T
ATECC608A-MAHAP-T
ATECC608A-MAHGP-T
ATECC608A-MAHVL-T
ATECC608A-MAHVM-T
ATECC508A-W07ZJ-F
ATECC508A-WWS8DA
ATECC508A-SSHDA-B
ATECC508A-SSHCZ-B
ATECC508A-SSHHL-B
ATECC508A-SSHRA-B
ATECC508A-SSHMT-B

ATECC508A-SSH1P-T
ATECC508A-RBHCZ-B
ATECC508A-RBHZB-B
ATECC508A-SSHDA-T
ATECC508A-SSHCZ-T
ATECC508A-SSHHL-T
ATECC508A-SSHRA-T
ATECC508A-SSHMT-T
ATECC508A-SSHZC-T
ATECC508A-SSHZJ-T
ATECC508A-SSHAW-T
ATECC508A-SSHWA-T
ATECC508A-SSHC9-T
ATECC508A-SSH1F-T
ATECC508A-SSH1M-T
ATECC508A-SSHC6-T
ATECC508A-SSH1L-T
ATECC508A-RBHCZ-T
ATECC508A-RBHZB-T
ATECC508A-MAHDA-T
ATECC508A-MAHCZ-T
ATECC508A-MAHWF-T
ATECC508A-MAHHL-T
ATECC508A-MAHDA-S
ATECC508A-MAHCZ-S
ATECC508A-MAHHL-S
ATECC508A-MAHKN-T
ATECC508A-MAHZA-T
ATECC508A-MAHZC-T
ATECC508A-MAHZG-S
ATECC508A-MAHZA-S
ATECC508A-MAHZC-S
ATECC508A-MAHUW-T
ATECC508A-MAHUX-T
ATECC508A-MAHUZ-T
ATECC508A-MAHZK-T
ATECC508A-MAHZK-S
ATECC508A-MAHSM-T
ATECC508A-MAHSM-S
ATECC508A-MAHAW-S
ATECC508A-MAHKN-S
ATECC508A-MAHWS-T
ATECC508A-MAHWS-S

RMES-20NCGX846-Memo # ML102020003S Information Notice: Introduction of new ATECC608B device family available in 3L CONTACT,8L UDFN and 8L SOIC packages as replacement to an existing ATECC508A and ATECC608A device families.

Affected Catalog Part Number

PCN_RMES-20NCGX846	
Affected_CPN	**New products availability date**
ATECC508A-W07ZJ-F	Not applicable
ATECC508A-WWS8DA	Not applicable
ATECC508A-SSHDA-B	October 31, 2020
ATECC508A-SSHCZ-B	October 31, 2020
ATECC508A-SSHHL-B	October 31, 2020
ATECC508A-SSHRA-B	October 31, 2020
ATECC508A-SSHMT-B	October 31, 2020
ATECC508A-SSH1P-T	October 31, 2020
ATECC508A-RBHCZ-B	October 20, 2020
ATECC508A-RBHZB-B	October 20, 2020
ATECC508A-SSHDA-T	October 31, 2020
ATECC508A-SSHCZ-T	October 31, 2020
ATECC508A-SSHHL-T	October 31, 2020
ATECC508A-SSHRA-T	October 31, 2020
ATECC508A-SSHMT-T	October 31, 2020
ATECC508A-SSHZC-T	October 31, 2020
ATECC508A-SSHZJ-T	October 31, 2020
ATECC508A-SSHAW-T	October 31, 2020
ATECC508A-SSHWA-T	October 31, 2020
ATECC508A-SSHC9-T	October 31, 2020
ATECC508A-SSH1F-T	October 31, 2020
ATECC508A-SSH1M-T	October 31, 2020
ATECC508A-SSH1P-T	October 31, 2020
ATECC508A-SSHC6-T	October 31, 2020
ATECC508A-SSH1L-T	October 31, 2020
ATECC508A-RBHCZ-T	October 20, 2020
ATECC508A-RBHZB-T	October 20, 2020
ATECC508A-MAHDA-T	October 20, 2020
ATECC508A-MAHCZ-T	October 20, 2020
ATECC508A-MAHWF-T	October 20, 2020
ATECC508A-MAHHL-T	October 20, 2020
ATECC508A-MAHDA-S	October 20, 2020
ATECC508A-MAHCZ-S	October 20, 2020
ATECC508A-MAHHL-S	October 20, 2020
ATECC508A-MAHKN-T	October 20, 2020
ATECC508A-MAHZA-T	October 20, 2020
ATECC508A-MAHZC-T	October 20, 2020
ATECC508A-MAHZG-S	October 20, 2020
ATECC508A-MAHZA-S	October 20, 2020
ATECC508A-MAHZC-S	October 20, 2020
ATECC508A-MAHUW-T	October 20, 2020
ATECC508A-MAHUX-T	October 20, 2020
ATECC508A-MAHUZ-T	October 20, 2020
ATECC508A-MAHZK-T	October 20, 2020

RMES-20NCGX846-Memo # ML102020003S Information Notice: Introduction of new ATECC608B device family available in 3L CONTACT,8L UDFN and 8L SOIC packages as replacement to an existing ATECC508A and ATECC608A device families.

Affected Catalog Part Number

PCN_RMES-20NCGX846	
Affected_CPN	**New products availability date**
ATECC508A-MAHZK-S	October 20, 2020
ATECC508A-MAHSM-T	October 20, 2020
ATECC508A-MAHSM-S	October 20, 2020
ATECC508A-MAHAW-S	October 20, 2020
ATECC508A-MAHKN-S	October 20, 2020
ATECC508A-MAHWS-T	October 20, 2020
ATECC508A-MAHWS-S	October 20, 2020
ATECC508A-MAHWW-S	October 20, 2020
ATECC508A-MAHWW-T	October 20, 2020
ATECC508A-MAH1A-T	October 20, 2020
ATECC508A-MAH1B-T	October 20, 2020
ATECC508A-MAH1C-T	October 20, 2020
ATECC508A-MAH1Q-T	October 20, 2020
ATECC508A-MAH2E-T	October 20, 2020
ATECC508A-MAH3A-T	October 20, 2020
ATECC508A-MAH3B-T	October 20, 2020
ATECC508A-MAHGF-T	October 20, 2020
ATECC508A-MAHJ4-T	October 20, 2020
ATECC508A-MAHJ4-S	October 20, 2020
ATECC508A-MAHPH-T	October 20, 2020
ATECC508A-MAHQA-T	October 20, 2020
ATECC508A-MAHT1-T	October 20, 2020
ATECC508A-MAH1A-S	October 20, 2020
ATECC508A-MAH1B-S	October 20, 2020
ATECC508A-MAH1C-S	October 20, 2020
ATECC508A-MAH1Q-S	October 20, 2020
ATECC508A-MAH2F-S	October 20, 2020
ATECC508A-MAH3A-S	October 20, 2020
ATECC508A-MAH3B-S	October 20, 2020
ATECC508A-MAHGF-S	October 20, 2020
ATECC508A-MAHPH-S	October 20, 2020
ATECC508A-MAHQA-S	October 20, 2020
ATECC508A-MAHT1-S	October 20, 2020
ATECC608A-SSHMD-B	October 31, 2020
ATECC608A-SSHDA-B	October 31, 2020
ATECC608A-SSHCZ-B	October 31, 2020
ATECC608A-SSHHL-B	October 31, 2020
ATECC608A-MAHMD-B	October 20, 2020
ATECC608A-MAHA2-B	October 20, 2020
ATECC608A-MAHT2-B	October 20, 2020
ATECC608A-W07CZ-T	Not applicable
ATECC608A-W07DA-T	Not applicable
ATECC608A-SSHDA-T	October 31, 2020
ATECC608A-SSHCZ-T	October 31, 2020

RMES-20NCGX846-Memo # ML102020003S Information Notice: Introduction of new ATECC608B device family available in 3L CONTACT,8L UDFN and 8L SOIC packages as replacement to an existing ATECC508A and ATECC608A device families.

Affected Catalog Part Number

PCN_RMES-20NCGX846	
Affected_CPN	**New products availability date**
ATECC608A-SSHHL-T	October 31, 2020
ATECC608A-SSH4P-T	October 31, 2020
ATECC608A-SSH4N-T	October 31, 2020
ATECC608A-SSH2P-T	October 31, 2020
ATECC608A-SSH3M-T	October 31, 2020
ATECC608A-MAHZN-S	October 20, 2020
ATECC608A-MAHDA-S	October 20, 2020
ATECC608A-MAHDA-T	October 20, 2020
ATECC608A-MAHCZ-S	October 20, 2020
ATECC608A-MAHCZ-T	October 20, 2020
ATECC608A-MAHHL-S	October 20, 2020
ATECC608A-MAHHL-T	October 20, 2020
ATECC608A-MAHA2-S	October 20, 2020
ATECC608A-MAH22-T	October 20, 2020
ATECC608A-MAHTN-T	October 20, 2020
ATECC608A-MAH1G-T	October 20, 2020
ATECC608A-MAH1W-T	October 20, 2020
ATECC608A-MAH2B-T	October 20, 2020
ATECC608A-MAH2G-T	October 20, 2020
ATECC608A-MAHAV-T	October 20, 2020
ATECC608A-MAHGX-T	October 20, 2020
ATECC608A-MAHLG-T	October 20, 2020
ATECC608A-MAH1G-S	October 20, 2020
ATECC608A-MAH1H-S	October 20, 2020
ATECC608A-MAH1K-S	October 20, 2020
ATECC608A-MAH1U-S	October 20, 2020
ATECC608A-MAH2G-S	October 20, 2020
ATECC608A-MAH2K-S	October 20, 2020
ATECC608A-MAH2M-S	October 20, 2020
ATECC608A-MAH2U-S	October 20, 2020
ATECC608A-MAH2V-S	October 20, 2020
ATECC608A-MAH2X-S	October 20, 2020
ATECC608A-MAH2Y-S	October 20, 2020
ATECC608A-MAH3Q-S	October 20, 2020
ATECC608A-MAHAA-S	October 20, 2020
ATECC608A-MAHAC-S	October 20, 2020
ATECC608A-MAHAP-S	October 20, 2020
ATECC608A-MAHAV-S	October 20, 2020
ATECC608A-MAHD3-S	October 20, 2020
ATECC608A-MAHGP-S	October 20, 2020
ATECC608A-MAHGX-S	October 20, 2020
ATECC608A-MAHLG-S	October 20, 2020
ATECC608A-MAH1H-T	October 20, 2020
ATECC608A-MAH2U-T	October 20, 2020

RMES-20NCGX846-Memo # ML102020003S Information Notice: Introduction of new ATECC608B device family available in 3L CONTACT,8L UDFN and 8L SOIC packages as replacement to an existing ATECC508A and ATECC608A device families.

Affected Catalog Part Number

PCN_RMES-20NCGX846	
Affected_CPN	**New products availability date**
ATECC608A-MAH3J-T	October 20, 2020
ATECC608A-MAH3P-T	October 20, 2020
ATECC608A-MAH4K-T	October 20, 2020
ATECC608A-MAHAP-T	October 20, 2020
ATECC608A-MAHGP-T	October 20, 2020
ATECC608A-MAHVL-T	October 20, 2020
ATECC608A-MAHVM-T	October 20, 2020