



Product Change Notification / SYST-30IWCH812

Date:

02-Oct-2020

Product Category:

PoE PD

PCN Type:

Document Change

Notification Subject:

Data Sheet - PD70224 Datasheet Document Revision

Affected CPNs:

[SYST-30IWCH812_Affected_CPN_10022020.pdf](#)

[SYST-30IWCH812_Affected_CPN_10022020.csv](#)

Notification Text:

SYST-30IWCH812

Microchip has released a new Product Documents for the PD70224 Datasheet of devices. If you are using one of these devices please read the document located at [PD70224 Datasheet](#).

Notification Status: Final

Description of Change:

- 1) Updated a typo for a value of K in the Package Measurements table
- 2) Updated the Introduction section.
- 3) Added Technical Support and Documentation section.
- 4) Updated the values of K in the Package Measurements table.
- 5) Updated the Internal Construction and Pinout figure.
- 6) Updated the 4.3 Recommended PCB Layout section.
- 7) Updated the PD70224 EVB PCB Silk Top figure.
- 8) Updated the Ordering Information table.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 02 Oct 2020

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

[PD70224 Datasheet](#)

Please contact your local [Microchip sales office](#) with questions or concerns regarding this notification.

Terms and Conditions:

If you wish to receive Microchip PCNs via email please register for our PCN email service at our [PCN home page](#) select register then fill in the required fields. You will find instructions about registering for Microchips PCN email service in the [PCN FAQ](#) section.

If you wish to change your PCN profile, including opt out, please go to the [PCN home page](#) select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.

IdealBridge™ Dual MOSFET-Based Bridge Rectifier

Introduction

PD70224 is a dual pack of MOSFET-based full-bridge rectifiers. It contains low-RDS 0.16 Ω N-channel MOSFETs for much higher overall efficiency and higher output power, particularly when used in Powered Devices for Power over Ethernet (PoE) applications. The entire drive circuitry for driving the MOSFETs is on-chip, including a charge pump for driving the high-side N-channel MOSFETs. The total forward drop (bridge offset) introduced by the IdealBridge™ rectifier is only 192 mV at 0.6 A, compared to a standard bridge rectifier that typically presents 2000 mV of forward drop.

PD70224 IdealBridge™ can support over 2 A current, making it the ideal choice for IEEE®802.3bt (Type 3 and Type 4), IEEE 802.3af and IEEE 802.3af (Type 1 and Type 2). The PD70224 also supports legacy 4 pair standards such as UPoE (60 W) and POH (Power over HDBase-T, 95 W)..

In addition, PD70224 is capable of helping to identify at the physical layer itself whether a 2-pair PSE or a 4-pair PSE is providing power over the cable. It does that by sensing the voltage on the line (un-rectified) side of the pairs.

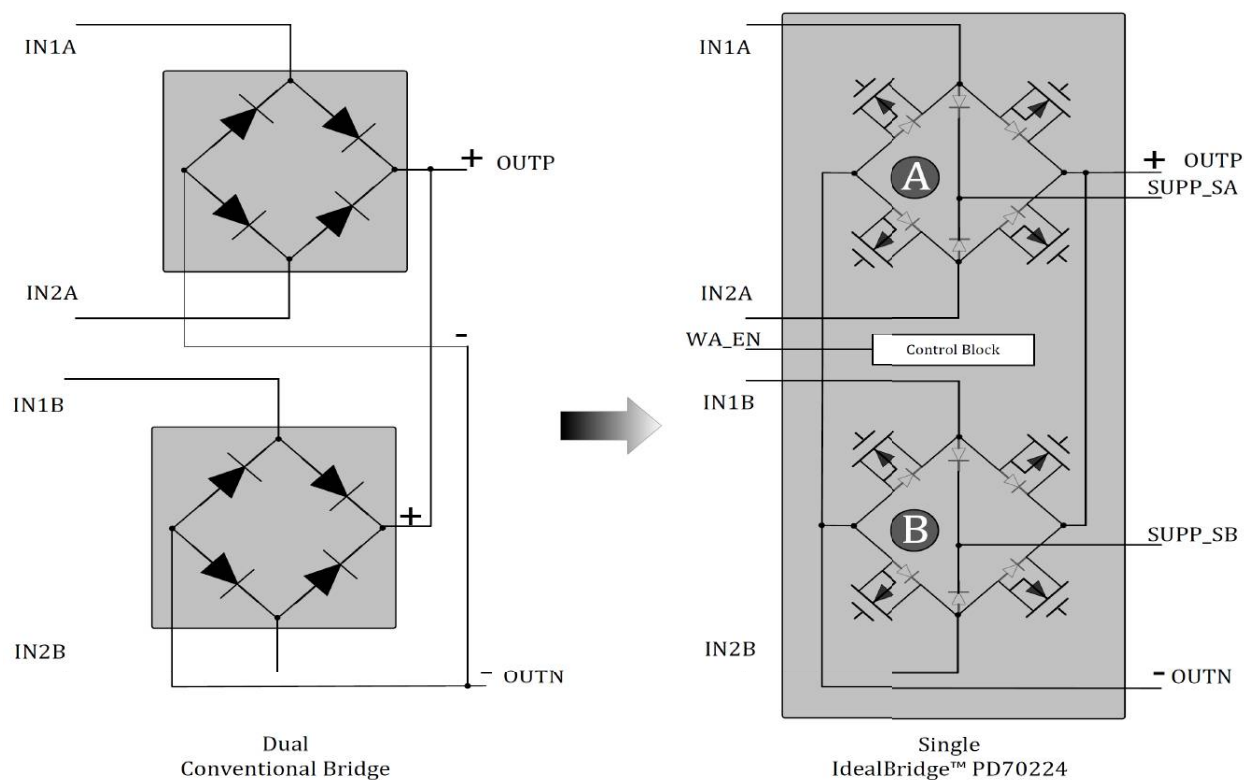
Features

- Active circuit with low forward-drop to replace dissipative passive diode bridges
- Self-contained drive circuitry for MOSFETs
- Designed to support IEEE 802.3af/at/bt, Universal PoE (UPOE), and Power over HDBase-T (PoH)
- Integrated 0.16 Ω N-Channel MOSFETs for 0.32 Ω total path resistance
- “Power present” indicator signals for identifying 4-pair bridge power
- Dedicated pin to implement adapter priority
- Low leakage, <10 μ A during detection
- Wide operating voltage range up to 57 V
- -40 °C to 85 °C ambient
- Available in 40-pin package
- MSL3, RoHS compliant

Applications

- Power over Ethernet IEEE 802.3bt/at/af
- Proprietary 4-pair standards, UPOE, and POH

Figure 1. Dual Conventional Bridge Versus Single Ideal Bridge



Technical Support and Documentation

For technical support visit the Microchip Technical Support Portal at: microchipsupport.force.com/s/.

For access to any related application note or documentation please consult your local Microchip Client Engagement Manager or visit our website at www.microchip.com/poe.

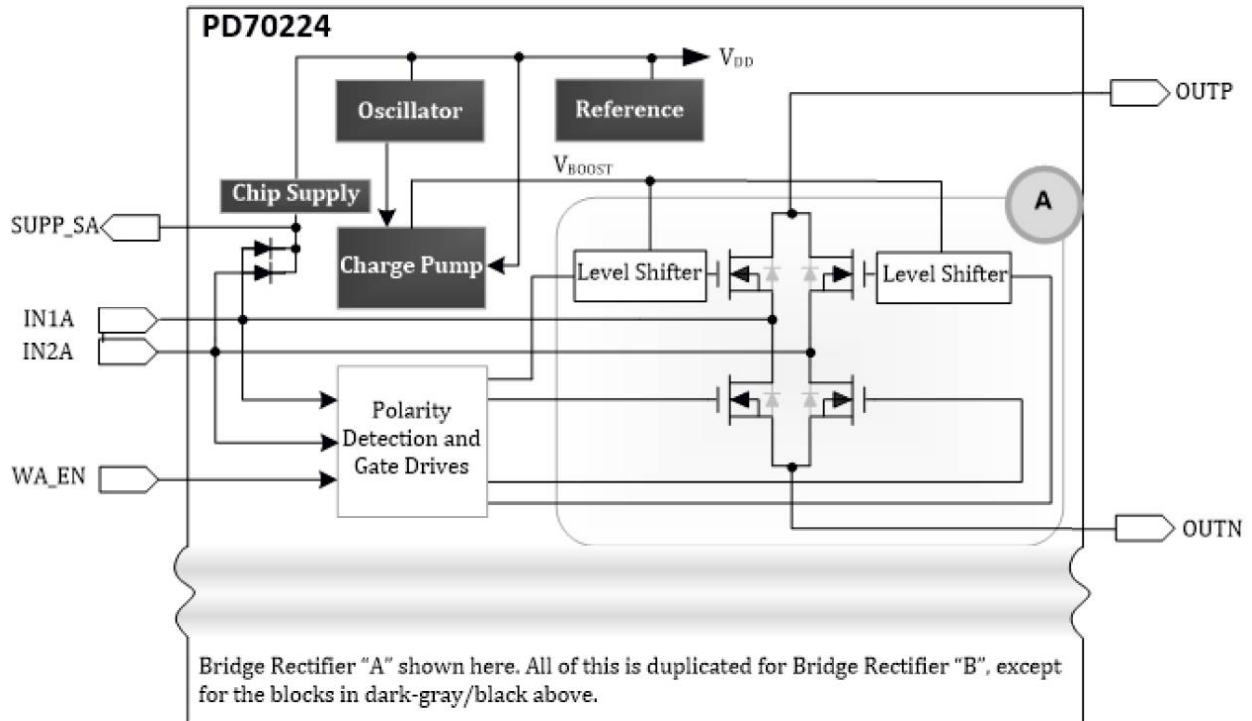
Table of Contents

Introduction.....	1
Features.....	1
Applications.....	1
Technical Support and Documentation.....	2
1. Functional Descriptions.....	4
1.1. Purpose of Charge Pump.....	5
1.2. Purpose and Use of Supply Pins.....	5
2. Electrical Specifications.....	6
2.1. Absolute Maximum Ratings.....	6
2.2. Operating Ratings.....	7
2.3. Electrical Characteristics.....	7
3. Pin Descriptions.....	10
4. Package Information.....	12
4.1. Package Outline Drawing.....	12
4.2. Thermal Specifications.....	13
4.3. Recommended PCB Layout.....	13
5. Application Information.....	16
5.1. Peripheral Devices.....	16
5.2. Operation with an External DC Source.....	16
6. Design Example.....	19
7. Ordering Information.....	21
8. Revision History.....	22
The Microchip Website.....	23
Product Change Notification Service.....	23
Customer Support.....	23
Microchip Devices Code Protection Feature.....	23
Legal Notice.....	23
Trademarks.....	24
Quality Management System.....	24
Worldwide Sales and Service.....	25

1. Functional Descriptions

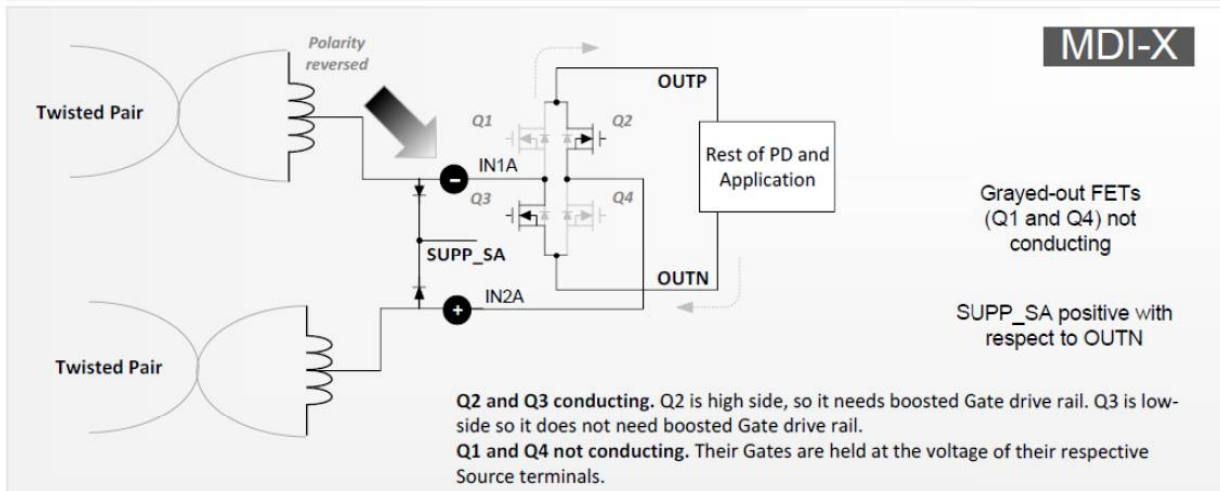
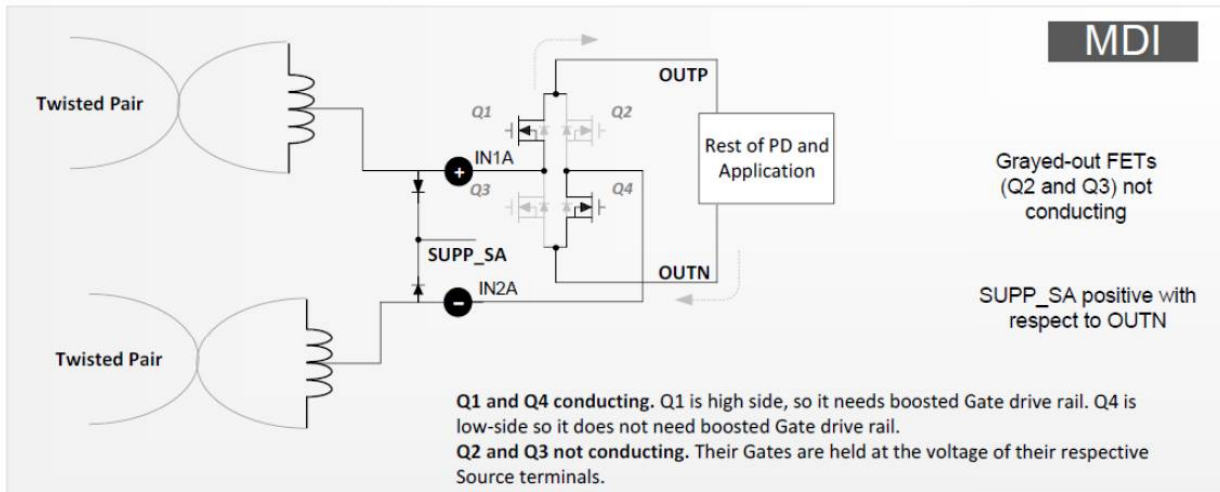
The following figure shows the functional blocks of PD70224.

Figure 1-1. Block Diagram



Bridge Rectifier "A" (powered with MDI or MDI-X)

The MOSFETs and active bridge circuitry is guaranteed to turn ON at a threshold set between 23.1V and 32V. Below that threshold, rectifier operation is through their body diodes only



1.1 Purpose of Charge Pump

In the case that follows, the FETs connected to OUTP (the "high-side" FETs) are the ones that require a boosted gate drive rail so they can be turned ON. The on-chip charge pump provides the boosted gate drive rail for the high-side FETs. The FETs connected to OUTN ("low-side" FETs) do not need a boosted drive rail to be turned ON.

1.2 Purpose and Use of Supply Pins

Since the twisted pair set is delivering power, in the following case, SUPP_SA is positive with respect to OUTN. But if these two twisted pairs were not connected to a PSE, SUPP_SA would be low. For a standard 2-pair or 4-pair PDs with two bridge rectifiers (4-pairs), one connected to the data pairs, the other to the spare pairs, the presence of high voltage on SUPP_SA and/or SUPP_SB will indicate whether the data pairs or spare pairs, or both, are connected to PSEs. So SUPP_SA and SUPP_SB will indicate whether the data pairs or spare pairs, or both, are connected to PSEs. So SUPP_SA and SUPP_SB can be used to indicate 2-pair or 4-pair PoE operation.

2. Electrical Specifications

The following section describes the electrical specifications of the device.

2.1 Absolute Maximum Ratings

Performance is not necessarily guaranteed over this entire range. These are maximum stress ratings only. Exceeding these ratings, even momentarily, can cause immediate damage, or negatively impact long-term operating reliability.

Table 2-1. Absolute Maximum Ratings

Parameter		Min	Max	Units
IN1A, IN1B, IN2A, IN2B to OUTN		−0.3	74	V
IN1A to IN2A		−0.3	74	V
IN1B to IN2B		−0.3	74	V
IN1A, IN1B, IN2A, IN2B to OUTP		−74		V
IN1A, IN2A to IN1B		−0.3	74	V
IN1A, IN2A to IN2B		−0.3	74	V
OUTP to OUTN		−0.3	74	V
OUTP to IN1A, IN1B, IN2A, IN2B		−0.3	74	V
SUPP_SA, SUPP_SB to OUTN		−0.3	74	V
WA_EN to OUTN		−0.3	5.5	V
I _{INA} , I _{INB} (currents through bridge A or B)			1.5	A
Junction temperature			150	°C
Lead soldering temperature (40 s, reflow)			260	°C
Storage temperature		−65	150	°C
ESD rating	HBM		±1250 ¹	V
	MM		±100	V
	CDM		±2000	V

1. All pins pass 1250 V, except IN1A and IN2A that pass 1000 V.

Note: EPAD1 is connected by copper plane on PCB to OUTP, and EPAD2 is similarly connected to OUTN. OUTN is ground for IC.

2.2 Operating Ratings

Performance is generally guaranteed over this range as provided under [Electrical Characteristics](#).

Table 2-2. Operating Ratings

Parameter	Min	Max	Units
IN1A, IN1B to OUTN		57	V
IN2A, IN2B to OUTN		57	V
WA_EN to OUTN	-0.3	5	V
Junction temperature	-40	125	°C
Port Current (I_{INx})	0	1.5	A

2.3 Electrical Characteristics

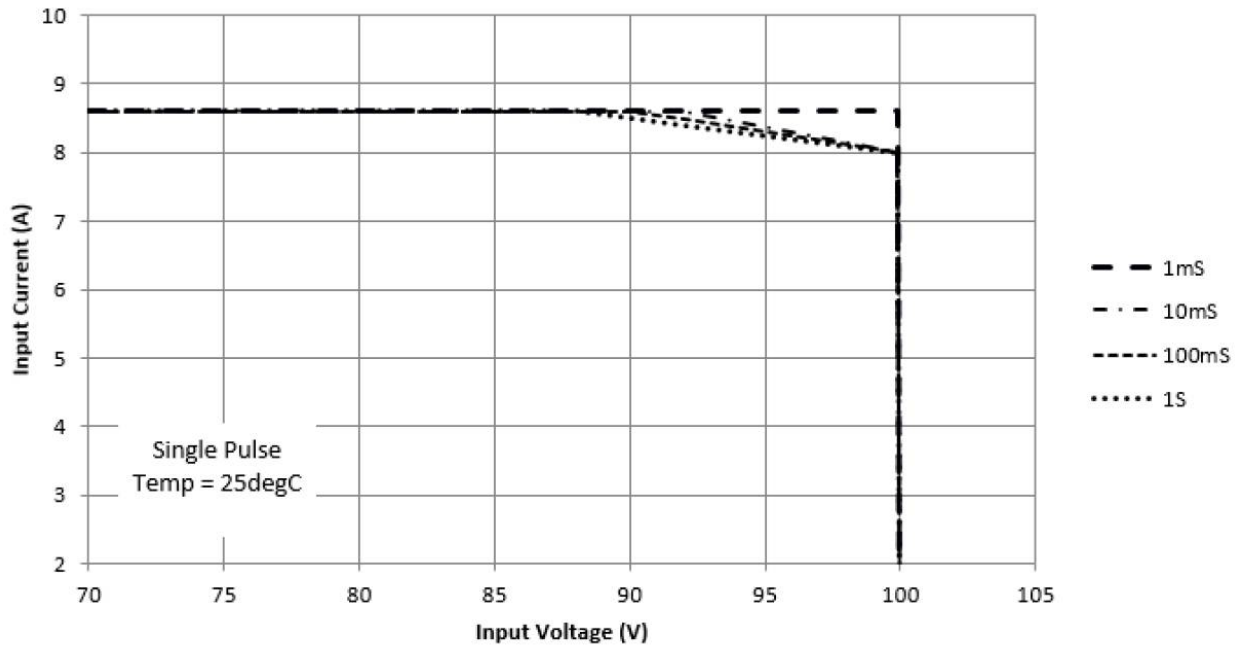
Unless otherwise specified under conditions, the Min and Max ratings stated below apply over the entire specified operating ratings of the device. Typ values stated are either by design or by production testing at 25 °C ambient.

Table 2-3. Typical Electrical Performance

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{INx}	Input Voltage for Bridge “x”, where x is “A” or “B”.				57	V
ΔI_Q	Differential Quiescent Current $I(V_{IN}=10.1\text{ V}) - I(V_{IN}=2.5\text{ V})$;	$2.5\text{ V} < V_{INx} < 10.1\text{ V}$; No load between OUTP and OUTN; No load on SUPP_Sx pins.		6	10	μA
I_Q	Quiescent Current (single bridge)	$10.2\text{ V} < V_{INx} < 23\text{ V}$; No load between OUTP & OUTN; No load on SUPP_Sx pins.			85	μA
	Quiescent Current (both bridge combined)	$V_{INx} = 55\text{ V}$; No load between OUTP & OUTN; No load on SUPP_Sx pins.			900	μA
V_{TURN_ON}	Active turn-on voltage of FETs		23.1	27.5	32	V
V_{HYST}	Turn-on voltage hysteresis			0.4		V
T_{ALT}	Alternate input voltage polarity – Delay time required ($V_{IN} = 0\text{ V}$) while alternating input voltage polarity.		200			ms
V_{OFFSET}	Bridge offset @ Off state	$V_{INx} < V_{TURN_ON}$, two body diodes in series $I_{INx} = 40\text{ mA}$			1.8	V

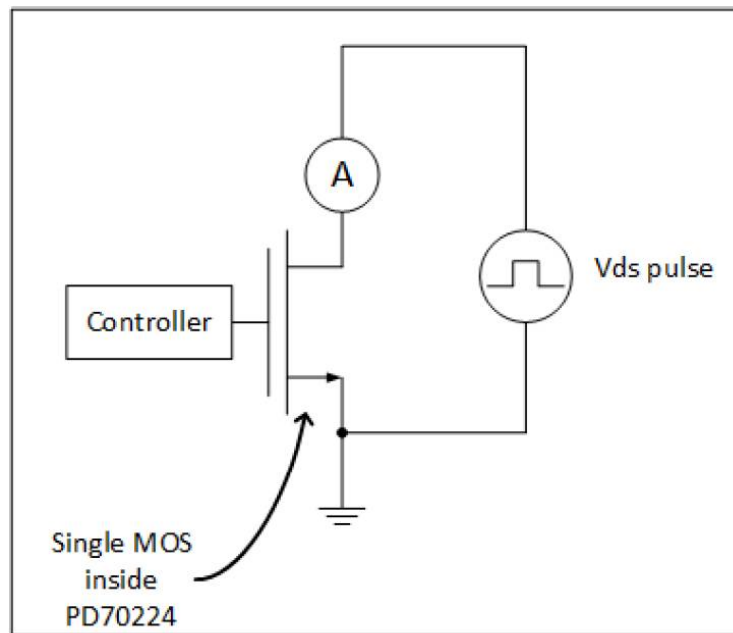
.....continued						
Symbol	Parameter	Conditions	Min	Typ	Max	Units
R _{DS}	FET drain to source resistance	I _D = 0.6 A T _J = 25 °C		0.16	0.26	Ω
		I _D = 0.6 A; –40 °C ≤ T _J ≤ 125 °C			0.38	Ω
I _R	Leakage current (reverse)	V _{OUTP} – V _{OUTN} = 57 V			80	μA
V _{BFD}	Backfeed voltage	Between input terminals with 100 kΩ resistor across them and 57 V between OUTP and OUTN			2.7	V
I _{MAX_Off}	Maximum Forward Current (per bridge) below V _{TURN_ON}				0.45	A
I _{MAX_On}	Maximum forward current (per bridge) above V _{TURN_ON} . Per bridge, while only one bridge out of the two is active.				1.5	A
I _{MAX_LOAD}	Maximum load current (per device) above V _{TURN_ON} . Per device while two bridges are active and each bridge is supporting half load.				2	A
V _{D_SUPP}	Maximum voltage drop between INx to SUPP_Sx pins.	Supp_Sx loaded with 100 kΩ resistor			2	V
I _{MAX_SUPP}	Maximum current to consume from SUPP_Sx pins.				10	mA
V _{IH}	WA_EN – Input high logic		1.35			V
V _{IL}	WA_EN – Input low logic				1.05	V

Figure 2-1. Safe Operating Area



The PD70224 SOA is based on measuring the SOA of a single NMOS device that is used to construct the diode bridge.

Figure 2-2. SOA Test Setup



This data is provided for information purposes. For additional information on Surge Immunity and Microchip Recommendations, see AN3410 PD Surge Protection for ITU-T k.21 2019.

3. Pin Descriptions

The following illustration is a representation of PD70224 device, as seen from the top and bottom view.

Figure 3-1. Internal Construction and Pinout

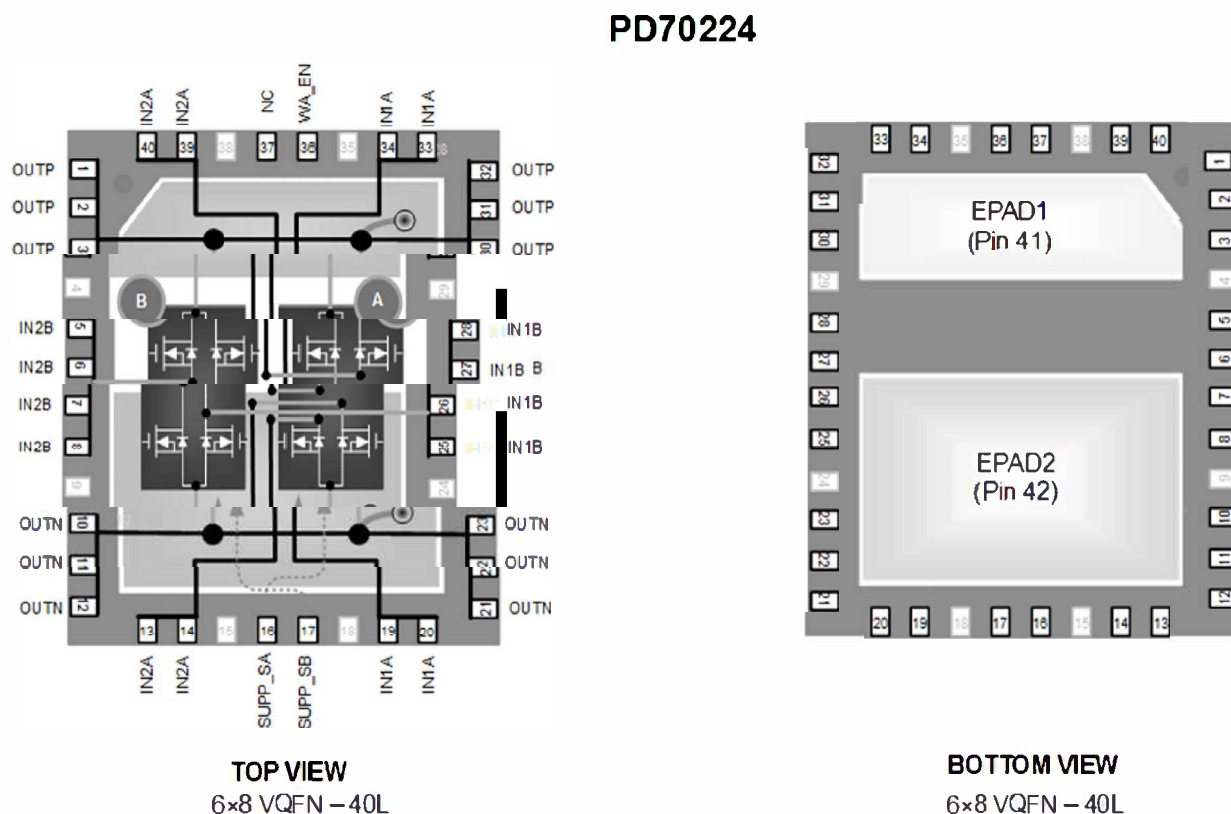


Table 3-1. Pin Description

Pin Number PD70224 VQFN 40 Lead	Pin Designator	Description
1, 2, 3	OUTP	Rectified positive (upper) rail shared by both bridges
4	N.A.	Not applicable (pin not present)
5, 6, 7, 8	IN2B	Input "2" of bridge rectifier number B
9	N.A.	Not applicable (pin not present)
10, 11, 12	OUTN	Rectified negative (lower) rail shared by both bridges
13, 14	IN2A	Input "2" of bridge rectifier number A (same as pins 39 and 40) ¹
15	N.A.	Not applicable (pin not present)
16	SUPP_SA	Input power supply detect pin for bride rectifier number A. Goes high when pairs connected to this bridge are powered by the PSE.
	N.A.	Not applicable (pin not present)
17	SUPP_SB	Input power supply detect pin for bride rectifier number B. Goes high when pairs connected to this bridge are powered by the PSE.

.....continued

Pin Number PD70224 VQFN 40 Lead	Pin Designator	Description
18	N.A.	Not applicable (pin not present)
19, 20	IN1A	Input "1" of bridge rectifier number A. ²
21, 22, 23	OUTN	Rectified negative (lower) rail shared by both bridges (same as pins 10, 11, and 12)
24	N.A.	Not applicable (pin not present)
25, 26, 27, 28	IN1B	Input "1" of bridge rectifier number B
29	N.A.	Not applicable (pin not present)
30, 31, 32	OUTP	Rectified positive (upper) rail shared by both bridges (same as pins 1, 2, and 3)
33, 34	IN1A	Input "1" of bridge rectifier number A (same as pins 19 and 20) ³
35	N.A.	Not applicable (pin not present)
36	WA_EN	While this input is low (referenced to OUTN), the chip work according to internal flow diagram. When this input is high, it enable wall adapter feature, that is, turn OFF internal switches and act as regular diode bridge.
	N.A.	Not applicable (pin not present)
37	N.C.	Not connected; do not connect externally (leave floating)
38	N.A.	Not applicable (pin not present)
39, 40	IN2A	Input "2" of bridge rectifier number A (same as pins 13 and 14) ⁴
41	EPAD1	Connect to OUTP on PCB
42	EPAD2	Connect to OUTN on PCB

Notes:

1. These pins are not shorted to pins 39 and 40 inside the device. The device functionality relies on a copper trace on the PCB, between pins 13, 14, 39, and 40.
2. These pins are not shorted to pins 33 and 34 inside the device. The device functionality relies on a copper trace on the PCB, between pins 33, 34, 19, and 20.
3. These pins are not shorted to pins 19 and 20 inside the device. The device functionality relies on a copper trace on the PCB, between pins 33, 34, 19, and 20.
4. These pins are not shorted to pins 13 and 14 inside the device. The device functionality relies on a copper trace on the PCB, between pins 13, 14, 39, and 40.

4. Package Information

4.1 Package Outline Drawing

Figure 4-1. PD70224 Package Outline Drawing 40-Pin QFN 6 mm × 8 mm

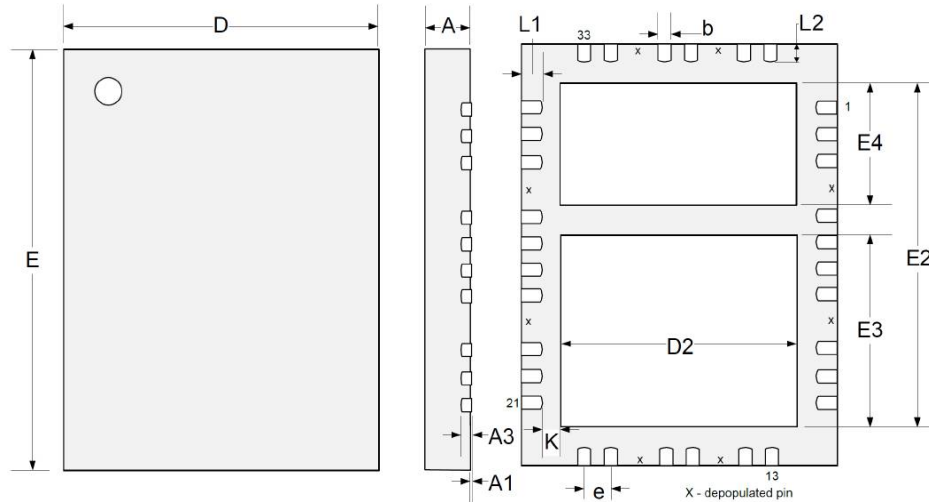


Table 4-1. Package Measurements

Dim	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	6.00 BSC		0.236 BSC	
E	8.00 BSC		0.315 BSC	
D2	4.25	4.50	0.167	0.177
E2	6.35	6.6	0.250	0.260
E3	3.50	3.75	0.138	0.148
E4	2.20	2.46	0.087	0.097
e	0.50 BSC		0.020 BSC	
K	0.30		0.012	
L1	0.37	0.57	0.014	0.022
L2	0.30	0.50	0.012	0.020

Notes:

- Dimensions do not include protrusions; these shall not exceed 0.155 mm (.006") on any side. Lead dimension shall not include solder coverage.
- Dimensions are in millimeters, inches for reference only.

4.2 Thermal Specifications

The following table lists the thermal specifications of PD70224.

Table 4-2. Thermal Properties

Thermal Resistance	Min	Typ	Max	Units
θ_{JA}		31		°C/W
θ_{JL}		2.5		°C/W
θ_{JC}		5		°C/W

Note: The θ_{JX} numbers assume no forced airflow. Junction temperature is calculated using $T_J = T_A + (P_D \times \theta_{JA})$. In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

4.3 Recommended PCB Layout

The following figures show the PD70224 recommended PCB layout for 40-pin QFN 6 mm × 8 mm.

The pad for pins 4, 9, 15, 18, 24, 29, 35, and 38 is missing from the layout because it does not exist in package.

Figure 4-2. Top-Layer Copper (mm)

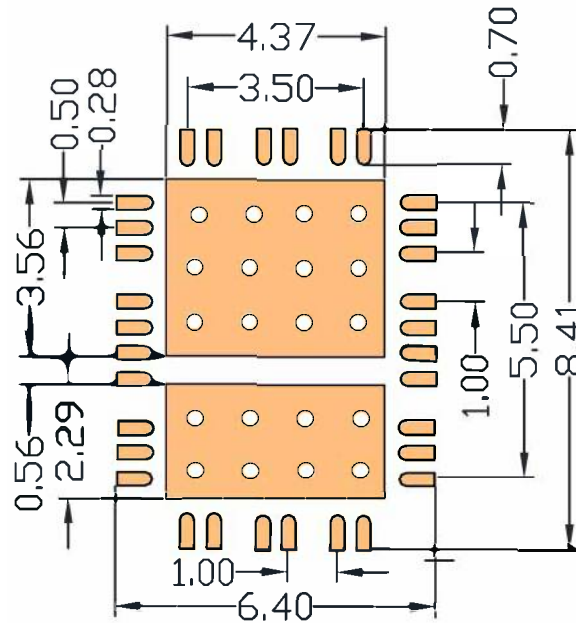


Figure 4-3. Top-Layer Solder Mask, Solder Paste, and Vias (mm)

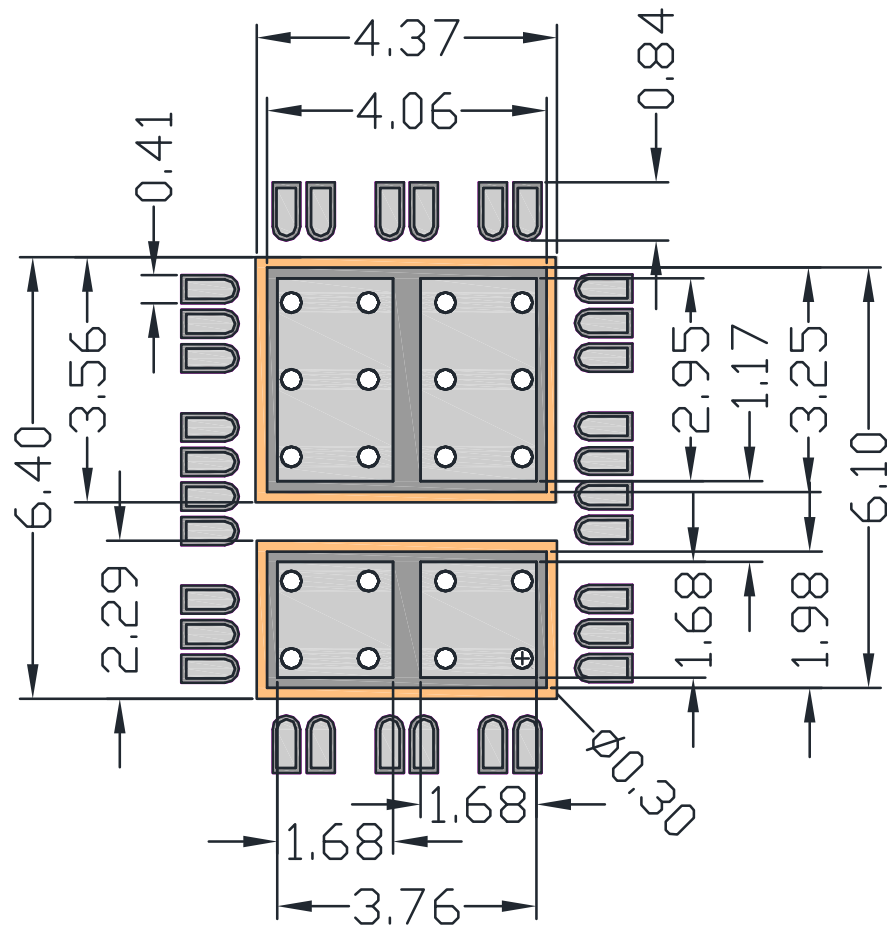
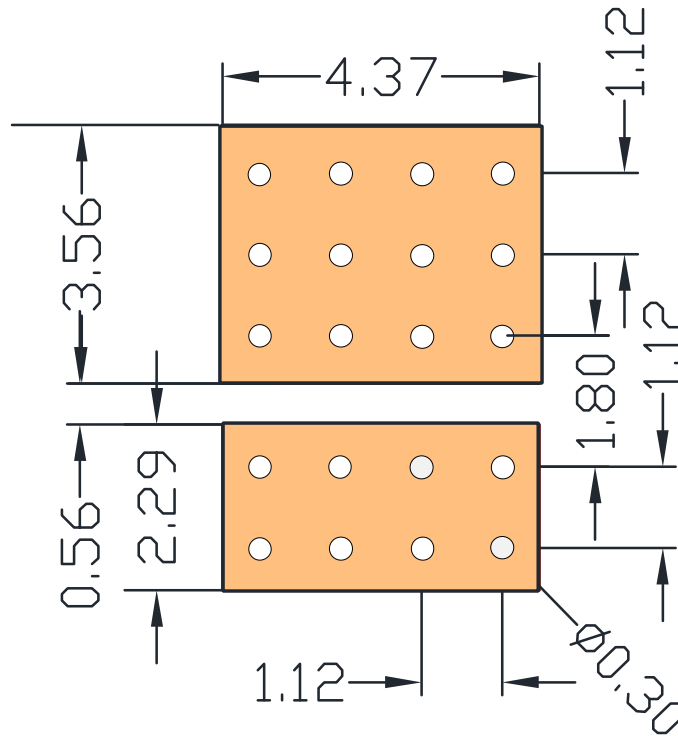


Figure 4-4. Bottom Layer Copper and Vias for Thermal Pad Array (mm)



Note: The contract manufacturer has latitude to modify the solder paste stencil for manufacturability reasons. The solder paste stencil covers 65% to 80% of the thermal pad and should not allow solder to be applied to the thermal vias under the QFN package using any method they deem appropriate. At the pin, the dimension of the paste mask should be 5-10% smaller than the PCB copper feature. Minimize the extension of the solder mask outside the edge of the package. Any design should be subject to system validation and qualification prior to commitment to mass production of field deployment. Use a 5 mil stencil.

5. Application Information

The following section describes the application information of the device.

5.1 Peripheral Devices

PD applications utilizing PD70224 IC should use 1 nF/100 V ceramic capacitor at Bridge A inputs and at Bridge B inputs.

For surge and ESD protection, refer to [AN3410, Design for PD System Surge Immunity PD701xx PD702xx](#).

A 10 kΩ resistor should be placed on SUPP_SA and SUPP_SB lines between PD70224 and PD70210A.

When WA_EN function is not used, connect WA_EN pin to OUTN Pin.

When WA_EN function is used, connect a capacitor (1 nF to 100 nF/10V) between WA_EN pin and OUTN Pin.

The devices are presented in the figures PD70224 Package Outline Drawing 40-Pin QFN 6 mm × 8 mm and PD70224 Top layer Copper Recommended PCB Layout (mm).

5.2 Operation with an External DC Source

PD applications utilizing the PD70224 IC may be operated with an external power source (DC wall adaptor). There are two cases of providing power with an external source, as shown in the following figures.

Note: Protection is not shown in either figure, see application note "Design for PD System Surge Immunity" for recommended protection scheme.

1. External source connected to application's low voltage supply rails. External source voltage level is dependent on DCDC output characteristics. This connection is not affected by the PD70224 use.
2. External source connected to PD device output connection toward the application (VPP to VPNOOUT). External source voltage level is dependent on DCDC input requirements.

Figure 5-1. External Power Input Connected to Application Supply Rails

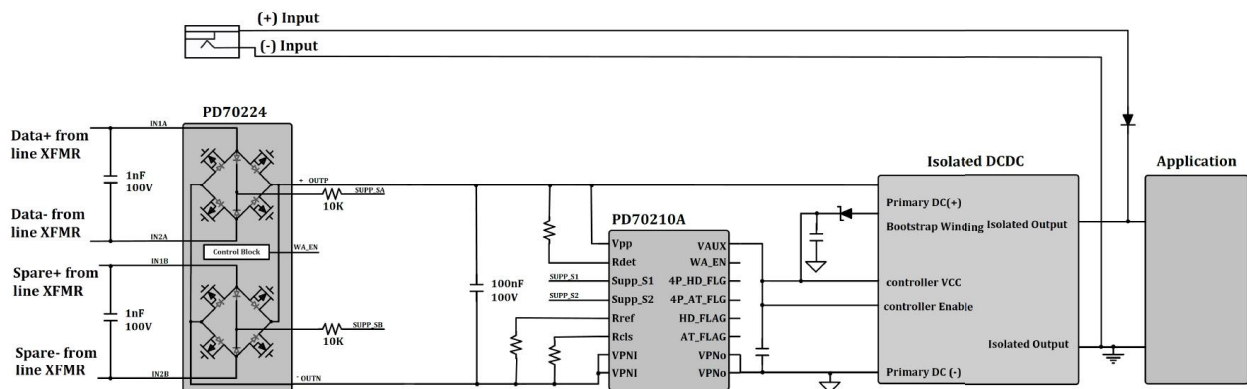
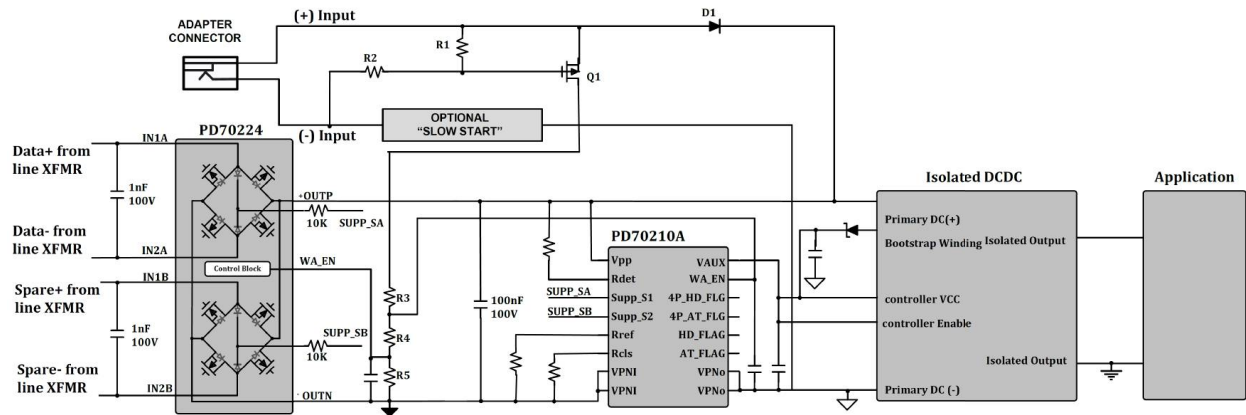


Figure 5-2. External Power Input Connected to PD70210A Output



5.2.1 External Source Connected to PD Device Output

The PD70224 WA_EN pin will be used for protecting the PSE when an external adapter is connected.

In this mode, the risk to PSE side exists when a higher voltage external adapter is hot connected to the system.

When the WA_EN input voltage is higher than its threshold level, PD70224 internal FETs are disabled, converting the device into standard diode bridge.

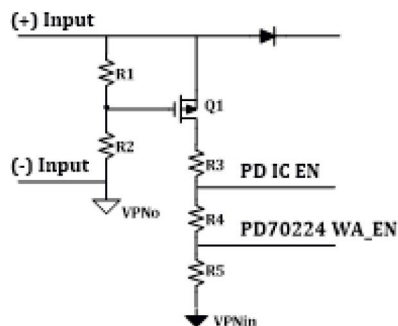
An optional “slow start” circuit prevents adapter jack contact arcing when an adapter is “hot plugged” by limiting its surge current. For the detailed circuit, see [AN3472, Implementing Aux Power in PoE](#).

The PD70210A also has a specific input pin, to disable the isolation switch, when an external adapter is connected.

In this case, WA_EN resistors divider depends on the “turn off” threshold of the PD70210A and PD70224.

Zooming into the resistors to be selected in external adapter connection.

Figure 5-3. External Power Input Resistors Dividers



R1 and R2 sets a rough threshold for PFET Q1 enable to detect whether external adapter exists or not. It should be set to be lower threshold than PD70224 and PD70210A disable levels.

R3, R4, and R5 set PD70210A disable threshold and PD70224 disable threshold.

PD70210A disable threshold should be set so that it will always be lower than PD70224 disable threshold.

1 V is a good choice for the margin between the two.

So, in case of 44 V–57 V external adapter, the disable setting can be selected as follows:

PFET enable threshold = 35 V

PD70224 disable threshold = 43 V

R1 and R2 setting should be so that the value of Q1 VGS < 20 V at max voltage condition of external adapter.

While external adapter voltage is above 35 V, Q1 will be above its VGSth value.

$$VGS = Vext_adapter \times \frac{R1}{R1 + R2}$$

Suppose VGSt_h is 3.5 V, thus we will set VGS= 5 V.

R1 is selected as 2 kΩ.

$$R2 = R1 \times \frac{Vext_adapter - VGS}{VGS}$$

Using R1= 2 kΩ, Vext_adapter= 30 V and VGS= maximum VGSt_h= 3.5 V. We get R2 value.

$$R2 = 15K\Omega$$

$$= PD70210A_Wa_en = Vext_adapter_PD70210A \times \frac{R4}{(R3 + R4)}$$

$$R2 = R1 \times \frac{Vext_adapter - VGS}{VGS}$$

R3, R4, and R5 are set using the following two equations.

$$(I) \quad PD70224_Wa_en = Vext_adapter_PD70224 \times \frac{R5}{(R3+R4+R5)}$$

$$(II) \quad PD70210A_Wa_en = Vext_adapter_PD70210A \times \frac{R4+R5}{(R3+R4+R5)}$$

Set R3, R4, and R5 up to few KΩ.

At equation (I) set Vext_adapter_PD70224= 44 V and from PD70224 datasheet PD70224 _WA_EN=1.35 V.

At equation (II) set Vext_adapter_PD70210A= (minimum Vext_adapter_PD70224 -1 V) and from PD_IC data sheet PD70210A_WA_EN= 2.4 V.

R5 is selected as 620.

Solving the two equations plus accuracy and verifying that PD70210A is always disconnected before PD70224, we get the optimum resistors values for an adapter of adapter of 36 V and above.

$$R3 = 15K\Omega$$

$$R4 = 820\Omega$$

$$R5 = 620\Omega$$

6. Design Example

The following four figures show the layout of PD70224 EVB evaluation board.

The board is two layers PCB. U2 is PD70224.

This board can be ordered from Microchip.

Figure 6-1. PD70224 EVB PCB Silk Top

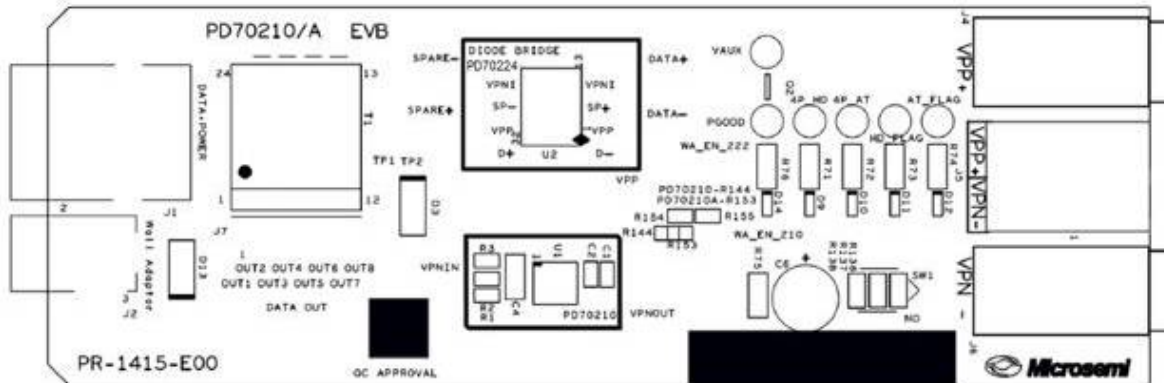


Figure 6-2. PD70224 EVB PCB Silk Bottom

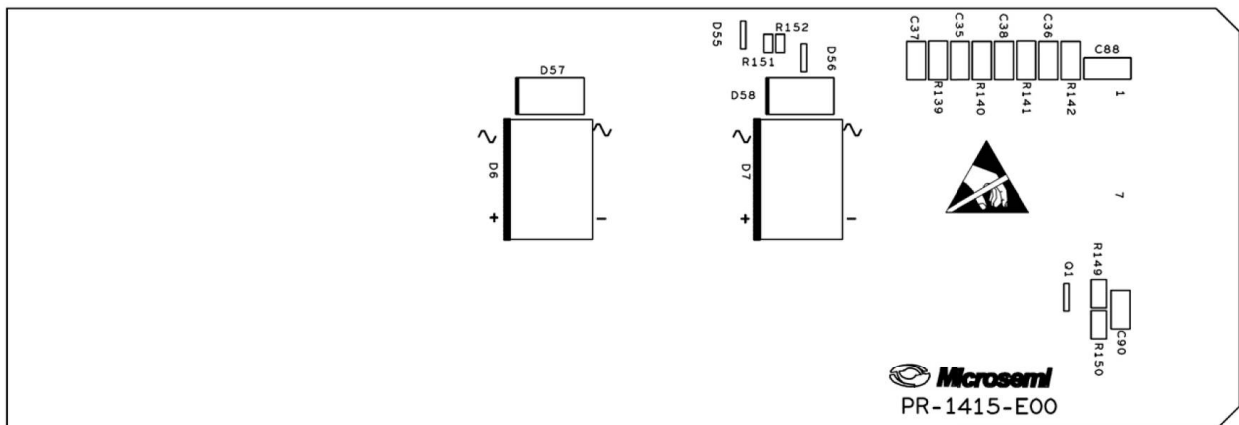


Figure 6-3. PD70224 EVB PCB Top Copper

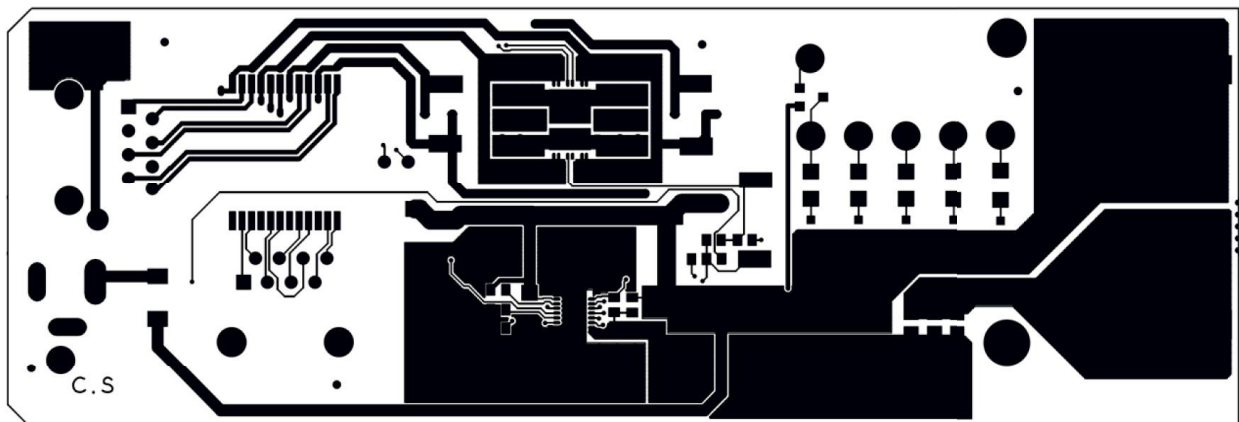
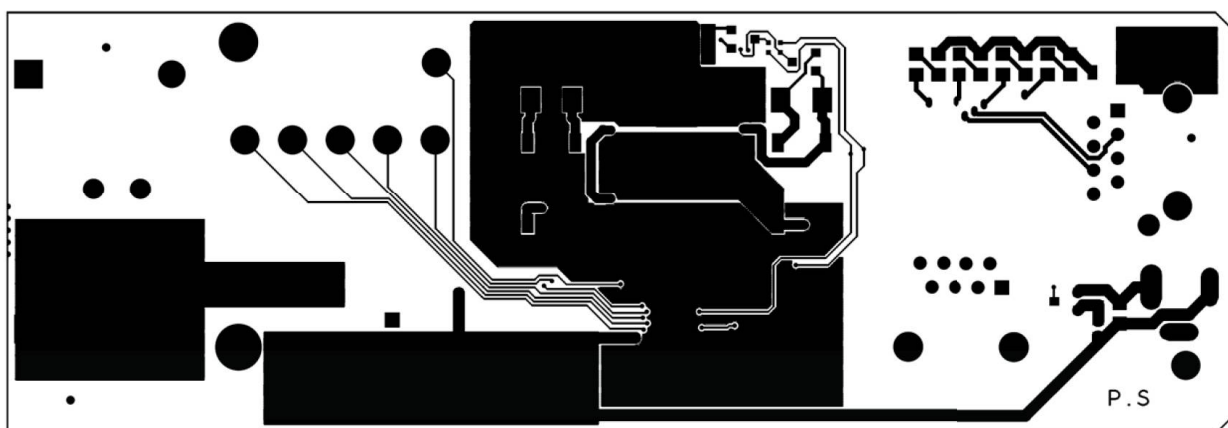


Figure 6-4. PD70224 EVB PCB Bottom Copper



7. Ordering Information

The following table lists the ordering information of the PD70224 device.

Table 7-1. Ordering Information

Part Number	Ambient Temperature	Type	Package	Packaging Type	Part Marking
PD70224ILQ-TR	–40 °C to 85 °C	RoHS compliant Pb free MSL3	QFN (40 lead)	Tape and reel	Microsemi Logo PD70224 ZZ e4 ¹ YYWWNNN

1. ZZ e4: ZZ= Random character with no meaning, e4 = Second-level interconnect.
2. YY= Year, WW= Week, NNN= Trace code.

8. Revision History

Revision	Date	Description
C	October 2020	Updated a typo for a value of K in the Package Measurements table.
B	September 2020	<p>The following is a summary of changes in revision C of this document.</p> <ul style="list-style-type: none"> • Updated the Introduction section. • Added Technical Support and Documentation section. • Updated the values of K in the Package Measurements table. • Updated the Internal Construction and Pinout figure. • Updated the 4.3 Recommended PCB Layout section. • Updated the PD70224 EVB PCB Silk Top figure. • Updated the Ordering Information table.
A	July 2020	<ul style="list-style-type: none"> • Updated to Microchip format. • Updated document number from PD-000307871 to DS00003590. • Deleted figure "PD70224 Bottom Layer Copper and Solder Paste Recommended PCB Layout for Thermal Pad Array (mm)" in the Recommended PCB Layout section.
3.0	August 2019	Updated the package marking in the Ordering Information section.
2.0	February 2018	<ul style="list-style-type: none"> • Updated part marking. • Updated figure External Power Input Connected to PD70210A Output. • Added MSL3 compliance. • Updated Safe Operating Area graph to show test methodology and discuss protection recommendations. • Moved Recommended Protection Scheme to the application note "Design for PD System Surge Immunity".
1.3	May 2016	Updated Figure 7 with optional slow start circuit.
1.2	November 2014	<ul style="list-style-type: none"> • Removed watermark. • Updated ESD with IN1A/IN2A 1000 V note.
1.1	July 2015	Updated ESD.
1.0	August 2014	<ul style="list-style-type: none"> • Added maximum SUPP_Sx current, application information, and SOA graph. • Updated MSL level.
0.73	June 2014	Updated leadframe for thermal pad.
0.72	May 2014	Added dimensions to recommended layout IMAX_LOAD.
0.7	May 2014	Initial Revision

The Microchip Website

Microchip provides online support via our website at www.microchip.com/. This website is used to make files and information easily available to customers. Some of the content available includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Product Change Notification Service

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to www.microchip.com/pcn and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: www.microchip.com/support

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Legal Notice

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with

your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AnyRate, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, chipKIT, chipKIT logo, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Klear, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PackeTime, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TempTrackr, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

APT, ClockWorks, The Embedded Control Solutions Company, EtherSynch, FlashTec, Hyper Speed Control, HyperLight Load, IntelliMOS, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet-Wire, SmartFusion, SyncWorld, Temux, TimeCesium, TimeHub, TimePictra, TimeProvider, Vite, WinPath, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BlueSky, BodyCom, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, INICnet, Inter-Chip Connectivity, JitterBlocker, KlearNet, KlearNet logo, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, SAM-ICE, Serial Quad I/O, SMART-I.S., SQL, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, and Symmcom are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2020, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

ISBN: 978-1-5224-6885-1

Quality Management System

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
Corporate Office 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: www.microchip.com/support Web Address: www.microchip.com	Australia - Sydney Tel: 61-2-9868-6733 China - Beijing Tel: 86-10-8569-7000 China - Chengdu Tel: 86-28-8665-5511 China - Chongqing Tel: 86-23-8980-9588 China - Dongguan Tel: 86-769-8702-9880 China - Guangzhou Tel: 86-20-8755-8029 China - Hangzhou Tel: 86-571-8792-8115 China - Hong Kong SAR Tel: 852-2943-5100 China - Nanjing Tel: 86-25-8473-2460 China - Qingdao Tel: 86-532-8502-7355 China - Shanghai Tel: 86-21-3326-8000 China - Shenyang Tel: 86-24-2334-2829 China - Shenzhen Tel: 86-755-8864-2200 China - Suzhou Tel: 86-186-6233-1526 China - Wuhan Tel: 86-27-5980-5300 China - Xian Tel: 86-29-8833-7252 China - Xiamen Tel: 86-592-2388138 China - Zhuhai Tel: 86-756-3210040	India - Bangalore Tel: 91-80-3090-4444 India - New Delhi Tel: 91-11-4160-8631 India - Pune Tel: 91-20-4121-0141 Japan - Osaka Tel: 81-6-6152-7160 Japan - Tokyo Tel: 81-3-6880-3770 Korea - Daegu Tel: 82-53-744-4301 Korea - Seoul Tel: 82-2-554-7200 Malaysia - Kuala Lumpur Tel: 60-3-7651-7906 Malaysia - Penang Tel: 60-4-227-8870 Philippines - Manila Tel: 63-2-634-9065 Singapore Tel: 65-6334-8870 Taiwan - Hsin Chu Tel: 886-3-577-8366 Taiwan - Kaohsiung Tel: 886-7-213-7830 Taiwan - Taipei Tel: 886-2-2508-8600 Thailand - Bangkok Tel: 66-2-694-1351 Vietnam - Ho Chi Minh Tel: 84-28-5448-2100	Austria - Wels Tel: 43-7242-2244-39 Fax: 43-7242-2244-393 Denmark - Copenhagen Tel: 45-4485-5910 Fax: 45-4485-2829 Finland - Espoo Tel: 358-9-4520-820 France - Paris Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79 Germany - Garching Tel: 49-8931-9700 Germany - Haan Tel: 49-2129-3766400 Germany - Heilbronn Tel: 49-7131-72400 Germany - Karlsruhe Tel: 49-721-625370 Germany - Munich Tel: 49-89-627-144-0 Fax: 49-89-627-144-44 Germany - Rosenheim Tel: 49-8031-354-560 Israel - Ra'anana Tel: 972-9-744-7705 Italy - Milan Tel: 39-0331-742611 Fax: 39-0331-466781 Italy - Padova Tel: 39-049-7625286 Netherlands - Drunen Tel: 31-416-690399 Fax: 31-416-690340 Norway - Trondheim Tel: 47-72884388 Poland - Warsaw Tel: 48-22-3325737 Romania - Bucharest Tel: 40-21-407-87-50 Spain - Madrid Tel: 34-91-708-08-90 Fax: 34-91-708-08-91 Sweden - Gothenberg Tel: 46-31-704-60-40 Sweden - Stockholm Tel: 46-8-5090-4654 UK - Wokingham Tel: 44-118-921-5800 Fax: 44-118-921-5820

SYST-30IWCH812 - Data Sheet - PD70224 Datasheet Document Revision

Affected Catalog Part Numbers(CPN)

PD70224ILQ-TR

PD70224LILQ-TR