



Cypress Semiconductor Corporation – An Infineon Technologies Company
198 Champion Court, San Jose, CA 95134. Tel: (408) 943-6200

PRODUCT CHANGE NOTIFICATION

PCN:PCN203801

Date: September 16, 2020

Subject: Qualification of UMC as an Alternate Wafer Fab Site for Select Industrial Grade 4Mb MoBL® SRAM Products

To: PCN Coordinator PCN Coordinator
FUTURE
PCN.System@Future.ca

Description of Change:

Cypress announces the qualification of UMC's 65nm (No. 3, Li-Hsin 2nd Rd., Hsinchu Science Park, Hsinchu, Taiwan, R.O.C.) as an alternate wafer fab site for select 90nm 2.2V – 3.6V and 4.5V – 5.5V industrial grade 4Mb MoBL® products. The 65nm products are drop-in replacement parts and form, fit, and function compatible with the 90nm 4Mb Async MoBL SRAM products manufactured at SkyWater, Minnesota. There will be no change to the existing marketing part numbers.

Benefit of Change:

Qualification of alternate manufacturing sites and technologies is part of Cypress' ongoing flexible manufacturing initiative. The goal of the flexible manufacturing initiative is to provide the means for Cypress to continue to meet delivery commitments through dynamic, changing market conditions.

Part Numbers Affected: 29

See the attached 'Affected Parts List' file for a list of all part numbers affected by this change. Note that any new parts that are introduced after the publication of this PCN will include all changes outlined in this PCN.

Qualification Status:

LL65 (65nm) technology at UMC was previously qualified through a series of tests identified in the Qualification Test Plan QTP#192409. This qualification report can be found as an attachment to this PCN or by visiting www.cypress.com and typing the QTP number in the keyword search window.

Sample Status:

Qualification samples may not be built ahead of time for all part numbers affected by this change. Please review the attached 'Affected Parts List' file for a list of affected part numbers with their associated sample ordering part numbers. If you require qualification samples, please

contact your local Cypress Sales Representative as soon as possible, preferably within 30 days of the date of this PCN, to place any sample orders.

Approximate Implementation Date:

Effective 90 days from the date of this notification or upon customer approval, whichever comes first, all shipments of Commercial, Industrial and Automotive non-PPAP part numbers in the attached file will be fabricated at either SkyWater or UMC.

Anticipated Impact:

None anticipated. Products fabricated at UMC are completely compatible with existing product from a form, fit, functional, parametric, and quality performance perspectives.

Cypress also recommends that customers take this opportunity to review these changes against current application notes, system design considerations and customer environment conditions to assess impact (if any) to their application.

Method of Identification:

Cypress maintains traceability of product to wafer level, including wafer fabrication location, through the lot number marked on the package.

Response Required:

No response is required.

For additional information regarding this change, contact your local sales representative or contact the PCN Administrator at pcn_adm@cypress.com.

Sincerely,

Cypress PCN Administration

Cypress Semiconductor Product Qualification Report

QTP# 192409 VERSION
September 2020**

4-MBIT MoBL Asynchronous SRAM Family LL65UP-25ODR Technology, UMC Fab 12A	
CY62146G*	INDUSTRIAL MoBL™, 4-MBIT (256K WORDS X 16 BIT) STATIC RAM W/ AND W/O ERROR CORRECTING CODE (ECC), 3V, 5V AND EXTENDED RANGE (GANGES EQUIVALENT)
CY62146GSL*	
CY62146GE*	
CY62146GESL*	
CY62147G*	
CY62147GE*	
CY621472G*	
CY62146GN*	
CY62147GN*	
CY62148G*	INDUSTRIAL MoBL™, 4-MBIT (512K WORDS X 8 BIT) STATIC RAM W/ AND W/O ERROR CORRECTING CODE (ECC), 3V, 5V AND EXTENDED RANGE (GANGES EQUIVALENT)
CY62148GN*	
CY62146E*	INDUSTRIAL MoBL™, 4-MBIT (256K WORDS X 16 BIT) STATIC RAM, 3V, 5V AND EXTENDED RANGE (RAM95 EQUIVALENT)
CY62147E*	
CY62148E*	INDUSTRIAL MoBL™, 4-MBIT (512K WORDS X 8 BIT) STATIC RAM, 3V, 5V AND EXTENDED RANGE (RAM95 EQUIVALENT)

FOR ANY QUESTIONS ON THIS REPORT, PLEASE CONTACT

reliability@cypress.com

Prepared By:

Josephine Pineda (JYF)
Reliability Engineer

Reviewed By:

Sandhya Chandrashekhar (SANC)
Reliability Manager

Approved By:

David Hoffman (DHH)
Reliability Director

QUALIFICATION HISTORY

QTP Number	Description of Qualification Purpose	Date Comp
091706	Qualification of 65nm (LL65) Technology at UMC Fab 12A and New Device CY7C1553K Base Die Product Family	August 2009
124902	Qualification of 16-MBIT Asynchronous SRAM Family, LL65UP-25ODR Technology at UMC Fab 12A	August 2014
144804	Qualification of 16-MBIT Asynchronous SRAM Family Rev.*D Silicon, LL65UP-25ODR Technology at UMC Fab 12A	February 2015
145003	Qualification of 4-MBIT Asynchronous SRAM Family, LL65UP-25ODR Technology at UMC Fab 12A	July 2015
192409	Qualification of 4-MBIT MoBL Asynchronous SRAM Family LL65UMP-25ODR Technology, UMC Fab 12A	August 2020

PRODUCT DESCRIPTION (for qualification)	
Qualification Purpose:	Qualify 4-MBIT MoBL Asynchronous SRAM Family, LL65UP-25ODR Technology at UMC Fab 12A
Marketing Part #:	CY62146G*, CY62147G*, CY621472G*, CY62148G* (GANGES EQUIVALENT) CY62146E*, CY62147E*, CY62148E* (RAM95 EQUIVALENT)
Device Description:	4-MBIT MoBL Asynchronous SRAM Family
Cypress Division:	Cypress Semiconductor Corporation –Memory Solutions (MS)

TECHNOLOGY/FAB PROCESS DESCRIPTION – LL65UP-25ODR			
Number of Metal Layers:	Proprietary	Metal Composition:	Proprietary
Passivation Type and Materials:	Proprietary		
Number of Transistors in Device	Proprietary		
Number of Logic Gates in Device	Proprietary		
Generic Process Technology/Design Rule (μ -drawn):	Proprietary		
Gate Oxide Material/Thickness (MOS):	Proprietary		
Name/Location of Die Fab (prime) Facility:	UMC Fab 12A		
Die Fab Line ID/Wafer Process ID:	L65LL		

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	ZW44A
Package Outline, Type, or Name:	TSOP II (Thin Small Outline Package)
Mold Compound Name/Manufacturer:	KE-G6000DA/ Kyocera
Mold Compound Flammability Rating:	V-0 / UL94
Oxygen Rating Index:	>28%
Leadframe Material:	Copper
Lead Finish, Composition / Thickness:	NiPdAu
Die Backside Preparation Method/Metallization:	Backgrind
Die Separation Method:	Saw
Die Attach Supplier:	Henkel
Die Attach Material:	QMI 509
Bond Diagram Designation:	001-95718
Wire Bond Method:	Thermosonic
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	001-99312
Name/Location of Assembly (prime) facility:	CML-RA
MSL Level	3
Reflow Profile	260C

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	CML-R

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
Acoustic Microscopy	J-STD-020 Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260°C Reflow)	P
Age Bond Strength	200°C, 4HRS MIL-STD-883, Method 883-2011	P
Constructional Analysis	Criteria: Meet external and internal characteristics of Cypress package	P
Dynamic Latch-up	125°C , 8.25V JESD78	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V, 750V, 1000V, 1250V JESD22-C101	P
Electrostatic Discharge Human Body Model (ESD-HBM)	1100V to 8000V JESD22-A114	P
Electrostatic Discharge Machine Model (ESD-MM)	200V JESD22-A115	P
High Accelerated Saturation Test (HAST)	JEDEC STD 22-A110: 130°C, 85%RH, 2.25V 110°C/130°C, 85%RH, 3.65V Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260°C Reflow)	P
High Temperature Steady State Life	Static Operating Condition, Vcc Max= 1.37/2.25V, 150°C JESD22-A108	P
High Temperature Storage	JESD22-A103:150°C No bias	P
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc Max = 1.44V, 125°C JESD22-A108	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc Max = 1.44V, 125°C JESD22-A108	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Boost Regulated at Core, 1.45V, External 2.05V, 125°C /150°C JESD22-A108	P
Low Temperature Operating Life	Dynamic Operating Condition, Vcc = 1.62V/2.25V, -30°C JESD22-A108	P
Pressure Cooker	JESD22-A102: 121°C, 100%RH, 15 PSIG Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260°C Reflow)	P
Pre/Post LFR AC/DC Char	AC/DC Critical Parameter Char at 0 hour/500/168/1000hrs	P
Static Latch-up	125°C , ± 100mA , ± 140mA 85°C, ± 140mA, ± 200mA, ± 300mA JESD78	P
Temperature Cycle	MIL-STD-883, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260°C Reflow)	P
Temperature Humidity Bias Test (THB)	JESD22-A101: 85°C/ 85% RH , 2.25V Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260°C Reflow)	P
Soft Error (Alpha Particle)	JESD89	P
Soft Error (Neutron)	JESD89	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF ³	Failure Rate
High Temperature Operating Life ¹ Early Failure Rate	3,575 Devices	0	N/A	N/A	0 PPM ¹
High Temperature Operating Life ² Long Term Failure Rate (150°C)	89,000 DHRs	0	0.7	170	8 FIT ²
High Temperature Operating Life ² Long Term Failure Rate (125°C)	1,908,000 DHRs	0	0.7	55	

¹Early Failure Rate was computed from QTP# 192409 data.

² Long Term Failure Rate was computed from QTP# 091706, QTP# 124902, QTP# 145003 and QTP# 192409 data.

¹ Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.

² Chi-squared 60% estimations used to calculate the failure rate..

³ Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp \left[\frac{E_A}{k} \left[\frac{1}{T_2} - \frac{1}{T_1} \right] \right]$$

where:

E_A =The Activation Energy of the defect mechanism.

K = Boltzmann's constant = 8.62x10⁻⁵ eV/Kelvin.

T₁ is the junction temperature of the device under stress and T₂ is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 091706

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	G-TAIWAN	COMP	15	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	G-TAIWAN	COMP	15	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	G-TAIWAN	COMP	15	0	
STRESS: AGE BOND STRENGTH							
CY7C1514KV18 (7C1553K)	8842022	610851583	G-TAIWAN	COMP	5	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	G-TAIWAN	COMP	5	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	G-TAIWAN	COMP	5	0	
STRESS: DYNAMIC LATCH-UP							
CY7C1470V33 (7C1470A)	4321389	610417278	CML-R	COMP	3	0	
STRESS: ESD-HUMAN BODY MODEL, 2,200V							
CY7C1514KV18 (7C1553K)	8842022	610852338	G-TAIWAN	COMP	8	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	G-TAIWAN	COMP	8	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	G-TAIWAN	COMP	8	0	
CY7C1514KV18 (7C1553K)	8844021	610908348	G-TAIWAN	COMP	8	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1514KV18 (7C1553K)	8842022	610852338	G-TAIWAN	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	G-TAIWAN	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	G-TAIWAN	COMP	9	0	
STRESS: ESD-MACHINE MODEL, 200V							
CY7C1514KV18 (7C1553K)	8842022	610852338	G-TAIWAN	COMP	5	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 2.25V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8844020	610854240	G-TAIWAN	128	78	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	G-TAIWAN	128	77	0	
STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C							
CY7C1514KV18 (7C1553K)	8844020	610851583	G-TAIWAN	1000	70	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 2.25V, Vcc Max							
CY7C1514KV18 (7C1553K)	8844020	610854240	G-TAIWAN	336	77	0	

Reliability Test Data

QTP #: 091706

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C15631KV18 (7C1553K)	8908001	610920385	G-TAIWAN	96	2367	0	
CY7C15631KV18 (7C1553K)	8912000	610920386	G-TAIWAN	96	2217	0	
CY7C15631KV18 (7C1553K)	8910015	610920548	G-TAIWAN	96	1321	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C1514KV18 (7C1553K)	8844021	610908348	G-TAIWAN	500	178	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C1514KV18 (7C1553K)	8844020	610854240	G-TAIWAN	1000	178	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	G-TAIWAN	1000	178	0	
STRESS: LOW TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, -30C, 2.25V Vcc							
CY7C1514KV18 (7C1553K)	8842022	610852338	G-TAIWAN	500	45	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	G-TAIWAN	168	76	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	G-TAIWAN	168	78	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	G-TAIWAN	168	77	0	
STRESS: Pre-/ Post HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE CHAR							
CY7C1514KV18 (7C1553K)	8844020	610854240	G-TAIWAN	COMP	10	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 3.42V, +/-240mA							
CY7C1514KV18 (7C1553K)	8844020	610854680	G-TAIWAN	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	G-TAIWAN	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844021	610908348	G-TAIWAN	COMP	9	0	
CY7C15631KV18 (7C1553K)	8911000	610922436	G-TAIWAN	COMP	9	0	
STRESS: TEMPERATURE CYCLE COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	G-TAIWAN	1000	77	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	G-TAIWAN	1000	78	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	G-TAIWAN	1000	77	0	
STRESS: STRESS: TEMPRATURE HUMIDITY TEST, 85C, 85%RH, 2.25V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	G-TAIWAN	1000	77	0	

Reliability Test Data

QTP #: 091706

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: SER – ALPHA PARTICLE, 3-TEMP, 3-VOLTAGE, @ 85C, Vcc Nom							
CY7C1514KV18 (7C1553K)	8842022	610851583	G-TAIWAN	COMP	3	0	
STRESS: X-SECTION/STEM XY AUDIT							
CY7C1514KV18 (7C1553K)	8842022	610851583	G-TAIWAN	COMP	1WF		

Reliability Test Data

QTP #: 124902

<i>Device</i>	<i>Fab Lot #</i>	<i>Assy Lot #</i>	<i>Assy Loc</i>	<i>Duration</i>	<i>Samp</i>	<i>Rej</i>	<i>Failure Mechanism</i>
STRESS: ACOUSTIC, MSL3							
CY7C1061G30 (7CC171061A)	9313001	611348183	CML-RA	COMP	15	0	
CY7C1061G30 (7CC171061A)	9313001	611348182	CML-RA	COMP	170	0	
CY7C1061G30 (7CC171061A)	9313001	611348184	CML-RA	COMP	15	0	
STRESS: AGE BOND STRENGTH							
CY7C1061G30 (7CC171061A)	9313001	611348183	CML-RA	COMP	3	0	
CY7C1061G30 (7CC171061A)	9313001	611348182	CML-RA	COMP	3	0	
STRESS: CONSTRUCTIONAL ANALYSIS							
CY7C1061G30 (7CC171061A)	9313001	611348183	CML-RA	COMP	5	0	
CY7C1061G30 (7CC171061A)	9313001	611348182	CML-RA	COMP	5	0	
STRESS: DYNAMIC LATCH-UP TESTING, 125C, 8.25V							
CY7C1061G30 (7CC171061A)	9313001	611348182	CML-RA	COMP	3	0	
STRESS: ESD-CHARGE DEVICE MODEL							
CY7C1061G30 (7CC171061A)	9312001	611328720	CML-RA	500	9	0	
CY7C1061G30 (7CC171061A)	9312001	611328720	CML-RA	1000	3	0	
CY7C1061G30 (7CC171061A)	9312001	611328720	CML-RA	1250	3	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	500	9	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	1000	3	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	1250	3	0	
CY7C1061G30 (7CC171061A)	9302002	611320002	G-TAIWAN	500	9	0	
CY7C1061G30 (7CC171061A)	9302002	611320002	G-TAIWAN	1000	3	0	
CY7C1061G30 (7CC171061A)	9302002	611320002	G-TAIWAN	1250	3	0	
CY7C1069G30 (7CC171069A)	9302002	611320107	G-TAIWAN	500	9	0	
CY7C1069G30 (7CC171069A)	9302002	611320107	G-TAIWAN	1000	3	0	
CY7C1069G30 (7CC171069A)	9302002	611320107	G-TAIWAN	1250	3	0	

Reliability Test Data

QTP #: 124902

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-CHARGE DEVICE MODEL							
CY7C1061GE30(7CC1710613A)	9308001	611340082	G-TAIWAN	500	9	0	
CY7C1061GE30(7CC1710613A)	9308001	611340082	G-TAIWAN	750	3	0	
CY7C1062G30 (7CC171062A)	9302002	611321701	G-TAIWAN	500	9	0	
CY7C1062G30 (7CC171062A)	9302002	611321701	G-TAIWAN	1000	3	0	
CY7C1062G30 (7CC171062A)	9302002	611321701	G-TAIWAN	1250	3	0	
STRESS: ESD-HUMAN BODY MODEL							
CY7C1062G30 (7CC171062A)	9302002	611321701	G-TAIWAN	1100	3	0	
CY7C1062G30 (7CC171062A)	9302002	611321701	G-TAIWAN	2200	8	0	
CY7C1062G30 (7CC171062A)	9302002	611321701	G-TAIWAN	3300	3	0	
CY7C1061G30 (7CC171061A)	9302002	611320002	G-TAIWAN	1100	3	0	
CY7C1061G30 (7CC171061A)	9302002	611320002	G-TAIWAN	2200	8	0	
CY7C1061G30 (7CC171061A)	9302002	611320002	G-TAIWAN	3300	3	0	
CY7C1069G30 (7CC171069A)	9302002	611320107	G-TAIWAN	1100	3	0	
CY7C1069G30 (7CC171069A)	9302002	611320107	G-TAIWAN	2200	8	0	
CY7C1069G30 (7CC171069A)	9302002	611320107	G-TAIWAN	3300	3	0	
CY7C1061GE30(7CC1710613A)	9308001	611340082	G-TAIWAN	1100	3	0	
CY7C1061GE30(7CC1710613A)	9308001	611340082	G-TAIWAN	2200	8	0	
CY7C1061GE30(7CC1710613A)	9308001	611340082	G-TAIWAN	3300	3	0	
CY7C1061G30 (7CC171061A)	9312001	611328720	CML-RA	1100	3	0	
CY7C1061G30 (7CC171061A)	9312001	611328720	CML-RA	2200	8	0	
CY7C1061G30 (7CC171061A)	9312001	611328720	CML-RA	3300	3	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	1100	3	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	2200	8	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	3300	3	0	
STRESS: HI-ACCEL SATURATION TEST, 110C, 85%RH, 3.65V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1061G30 (7CC171061A)	9313001	611348182	CML-RA	264	30	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 3.65V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1061G30 (7CC171061A)	9313001	611348183	CML-RA	128	79	0	

Reliability Test Data

QTP #: 124902

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE – REG-ON, 125C, 6.0V							
CY7C1061G30 (7CC171061A)	9313001	611333269	CML-RA	96	50	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	96	50	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, 1.44V							
CY7C1061G30 (7CC171061A)	9313001	611333269	CML-RA	96	2107	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	96	1818	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, 1.44V							
CY7C1061G30 (7CC171061A)	9312001	611414530	CML-RA	168	1790	0	
CY7C1061G30 (7CC171061A)	9312001	611414530	CML-RA	1000	1750	0	
CY7C1061G30 (7CC171061A)	9313001	611333269	CML-RA	168	1800	0	
CY7C1061G30 (7CC171061A)	9313001	611333269	CML-RA	1000	1800	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	168	1790	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	1000	1780	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 1.37V							
CY7C1061G30 (7CC171061A)	9313001	611333269	CML-RA	168	80	0	
CY7C1062G30 (7CC171062A)	9302002	611321701	G-TAIWAN	168	80	0	
STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C							
CY7C1061G30 (7CC171061A)	9313001	611333088	CML-RA	500	79	0	
CY7C1061G30 (7CC171061A)	9313001	611333088	CML-RA	1000	79	0	
STRESS: LOW TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, -30C, 1.62V							
CY7C1061G30 (7CC171061A)	9313001	611333269	CML-RA	500	83	0	
STRESS: PRE/POST LFR CRITICAL PARAMETERS							
CY7C1061G30 (7CC171061A)	9312001	611414530	CML-RA	0	10+2	0	
CY7C1061G30 (7CC171061A)	9312001	611414530	CML-RA	1000	10+2	0	
CY7C1061G30 (7CC171061A)	9313001	611333269	CML-RA	0	10+2	0	
CY7C1061G30 (7CC171061A)	9313001	611333269	CML-RA	1000	10+2	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	0	10+2	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	1000	10+2	0	

Reliability Test Data

QTP #: 124902

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: PRE/POST LTOL CRITICAL PARAMETERS							
CY7C1061G30 (7CC171061A)	9313001	611333269	CML-RA	0	10+2	0	
CY7C1061G30 (7CC171061A)	9313001	611333269	CML-RA	500	10+2	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1061G30 (7CC171061A)	9313001	611348183	CML-RA	168	79	0	
CY7C1061G30 (7CC171061A)	9313001	611348183	CML-RA	288	79	0	
CY7C1061G30 (7CC171061A)	9313001	611333088	CML-RA	168	78	0	
CY7C1061G30 (7CC171061A)	9313001	611333088	CML-RA	288	78	0	
STRESS: STATIC LATCH-UP TESTING, 85C, 8.25V/9.1V, +/-140mA							
CY7C1062G30 (7CC171062A)	9302002	611321701	G-TAIWAN	COMP	6	0	
CY7C1061G30 (7CC171061A)	9302002	611320002	G-TAIWAN	COMP	6	0	
CY7C1069G30 (7CC171069A)	9302002	611320107	G-TAIWAN	COMP	6	0	
CY7C1061GE30(7CC1710613A)	9308001	611340082	G-TAIWAN	COMP	6	0	
CY7C1061G30 (7CC171061A)	9312001	611328720	CML-RA	COMP	6	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	COMP	6	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 8.25V/9.1V, +/-140mA							
CY7C1062G30 (7CC171062A)	9302002	611321701	G-TAIWAN	COMP	2	0	
CY7C1061G30 (7CC171061A)	9302002	611320002	G-TAIWAN	COMP	2	0	
CY7C1069G30 (7CC171069A)	9302002	611320107	G-TAIWAN	COMP	2	0	
CY7C1061GE30(7CC1710613A)	9308001	611340082	G-TAIWAN	COMP	2	0	
CY7C1061G30 (7CC171061A)	9312001	611328720	CML-RA	COMP	2	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	COMP	2	0	
STRESS: STATIC LATCH-UP TESTING, 85C, 8.25V/9.1V, +/-180mA							
CY7C1062G30 (7CC171062A)	9302002	611321701	G-TAIWAN	COMP	2	0	
CY7C1061G30 (7CC171061A)	9302002	611320002	G-TAIWAN	COMP	2	0	
CY7C1069G30 (7CC171069A)	9302002	611320107	G-TAIWAN	COMP	2	0	
CY7C1061GE30(7CC1710613A)	9308001	611340082	G-TAIWAN	COMP	2	0	
CY7C1061G30 (7CC171061A)	9312001	611328720	CML-RA	COMP	2	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	COMP	2	0	

Reliability Test Data

QTP #: 124902

<i>Device</i>	<i>Fab Lot #</i>	<i>Assy Lot #</i>	<i>Assy Loc</i>	<i>Duration</i>	<i>Samp</i>	<i>Rej</i>	<i>Failure Mechanism</i>
STRESS: SER – ALPHA PARTICLE SEL, 25C/85C/120C, 1.65V/3.3V/5.5V							
7C1710614GE	0	0	UMC	COMP	3	0	
STRESS: SER – NEUTRON SEL, 85C/125C, 5.25V							
7C17165A	0	0	UMC	COMP	3	0	
STRESS: TEMPERATURE CYCLE COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1061G30 (7CC171061A)	9313001	611348183	CML-RA	500	80	0	
CY7C1061G30 (7CC171061A)	9313001	611348183	CML-RA	1000	79	0	
CY7C1061G30 (7CC171061A)	9313001	611348182	CML-RA	500	80	0	
CY7C1061G30 (7CC171061A)	9313001	611348182	CML-RA	1000	78	0	
CY7C1061G30 (7CP1710612A)	9313001	611420263	CML-RA	500	80	0	
CY7C1061G30 (7CP1710612A)	9313001	611420263	CML-RA	1000	80	0	
CY7C1061G30 (7CC171061A)	9313001	611348184	CML-RA	500	80	0	
CY7C1061G30 (7CC171061A)	9313001	611348184	CML-RA	1000	80	0	
STRESS: X-SECTION/STEM XY AUDIT							
7C17165A	9302002	0	UMC	COMP	1WF	0	

Reliability Test Data

QTP #:144804

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-CHARGE DEVICE MODEL							
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	500	9	0	
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	1000	3	0	
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	1250	3	0	
STRESS: ESD-HUMAN BODY MODEL							
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	1100	3	0	
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	2200	8	0	
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	3300	3	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, 1.44V							
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	96	927	0	
CY62167G30 (7CC172167A)	9438001	611503292	G-TAIWAN	96	695	0	
STRESS: STATIC LATCH-UP TESTING, 85C, 8.25V, +/-140mA							
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 85C, 9.1V, +/-200mA							
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 8.25V, +/-140mA							
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	COMP	3	0	
YIELD: CLASS							
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	COMP	EQUIVALENT		
YIELD: E-TEST							
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	COMP	EQUIVALENT		
YIELD: SORT							
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	COMP	EQUIVALENT		

Reliability Test Data

QTP #:145003

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC, MSL3							
CY62147GE30 (7CP1721473A)	9507001	611513199	CML-RA	COMP	15	0	
CY62147GE30 (7CP1721473A)	9508002	611520638	CML-RA	COMP	15	0	
STRESS: ESD-CHARGE DEVICE MODEL							
CY62147GE30 (7CP1721473A)	9507001	611513199	CML-RA	500	9	0	
CY62147GE30 (7CP1721473A)	9507001	611513199	CML-RA	750	3	0	
CY62147GE30 (7CP1721473A)	9507001	611513199	CML-RA	1000	3	0	
CY62147GE30 (7CP1721473A)	9507001	611513199	CML-RA	1250	3	0	
CY7S1041GE30 (7CP1710416A)	9507001	611513220	CML-RA	500	9	0	
CY7S1041GE30 (7CP1710416A)	9507001	611513220	CML-RA	750	3	0	
CY7S1041GE30 (7CP1710416A)	9507001	611513220	CML-RA	1000	3	0	
CY7S1041GE30 (7CP1710416A)	9507001	611513220	CML-RA	1250	3	0	
CY62147GE30 (7CP1721473A)	9507001	611514757	CML-RA	500	9	0	
CY62147GE30 (7CP1721473A)	9507001	611514757	CML-RA	750	3	0	
CY62147GE30 (7CP1721473A)	9507001	611514757	CML-RA	1000	3	0	
CY62147GE30 (7CP1721473A)	9507001	611514757	CML-RA	1250	3	0	
CY7C1041GE30 (7CP1710413A)	9507001	611515056	CML-RA	500	9	0	
CY7C1041GE30 (7CP1710413A)	9507001	611515056	CML-RA	750	3	0	
CY7C1041GE30 (7CP1710413A)	9507001	611515056	CML-RA	1000	3	0	
CY7C1041GE30 (7CP1710413A)	9507001	611515056	CML-RA	1250	3	0	
CY7C1041GE30 (7CP1710413A)	9507001	611515056	CML-RA	1500	3	0	
CY7S1041G30 (7CP1710414A)	9507001	611513575	JT-CHINA	500	9	0	
CY7S1041G30 (7CP1710414A)	9507001	611513575	JT-CHINA	750	3	0	
CY7S1041G30 (7CP1710414A)	9507001	611513575	JT-CHINA	1000	3	0	
CY7S1041G30 (7CP1710414A)	9507001	611513575	JT-CHINA	1250	3	0	
CY7S1041G30 (7CP1710414A)	9507001	611513575	JT-CHINA	1500	3	0	
CY7S1049GE30 (7CP1710496A)	9507001	611515679	JT-CHINA	500	9	0	
CY7S1049GE30 (7CP1710496A)	9507001	611515679	JT-CHINA	750	3	0	
CY7S1049GE30 (7CP1710496A)	9507001	611515679	JT-CHINA	1000	3	0	

Reliability Test Data

QTP #:145003

<i>Device</i>	<i>Fab Lot #</i>	<i>Assy Lot #</i>	<i>Ass Loc</i>	<i>Duration</i>	<i>Samp</i>	<i>Rej</i>	<i>Failure Mechanism</i>
STRESS: ESD-CHARGE DEVICE MODEL							
CY621472G30 (7CP1721472A)	9507001	611515678	JT-CHINA	500	9	0	
CY621472G30 (7CP1721472A)	9507001	611515678	JT-CHINA	750	3	0	
CY621472G30 (7CP1721472A)	9507001	611515678	JT-CHINA	1000	3	0	
CY621472G30 (7CP1721472A)	9507001	611515678	JT-CHINA	1250	3	0	
CY621472G30 (7CP1721472A)	9507001	611515678	JT-CHINA	1500	3	0	
CY621472G30 (7CP1721472A)	9507001	611515678	JT-CHINA	1750	3	0	
CY62147G30 (7CP1721472A)	9507001	611515060	G-TAIWAN	500	9	0	
CY62147G30 (7CP1721472A)	9507001	611515060	G-TAIWAN	750	3	0	
CY62147G30 (7CP1721472A)	9507001	611515060	G-TAIWAN	1000	3	0	
CY62147G30 (7CP1721472A)	9507001	611515060	G-TAIWAN	1250	3	0	
CY62147G30 (7CP1721472A)	9507001	611515060	G-TAIWAN	1500	3	0	
CY62147G30 (7CP1721472A)	9507001	611515060	G-TAIWAN	1750	3	0	
CY62148G (7CP172148A)	9507001	611513574	JT-CHINA	500	9	0	
CY62148G (7CP172148A)	9507001	611513574	JT-CHINA	750	3	0	
CY7S1049GE30 (7CP1710496A)	9507001	611515680	JT-CHINA	500	9	0	
CY7S1049GE30 (7CP1710496A)	9507001	611515680	JT-CHINA	750	3	0	
CY7S1049GE30 (7CP1710496A)	9507001	611515680	JT-CHINA	1000	3	0	
CY7S1049GE30 (7CP1710496A)	9507001	611515680	JT-CHINA	1250	3	0	
CY7S1041G30 (7CP1710414A)	9507001	611515681	JT-CHINA	500	9	0	
CY7S1041G30 (7CP1710414A)	9507001	611515681	JT-CHINA	750	3	0	
CY7S1041G30 (7CP1710414A)	9507001	611515681	JT-CHINA	1000	3	0	
CY7S1041G30 (7CP1710414A)	9507001	611515681	JT-CHINA	1250	3	0	
CY7S1041G30 (7CP1710414A)	9507001	611515681	JT-CHINA	1500	3	0	
CY7C1041GE30 (7CP1710413A)	9507001	611515682	JT-CHINA	500	9	0	
CY7C1041GE30 (7CP1710413A)	9507001	611515682	JT-CHINA	750	3	0	
CY7C1041GE30 (7CP1710413A)	9507001	611515682	JT-CHINA	1000	3	0	
CY7C1041GE30 (7CP1710413A)	9507001	611515682	JT-CHINA	1250	3	0	

Reliability Test Data

QTP #:145003

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-CHARGE DEVICE MODEL							
CY7C1041GE30 (7CP1710413A)	9507001	611515682	JT-CHINA	1500	3	0	
CY7C1041GE30 (7CP1710413A)	9507001	611515682	JT-CHINA	1750	3	0	
CY7C1041GE30 (7CP1710413A)	9507001	611515682	JT-CHINA	2000	3	0	
CY62148G (7CP172148A)	9507001	611513173	T-TAIWAN	500	18	0	
CY62148G (7CP172148A)	9507001	611513173	T-TAIWAN	750	9	0	
STRESS: ESD-HUMAN BODY MODEL							
CY62147GE30 (7CP1721473A)	9507001	611513199	CML-RA	1100	3	0	
CY62147GE30 (7CP1721473A)	9507001	611513199	CML-RA	2200	8	0	
CY62147GE30 (7CP1721473A)	9507001	611513199	CML-RA	3300	3	0	
CY62147GE30 (7CP1721473A)	9507001	611513199	CML-RA	4000	3	0	
CY62147GE30 (7CP1721473A)	9507001	611513199	CML-RA	5000	3	0	
CY62147GE30 (7CP1721473A)	9507001	611513199	CML-RA	6000	3	0	
CY62147GE30 (7CP1721473A)	9507001	611513199	CML-RA	7000	3	0	
CY62147GE30 (7CP1721473A)	9507001	611513199	CML-RA	8000	3	0	
CY7S1041GE30 (7CP1710416A)	9507001	611513220	CML-RA	1100	3	0	
CY7S1041GE30 (7CP1710416A)	9507001	611513220	CML-RA	2200	8	0	
CY7S1041GE30 (7CP1710416A)	9507001	611513220	CML-RA	3300	3	0	
CY7S1041GE30 (7CP1710416A)	9507001	611513220	CML-RA	4000	3	0	
CY7S1041GE30 (7CP1710416A)	9507001	611513220	CML-RA	5000	3	0	
CY7S1041GE30 (7CP1710416A)	9507001	611513220	CML-RA	6000	3	0	
CY7S1041GE30 (7CP1710416A)	9507001	611513220	CML-RA	7000	3	0	
CY7S1041GE30 (7CP1710416A)	9507001	611513220	CML-RA	8000	3	0	
CY62147GE30 (7CP1721473A)	9507001	611514757	CML-RA	1100	3	0	
CY62147GE30 (7CP1721473A)	9507001	611514757	CML-RA	2200	8	0	
CY62147GE30 (7CP1721473A)	9507001	611514757	CML-RA	3300	3	0	
CY62147GE30 (7CP1721473A)	9507001	611514757	CML-RA	4000	3	0	
CY62147GE30 (7CP1721473A)	9507001	611514757	CML-RA	5000	3	0	

Reliability Test Data

QTP #:145003

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-HUMAN BODY MODEL							
CY62147GE30 (7CP1721473A)	9507001	611514757	CML-RA	6000	3	0	
CY62147GE30 (7CP1721473A)	9507001	611514757	CML-RA	7000	3	0	
CY62147GE30 (7CP1721473A)	9507001	611514757	CML-RA	8000	3	0	
CY7C1041GE30 (7CP1710413A)	9507001	611515056	CML-RA	1100	3	0	
CY7C1041GE30 (7CP1710413A)	9507001	611515056	CML-RA	2200	8	0	
CY7C1041GE30 (7CP1710413A)	9507001	611515056	CML-RA	3300	3	0	
CY7C1041GE30 (7CP1710413A)	9507001	611515056	CML-RA	4000	3	0	
CY7C1041GE30 (7CP1710413A)	9507001	611515056	CML-RA	5000	3	0	
CY7C1041GE30 (7CP1710413A)	9507001	611515056	CML-RA	6000	3	0	
CY7C1041GE30 (7CP1710413A)	9507001	611515056	CML-RA	7000	3	0	
CY7C1041GE30 (7CP1710413A)	9507001	611515056	CML-RA	8000	3	0	
CY7S1041G30 (7CP1710414A)	9507001	611513575	JT-CHINA	1100	3	0	
CY7S1041G30 (7CP1710414A)	9507001	611513575	JT-CHINA	2200	8	0	
CY7S1041G30 (7CP1710414A)	9507001	611513575	JT-CHINA	3300	3	0	
CY7S1041G30 (7CP1710414A)	9507001	611513575	JT-CHINA	4000	3	0	
CY7S1041G30 (7CP1710414A)	9507001	611513575	JT-CHINA	5000	3	0	
CY7S1041G30 (7CP1710414A)	9507001	611513575	JT-CHINA	6000	3	0	
CY7S1041G30 (7CP1710414A)	9507001	611513575	JT-CHINA	7000	3	0	
CY7S1041G30 (7CP1710414A)	9507001	611513575	JT-CHINA	8000	3	0	
CY7S1049GE30 (7CP1710496A)	9507001	611515679	JT-CHINA	1100	3	0	
CY7S1049GE30 (7CP1710496A)	9507001	611515679	JT-CHINA	2200	8	0	
CY7S1049GE30 (7CP1710496A)	9507001	611515679	JT-CHINA	3300	3	0	
CY7S1049GE30 (7CP1710496A)	9507001	611515679	JT-CHINA	4000	3	0	
CY7S1049GE30 (7CP1710496A)	9507001	611515679	JT-CHINA	5000	3	0	
CY7S1049GE30 (7CP1710496A)	9507001	611515679	JT-CHINA	6000	3	0	
CY7S1049GE30 (7CP1710496A)	9507001	611515679	JT-CHINA	7000	3	0	
CY7S1049GE30 (7CP1710496A)	9507001	611515679	JT-CHINA	8000	3	0	

Reliability Test Data

QTP #:145003

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-HUMAN BODY MODEL							
CY621472G30 (7CP1721472A)	9507001	611515678	JT-CHINA	1100	3	0	
CY621472G30 (7CP1721472A)	9507001	611515678	JT-CHINA	2200	8	0	
CY621472G30 (7CP1721472A)	9507001	611515678	JT-CHINA	3300	3	0	
CY621472G30 (7CP1721472A)	9507001	611515678	JT-CHINA	4000	3	0	
CY621472G30 (7CP1721472A)	9507001	611515678	JT-CHINA	5000	3	0	
CY621472G30 (7CP1721472A)	9507001	611515678	JT-CHINA	6000	3	0	
CY621472G30 (7CP1721472A)	9507001	611515678	JT-CHINA	7000	3	0	
CY621472G30 (7CP1721472A)	9507001	611515678	JT-CHINA	8000	3	0	
CY62147G30 (7CP1721472A)	9507001	611515060	G-TAIWAN	1100	3	0	
CY62147G30 (7CP1721472A)	9507001	611515060	G-TAIWAN	2200	8	0	
CY62147G30 (7CP1721472A)	9507001	611515060	G-TAIWAN	3300	3	0	
CY62147G30 (7CP1721472A)	9507001	611515060	G-TAIWAN	4000	3	0	
CY62147G30 (7CP1721472A)	9507001	611515060	G-TAIWAN	5000	3	0	
CY62147G30 (7CP1721472A)	9507001	611515060	G-TAIWAN	6000	3	0	
CY62147G30 (7CP1721472A)	9507001	611515060	G-TAIWAN	7000	3	0	
CY62148G (7CP172148A)	9507001	611513574	JT-CHINA	1100	3	0	
CY62148G (7CP172148A)	9507001	611513574	JT-CHINA	2200	8	0	
CY62148G (7CP172148A)	9507001	611513574	JT-CHINA	3300	3	0	
CY62148G (7CP172148A)	9507001	611513574	JT-CHINA	4000	3	0	
CY62148G (7CP172148A)	9507001	611513574	JT-CHINA	5000	3	0	
CY62148G (7CP172148A)	9507001	611513574	JT-CHINA	6000	3	0	
CY62148G (7CP172148A)	9507001	611513574	JT-CHINA	7000	3	0	
CY62148G (7CP172148A)	9507001	611513574	JT-CHINA	8000	3	0	
CY62148G (7CP172148A)	9507001	611513173	T-TAIWAN	1100	3	0	
CY62148G (7CP172148A)	9507001	611513173	T-TAIWAN	2200	8	0	
CY62148G (7CP172148A)	9507001	611513173	T-TAIWAN	3300	3	0	
CY62148G (7CP172148A)	9507001	611513173	T-TAIWAN	4000	3	0	
CY62148G (7CP172148A)	9507001	611513173	T-TAIWAN	5000	3	0	

Reliability Test Data

QTP #:145003

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-HUMAN BODY MODEL							
CY62148G (7CP172148A)	9507001	611513173	T-TAIWAN	6000	3	0	
CY62148G (7CP172148A)	9507001	611513173	T-TAIWAN	7000	3	0	
CY62148G (7CP172148A)	9507001	611513173	T-TAIWAN	8000	3	0	
STRESS: ESD-MACHINE MODEL							
CY62147GE30 (7CP1721473A)	9507001	611513199	CML-RA	200	5	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, 1.44V							
CY7C1041G30 (7CP171041A)	9507001	611516374	CML-RA	96	1549	0	
CY62147G30 (7CP172147A)	9507001	611516367	CML-RA	96	1543	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE REGULATOR ON, 125C, 1.44V							
CY62147G30 (7CP172147A)	9507001	611516367	CML-RA	96	500		
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, 1.44V							
CY62147GE30 (7CP1721473A)	9507001	611513199	CML-RA	168	193	0	
CY62147GE30 (7CP1721473A)	9507001	611513199	CML-RA	1000	193	0	
CY62147G30 (7CP172147A)	9507001	611510721	CML-RA	168	197	0	
CY62147G30 (7CP172147A)	9507001	611510721	CML-RA	1000	197	0	
CY7C1041G30 (7CP171041A)	9507001	611516374	CML-RA	168	198	0	
CY7C1041G30 (7CP171041A)	9507001	611516374	CML-RA	1000	198	0	
CY62147G30 (7CP172147A)	9507001	611516367	CML-RA	168	191	0	
CY62147G30 (7CP172147A)	9507001	611516367	CML-RA	1000	191	0	
STRESS: PRE/POST LFR CRITICAL PARAMETERS							
CY7C1041G30 (7CP171041A)	9507001	611516374	CML-RA	0	10+2	0	
CY7C1041G30 (7CP171041A)	9507001	611516374	CML-RA	168	10+2	0	
CY7C1041G30 (7CP171041A)	9507001	611516374	CML-RA	500	10+2	0	
CY62147G30 (7CP172147A)	9507001	611516367	CML-RA	0	10+2	0	
CY62147G30 (7CP172147A)	9507001	611516367	CML-RA	168	10+2	0	
CY62147G30 (7CP172147A)	9507001	611516367	CML-RA	500	10+2	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY62147GE30 (7CP1721473A)	9507001	611513199	CML-RA	168	79	0	
CY62147GE30 (7CP1721473A)	9507001	611513199	CML-RA	288	78	0	

Reliability Test Data

QTP #:145003

<i>Device</i>	<i>Fab Lot #</i>	<i>Assy Lot #</i>	<i>Assy Loc</i>	<i>Duration</i>	<i>Samp</i>	<i>Rej</i>	<i>Failure Mechanism</i>
STRESS: SER – ALPHA PARTICLE							
CY62147GE30 (7CP1721473A)	9507001	611513199	CML-RA	COMP	3	0	
STRESS: SER – NEUTRON							
CY62147GE30 (7CP1721473A)	9507001	611513199	CML-RA	COMP	3	0	
CY7S1041G30 (7CP1710414A)	9507001	611513575	JT-CHINA	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 85C, 8.25V, +/-140mA							
CY62147GE30 (7CP1721473A)	9507001	611513199	CML-RA	COMP	6	0	
CY7S1041GE30 (7CP1710416A)	9507001	611513220	CML-RA	COMP	6	0	
CY62147GE30 (7CP1721473A)	9507001	611514757	CML-RA	COMP	6	0	
CY7C1041GE30 (7CP1710413A)	9507001	611515056	CML-RA	COMP	6	0	
CY7S1041G30 (7CP1710414A)	9507001	611513575	JT-CHINA	COMP	6	0	
CY7S1049GE30 (7CP1710496A)	9507001	611515679	JT-CHINA	COMP	6	0	
CY621472G30 (7CP1721472A)	9507001	611515678	JT-CHINA	COMP	6	0	
CY62147G30 (7CP1721472A)	9507001	611515060	G-TAIWAN	COMP	6	0	
CY62148G (7CP172148A)	9507001	611513574	JT-CHINA	COMP	6	0	
CY62148G (7CP172148A)	9507001	611513173	T-TAIWAN	COMP	6	0	
STRESS: STATIC LATCH-UP TESTING, 85C, 9.1V, +/-200mA							
CY62147GE30 (7CP1721473A)	9507001	611513199	CML-RA	COMP	3	0	
CY7S1041GE30 (7CP1710416A)	9507001	611513220	CML-RA	COMP	3	0	
CY62147GE30 (7CP1721473A)	9507001	611514757	CML-RA	COMP	3	0	
CY7C1041GE30 (7CP1710413A)	9507001	611515056	CML-RA	COMP	3	0	
CY7S1041G30 (7CP1710414A)	9507001	611513575	JT-CHINA	COMP	3	0	
CY7S1049GE30 (7CP1710496A)	9507001	611515679	JT-CHINA	COMP	3	0	
CY621472G30 (7CP1721472A)	9507001	611515678	JT-CHINA	COMP	3	0	
CY62147G30 (7CP1721472A)	9507001	611515060	G-TAIWAN	COMP	3	0	
CY62148G (7CP172148A)	9507001	611513574	JT-CHINA	COMP	3	0	
CY62148G (7CP172148A)	9507001	611513173	T-TAIWAN	COMP	3	0	

Reliability Test Data

QTP #:145003

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: STATIC LATCH-UP TESTING, 125C, 8.25V, +/-140mA							
CY62147GE30 (7CP1721473A)	9507001	611513199	CML-RA	COMP	3	0	
CY7S1041GE30 (7CP1710416A)	9507001	611513220	CML-RA	COMP	3	0	
CY62147GE30 (7CP1721473A)	9507001	611514757	CML-RA	COMP	3	0	
CY7C1041GE30 (7CP1710413A)	9507001	611515056	CML-RA	COMP	3	0	
CY7S1041G30 (7CP1710414A)	9507001	611513575	JT-CHINA	COMP	3	0	
CY7S1049GE30 (7CP1710496A)	9507001	611515679	JT-CHINA	COMP	3	0	
CY621472G30 (7CP1721472A)	9507001	611515678	JT-CHINA	COMP	3	0	
CY62147G30 (7CP1721472A)	9507001	611515060	G-TAIWAN	COMP	3	0	
CY62148G (7CP172148A)	9507001	611513574	JT-CHINA	COMP	3	0	
CY62148G (7CP172148A)	9507001	611513173	T-TAIWAN	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 85C, 9.1V, +/-300mA							
CY62147GE30 (7CP1721473A)	9507001	611513199	CML-RA	COMP	3	0	
CY7S1041GE30 (7CP1710416A)	9507001	611513220	CML-RA	COMP	3	0	
CY62147GE30 (7CP1721473A)	9507001	611514757	CML-RA	COMP	3	0	
CY7C1041GE30 (7CP1710413A)	9507001	611515056	CML-RA	COMP	3	0	
CY7S1041G30 (7CP1710414A)	9507001	611513575	JT-CHINA	COMP	3	0	
CY7S1049GE30 (7CP1710496A)	9507001	611515679	JT-CHINA	COMP	3	0	
CY621472G30 (7CP1721472A)	9507001	611515678	JT-CHINA	COMP	3	0	
CY62147G30 (7CP1721472A)	9507001	611515060	G-TAIWAN	COMP	3	0	
CY62148G (7CP172148A)	9507001	611513574	JT-CHINA	COMP	3	0	
CY62148G (7CP172148A)	9507001	611513173	T-TAIWAN	COMP	3	0	
STRESS: TEMPERATURE CYCLE COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY62147G30 (7CP172147A)	9507001	611516367	CML-RA	500	80	0	
CY62147GE30 (7CP1721473A)	9508002	611520638	CML-RA	500	80	0	

Reliability Test Data

QTP #:192409

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-CHARGE DEVICE MODEL							
CY62147G30 (7CP172147A)	9827018	611909873	CML-RA	500	9	0	
CY62147G30 (7CP172147A)	9827018	611909873	CML-RA	1000	3	0	
CY62147G30 (7CP172147A)	9827018	611909873	CML-RA	1250	3	0	
STRESS: ESD-HUMAN BODY MODEL							
CY62147G30 (7CP172147A)	9827018	611909873	CML-RA	1100	3	0	
CY62147G30 (7CP172147A)	9827018	611909873	CML-RA	2200	8	0	
CY62147G30 (7CP172147A)	9827018	611909873	CML-RA	3300	3	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, 1.44V							
CY62147G30 (7CP172147A)	9827018	611909873	CML-RA	96	1614	0	
CY62147G309 (7CP172147A)	9827018	612024937	CML-RA	96	1961	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, 1.44V							
CY62147G30 (7CP172147A)	9827018	611909873	CML-RA	1000	120	0	
CY62147G30 (7CP172147A)	9827018	611909873	CML-RA	2000	120	0	
STRESS: PRE/POST LFR CRITICAL PARAMETERS							
CY62147G30 (7CP172147A)	9827018	611909873	CML-RA	0	10+2	0	
CY62147G30 (7CP172147A)	9827018	611909873	CML-RA	1000	10+2	0	
STRESS: STATIC LATCH-UP TESTING, 85C, 9.1V, +/-140mA							
CY62147G30 (7CP172147A)	9827018	611909873	CML-RA	COMP	2	0	
STRESS: STATIC LATCH-UP TESTING, 85C, 9.1V, +/-200mA							
CY62147G30 (7CP172147A)	9827018	611909873	CML-RA	COMP	2	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 8.25V, +/-100mA							
CY62147G30 (7CP172147A)	9827018	611909873	CML-RA	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 9.1V, +/-140mA							
CY62147G30 (7CP172147A)	9827018	611909873	CML-RA	COMP	2	0	

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Cypress Semiconductor Corporation

CY6214XEV30/ELL/ESL Characterization Report

4 Mbit Static RAM

Design Engineering Director or Manager

Prashant Saxena

psc@cypress.com

Product Engineering Director

Shailesh Chauhan

svc@cypress.com

Product Engineer

Mark Lindsey Magboo

qoo@cypress.com

Applications Engineer

Vinay Manikkoth

vini@cypress.com

Marketing Engineer

Karthik Rangarajan

karr@cypress.com



www.cypress.com

198 Champion Ct.
San Jose, CA 95134 USA

Tel: (408) 943 2600

Fax: (408) 943 4730

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2.0 Introduction

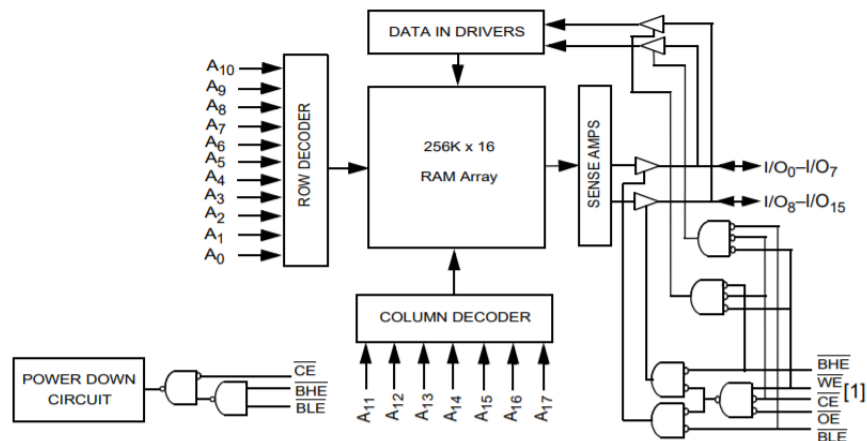
2.1 General Description

The CY62147EV30 is a high performance CMOS static RAM (SRAM) organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra low active current. It is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99 percent when deselected (CE HIGH or both BLE and BHE are HIGH). The input and output pins (I/O0 through I/O15) are placed in a high impedance state when:

- Deselected (CE HIGH)
- Outputs are disabled (OE HIGH)
- Both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH)
- Write operation is active (CE LOW and WE LOW) To write to the device, take Chip Enable (CE) and Write Enable (WE) inputs LOW.

If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O0 through I/O7) is written into the location specified on the address pins (A0 through A17). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O8 through I/O15) is written into the location specified on the address pins (A0 through A17). To read from the device, take Chip Enable (CE) and Output Enable (OE) LOW while forcing the Write Enable (WE) HIGH. If Byte Low enable (BLE) is LOW, then data from the memory location specified by the address pins appear on I/O0 to I/O7. If Byte High enable (BHE) is LOW, then data from memory appears on I/O8 to I/O15.

Logic Block Diagram



Pin Configurations – X16

Figure 1. 48-ball VFBGA pinout (Single Chip Enable)

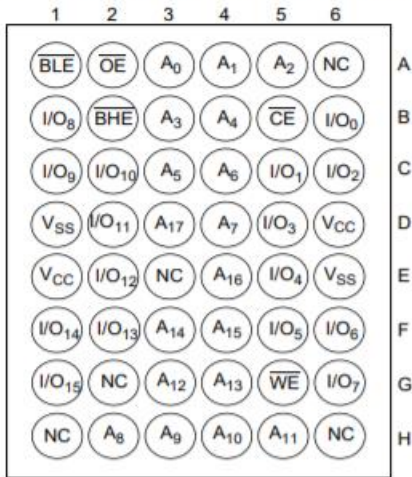


Figure 2. 48-ball VFBGA pinout (Dual Chip Enable)



Figure 3. 44-pin TSOP II pinout (Single Chip Enable)

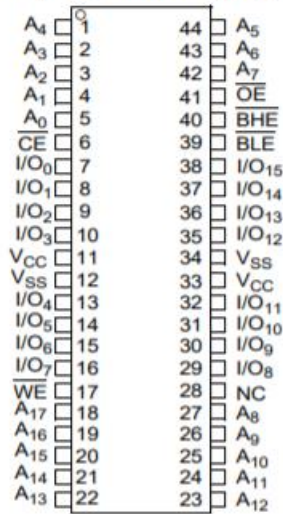
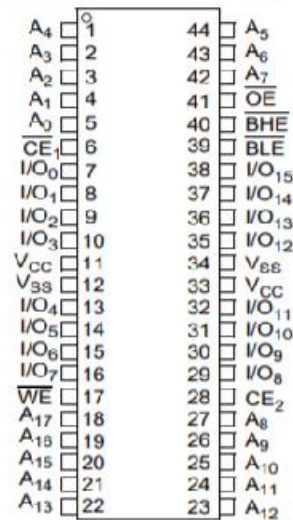


Figure 4. 44-pin TSOP II (Dual Chip Enable)



Pin Configurations – X8

Figure 5. 36-ball VFBGA pinout
Top View

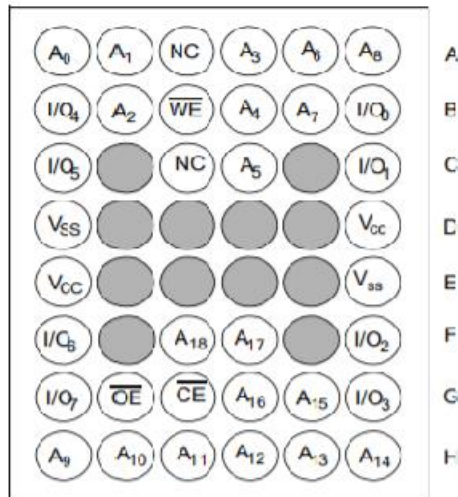
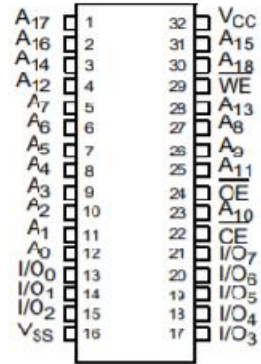


Figure 6. 32-pin SOIC/T SOP II pinout
Top View



2.2 Datasheet

The CY6214XE30/ELL/ESL meets all datasheet specifications. The datasheet is available from the Cypress Website at:

[CY62147EV30 Datasheet](#)

[CY62146ESL Datasheet](#)

[CY62146ELL Datasheet](#)

[CY621472E30 Datasheet](#)

2.3 Application Notes

The CY6214XE30/ELL/ESL has the following associated Application Notes at this time. The Application Notes are available from the Cypress website at the URL provided below.

[AN44517](#) - Design Recommendation for Battery-Backed SRAMs Using Cypress MoBL® SRAMs

2.4 White Papers

The CY6214XE30/ELL/ESL has no associated White Papers at this time.

2.5 Qualification Report

The CY6214XE30/ELL/ESL is qualified under QTP 192409.

3.0 Characterization Hardware and Setup

3.1 Measurement System and Hardware

The following equipments and hard wares are used for the DC and AC parametric characterization of this device.

3.1.1 Characterization Board

All the DC parameters and the AC parameters were measured using 48TSOP1 package with the D1054 hand test interface board and 48VFBGA package with D84348 board connected to L042 load board. Pin capacitance was measured using the probe card type board.

3.1.2 ATE

Advantest 5581P tester was used for the DC and AC parameter characterization.

3.1.3 Temperature Forcing System

Temptronics TP04310A Precision Temperature Forcing System was used to force ambient temperature.

3.1.4 Frequency LCR Meter

HP4284A LCR Meter was used to measure input and output pin capacitance.

3.1.5 Power Supply

The Kiethley 2400 Source Meter was used to supply power for device for pin capacitance measurement.

3.2 Characterization Conditions and Parameters

Characterization was done on the following device and conditions as listed in [Table 1](#). Units used for characterization are quick builds and chosen randomly unless specified.

Table 1. Characterization Conditions and Parameters

Parameter	Device	Fab Lot	Assy Lot	# of Devices	Voltage Variation (V)	Temperature Variation (°C)
DC & AC	CY62147EV30LL-45ZSXI	9827018	611909873	30	2.2V-3.6V, 4.5V-5.5V	-40, 25, 85

The part is qualified for a new technology and fabrication site. The below tables compare the characterization results for the current technology and the new technology.

4.0 DC Characterization

4.1 DC Characterization Summary over V_{DD} and Temperature

Table 2. DC Characterization Results across V_{DD} and Temperature

Parameter	Description		Test Conditions	Datasheet (45ns)			90nm Skywater fab (current)			65nm UMC fab (New)			Unit	
				Min	Typ	Max	Min	Mean	Max	Min	Mean	Max		
V_{OH}	Output HIGH voltage	2.2V to 2.7V	$VCC = \text{Min}, IOH = -0.1 \text{ mA}$	2.0	-	-	2.16	2.16	2.17	2.16	2.18	2.19	V	
		2.7V to 3.6V	$VCC = \text{Min}, IOH = -1.0 \text{ mA}$	2.4	-	-	2.61	2.62	2.63	2.61	2.65	2.65		
		4.5V to 5.5V	$VCC = \text{Min}, IOH = -1.0 \text{ mA}$	2.4	-	-	2.65	2.74	2.85	4.44	4.44	4.45		
V_{OL}	Output LOW voltage	2.2V to 2.7V	$VCC = \text{Min}, IOL = 0.1 \text{ mA}$	-	-	0.4	0.032	0.033	0.040	0.024	0.027	0.040	V	
		2.7V to 3.6V	$VCC = \text{Min}, IOL = 2.1 \text{ mA}$	-	-	0.4	0.108	0.111	0.114	0.070	0.073	0.082		
		4.5V to 5.5V	$VCC = \text{Min}, IOL = 2.1 \text{ mA}$	-	-	0.4	0.104	0.107	0.110	0.056	0.068	0.080		
V_{IH}	Input HIGH voltage	2.2V to 2.7V		1.8	-	$VCC + 0.3$	1.22	1.26	1.29	1.39	1.44	1.50	V	
		2.7V to 3.6V		2.0	-	$VCC + 0.3$	1.58	1.67	1.78	1.39	1.44	1.50		
		4.5V to 5.5V		2.0	-	$VCC + 0.5$	1.61	1.71	1.84	1.42	1.46	1.51		
V_{IL}	Input LOW voltage	2.2V to 2.7V		-0.3	-	0.6	0.84	0.88	0.92	0.80	0.90	1.03	V	
		2.7V to 3.6V		-0.3	-	0.8	0.96	0.99	1.02	1.07	1.16	1.21		
		4.5V to 5.5V		-0.5	-	0.8	1.11	1.16	1.21	1.04	1.07	1.10		
I_{IX}	Input leakage current		$GND < V_{IN} < VCC$	-1.0	-	1.0	-0.02	0.02	0.06	-0.04	0.04	0.12	μA	
I_{OZ}	Output leakage current		$GND < V_{OUT} < VCC$, Output disabled	-1.0	-	1.0	-0.02	0.02	0.06	-0.02	0.01	0.04	μA	
I_{CC}	Operating supply current		$VCC = \text{Max}, I_{OUT} = 0 \text{ mA}, \text{ CMOS levels}$	$f = 1 \text{ MHz}$	-	3.5	6	1.69	1.87	1.99	1.85	2.31	3.33	mA
				$f = f_{\text{max}} = 1/RC$	-	15	20	14.92	16.03	17.12	12.60	13.35	14.80	
I_{sb1}	Automatic Power-down Current – CMOS Inputs;		$CE1 > VCC - 0.2 \text{ V}$ or $CE2 < 0.2 \text{ V}$ or $(BHE \text{ and } BLE) > VCC - 0.2 \text{ V}$, $V_{IN} > VCC - 0.2 \text{ V}$, $V_{IN} < 0.2 \text{ V}$, $f = f_{\text{max}}$ (address and data only), $f = 0$ (OE, and WE), $VCC = VCC(\text{max})$	-	2.5	7	1.94	2.31	2.74	4.10	4.52	5.14	μA	
I_{sb2}	Current – CMOS Inputs		$CE1 > VCC - 0.2 \text{ V}$ or $CE2 < 0.2 \text{ V}$ or $(BHE \text{ and } BLE) > VCC - 0.2 \text{ V}$, $V_{IN} > VCC - 0.2 \text{ V}$ or $V_{IN} < 0.2 \text{ V}$, $f = 0$, $VCC = VCC(\text{max})$	-	2.5	7	1.70	2.17	2.90	4.12	4.59	5.20	μA	

Capacitance

Parameter	Description	Test Conditions	Datasheet	90nm Skywater fab (current)	65nm UMC fab (New)	Unit
C _{IN}	Input capacitance	TA = 25 °C, f = 1 MHz, VCC = VCC(typ)	10	7.8	7.2	pF
C _{OUT}	Output capacitance		10	6.8	5.7	pF

Data Retention Characteristics

Parameter	Description	Test Conditions	Datasheet (45ns)			90nm Skywater fab (current)			65nm UMC fab (New)			Unit
			Min	Typ	Max	Min	Mean	Max	Min	Mean	Max	
V _{DR}	VCC for data retention		1.5	-	-	Pass	-	-	Pass	-	-	V
I _{CCDR}	Data retention current	VCC = 1.5 V, CE > VCC - 0.2 V, VIN > VCC - 0.2 V or VIN < 0.2 V	-	3	8.8	1.74	2.00	2.42	4.50	4.95	5.60	uA
t _{CDR}	Chip deselect to data retention time		0	-	-	Pass	-	-	Pass	-	-	V
t _R	Operation recovery time		45	-	-	pass	-	-	Pass	-	-	ns

5.0 AC Characterization

5.1 AC Characterization Summary over V_{DD} and Temperature

Table 4. AC Characterization Results across V_{DD} and Temperature

Parameter	Description	Datasheet (45ns)		90nm Skywater fab (current)			65nm UMC fab (New)			Unit
		Min	Max	Min	Mean	Max	Min	Mean	Max	
Read Cycle										
t _{RC}	Read cycle time	45.0	-	Pass	-	-	Pass	-	-	ns
t _{AA}	Address to data valid	-	45.0	26.06	29.40	34.19	16.21	17.37	19.02	ns
t _{OHA}	Data hold from address change	10.0	-	13.37	14.69	16.44	15.45	15.85	16.39	ns
t _{ACE}	CEB LOW to data valid	-	45.0	28.00	29.99	34.94	31.19	33.04	34.94	ns
t _{DOE}	OEB LOW to data valid	-	22.0	9.62	10.70	12.31	7.63	8.36	9.44	ns
t _{LZOE}	OEB LOW to low-Z	5	-	7.65	7.74	7.75	7.65	7.74	7.75	ns
t _{HZOE}	OEB HIGH to high-Z	-	18.0	5.65	5.80	5.87	5.73	5.87	5.93	ns
t _{LZCE}	CEB LOW to low-Z	10.0	-	27.80	27.83	27.90	27.75	27.82	27.90	ns
t _{HZCE}	CEB LOW to low-Z	-	18.0	6.05	6.10	6.15	6.03	6.15	6.28	ns
t _{PU}	CEB LOW to power-up	0	-	pass	-	-	pass	-	-	ns
t _{pd}	CEB HIGH to power-down	-	45.0	-	-	pass	-	-	pass	ns
t _{DBE}	Byte enable to data valid	-	45.0	28.56	31.85	37.06	30.13	32.01	33.94	ns
t _{LZBE}	Byte enable to low-Z	5	-	28.13	28.20	28.28	27.18	28.09	28.23	ns
t _{HZBE}	Byte disable to high-Z	-	18.0	6.03	6.08	6.15	6.03	6.10	6.18	ns

Parameter	Description	Datasheet (45ns)		90nm Skywater fab (current)			65nm UMC fab (New)			Unit
		Min	Max	Min	Mean	Max	Min	Mean	Max	
Write Cycle										
t _{WC}	Write cycle time	45.0	-	pass	-	-	pass	-	-	ns
t _{SCE}	CE LOW to write end	-	35.0	15.00	17.88	21.31	26.44	27.63	29.62	ns
t _{AW}	Address setup to write end	-	35.0	13.06	15.56	18.37	27.56	28.62	30.37	ns
t _{HA}	Address hold from write end	0	-	-6.56	-5.81	-5.12	-13.94	-12.91	-11.87	ns
t _{SA}	Address setup to write start	0	-	-9.00	-8.12	-7.50	-9.81	-8.80	-8.25	ns
t _{PWE}	WE pulse width	-	35.0	12.19	14.17	17.31	7.44	7.94	8.94	ns
t _{BW}	Byte Enable to write end	-	35.0	16.37	19.77	23.87	27.75	28.93	30.88	ns
t _{SD}	Data setup to write end	-	25.0	9.94	11.08	12.62	6.19	6.54	7.00	ns
t _{HD}	Data hold from write end	0	-	-6.31	-5.66	-5.00	-3.31	-2.91	-2.50	ns
t _{HZWE}	WE LOW to high-Z	-	18.0	6.21	6.22	6.23	6.20	6.22	6.24	ns
t _{LZWE}	WE HIGH to low-Z	10.0	-	15.70	15.78	15.85	15.85	15.89	15.93	ns

Document History Page

Rev.	ECN No.	Orig. of Change	Description of Change
**	6960426	ARAV	New Characterization Report

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