Product Change Notification / SYST-28MDSQ101

Date:

10-Aug-2020

Product Category:

16-Bit - Microcontrollers and Digital Signal Controllers

PCN Type:

Silicon Die Revision

Notification Subject:

ERRATA - dsPIC33CK64MP105 Family Silicon Errata and Data Sheet Clarification

Affected CPNs:

SYST-28MDSQ101_Affected_CPN_08102020.pdf
SYST-28MDSQ101_Affected_CPN_08102020.csv

Notification Text:

SYST-28MDSQ101

Microchip has released a new Product Documents for the dsPIC33CK64MP105 Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at dsPIC33CK64MP105 Family Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change:
1) Added silicon revision A2.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Estimated First Ship Date: 10 Aug 2020

NOTE: Please be advised that after the estimated first ship date customers may receive pre and post change parts.

Markings to Distinguish Revised from Unrevised Devices: Traceability Code

Attachments:

dsPIC33CK64MP105 Family Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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dsPIC33CK64MP105

dsPIC33CK64MP105 Family
Silicon Errata and Data Sheet Clarification

The dsPIC33CK64MP105 family devices that you have received conform functionally to the current Device Data Sheet (DS70005363**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the dsPIC33CK64MP105 silicon.

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A2**).

Data Sheet clarifications and corrections start on page 6, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

> **Note:** If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various dsPIC33CK64MP105 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision	
		A0	A2
dsPIC33CK32MP102	0x8E00	0x0000	0x0002
dsPIC33CK32MP103	0x8E01		
dsPIC33CK32MP105	0x8E02		
dsPIC33CK64MP102	0x8E10		
dsPIC33CK64MP103	0x8E11		
dsPIC33CK64MP105	0x8E12		

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions	
				A0	A2
I2C	Interrupt	1.	In Slave mode, an incorrect interrupt is generated when DHEN = 1.	X	X
I2C	Idle	2.	Module SFR registers are reset in Idle mode.	X	X
I2C	SMBus 3.0	3.	When Configuration bit, SMB3EN (FDEVOPT[10]) = 1, the SMBus 3.0 VIH minimum specification may not be met.	X	
Oscillator	XT, HS	4.	Removed.		
PWM	Dead Time	5.	When feed-forward PCI is used for dead-time compensation (DTCMPSEL = 1), the PWMx outputs are overridden.	X	X
UART	Frame Error	6.	FERR bit will not get set if a Stop bit is received.	X	X
UART	Sleep	7.	SLPEN needs to be set when waking from Sleep with a UART reception.	X	X
UART	Address Detect	8.	When writing to UxP1 with UTXBRK = 1, the content of P1 will not get transmitted.	X	X
UART	IrDA®	9.	When the UART is operating in IrDA mode, the received data may be corrupted.	X	X
I/O	POR	10.	Spike on I/O at POR.	X	
ICSP™ Flash Write Inhibit	Flash Write Inhibit	11.	Flash memory cannot be protected against reprogramming.	X	
CPU	FLIM Instruction	12.	When the operands are of different signs, the FLIM instruction may not force the correct data limit.	X	X
CPU	DIV.SD Instruction	13.	Overflow bit is not getting set when an overflow occurs.	X	X
CPU	MAXAB/MINAB/ MINZAB Instructions	14.	MAXAB, MINAB and MINZAB do not work for different sign operands.	X	X
CPU	Byte Mode Instructions	15.	Upper byte of the destination register may not be persistent.	X	X
DMA	ADC Triggers	16.	DMA is triggered continuously from ADC.	X	
I2C	I2C	17.	All instances of I2C may exhibit errors and should not be used.	X	
Oscillator	VCO and AVCO Dividers	18.	Main and auxiliary PLL external VCO dividers can fail to output the clock.	X	X

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A2**).

1. Module: I²C

In Slave mode with DHEN = 1 (Data Hold Enable), if software sends a NACK, a Slave interrupt is asserted at the 9th falling edge of the clock.

Work around

Software should ignore the Slave interrupt that is asserted after sending a NACK.

Affected Silicon Revisions

A0	A2						
X	X						

2. Module: I²C

In Slave mode, the SFRs are reset when the device is in Idle and the module is set for discontinue in Idle (I2CSIDL = 1).

Work around

None.

Affected Silicon Revisions

A0	A2						
X	X						

3. Module: I²C

When selecting SMBus 3.0 operation using Configuration bit, SMB3EN (FDEVOPT[10]), the Voltage Input High (V_{IH}) of the SMBus 3.0 specification minimum may not be met.

Work around

None.

Affected Silicon Revisions

A0	A2						
X							

4. Module: Oscillator

This errata is no longer applicable to any silicon revisions of this product. See **Section 2.5 External Oscillator Pins** in the current device data sheet for guidance on oscillator design to avoid start-up related issues.

5. Module: PWM

When feed-forward PCI is used for dead-time compensation (DTCMPSEL = 1), the PWMx outputs are overridden.

Work around

Use Sync PCI (DTCMPSEL = 0) for dead-time compensation.

Affected Silicon Revisions

A0	A2						
X	X						

6. Module: UART

When UART is operating with STSEL[1:0] = 2, (two Stop bits sent, two checked at receive) and STPMD = 0, the FERR bit will not get set if a Stop bit is received.

Work around

Use STPSEL = 3 instead of STSEL = 2. When operating with STSEL = 3 mode, the UART will be configured to send two Stop bits, but check one at receive.

Affected Silicon Revisions

A0	A2						
X	X						

7. Module: UART

When waking from Sleep with a UART reception, SLPEN needs to be set in addition to WAKE = 1.

Work around

Set the SPLEN bit in addition to WAKE before entering Sleep.

Affected Silicon Revisions

A0	A2						
X	X						

8. Module: UART

In UART Address Detect mode, writing to UxP1 with UTXBRK = 1 should cause a Break to be transmitted, followed by the content in P1, but the content of P1 will not get transmitted.

Work around

After writing to P1, wait for UTXBRK to get clear and then rewrite to P1.

Affected Silicon Revisions

A0	A2						
X	X						

9. Module: UART

When the UART is operating in IrDA® mode, the received data may be corrupted.

Work around

None.

Affected Silicon Revisions

A0	A2						
X	X						

10. Module: I/O

At device power-up, the I/O pins may drive a pulse up to 0.8V for a duration of up to 100 µSec.

Work around

It is recommended to ensure the circuitry that is connected to the pins can endure this pulse.

Example applications affected may include complementary power switches, where a transient current shoot-through might occur.

High-voltage applications with complementary switches should power the high-voltage 200 µSec later than powering the dsPIC® DSC to avoid the issue.

Behavior is specific to each part and not affected by aging.

Affected Silicon Revisions

A0	A2						
X							

11. Module: ICSP™ Flash Write Inhibit

The ICSP Write Inhibit feature does not prevent ICSP Flash erase and program operations, even if the lock values are written.

Work around

None.

Affected Silicon Revisions

A0	A2						
X							

12. Module: CPU

The FLIM instruction may incorrectly limit the data range when operating on signed operands of different sign values. If the operands are either all negative or all positive, the limit is correct.

Work around

None.

Affected Silicon Revisions

A0	A2						
X	X						

13. Module: CPU

When using the Signed 32-by-16-bit Division instruction, DIV.SD, the Overflow bit may not always get set when an overflow occurs.

Work around

Test for and handle overflow conditions outside of the div.sd instruction.

Affected Silicon Revisions

A0	A2						
X	X						

14. Module: CPU

When operating on signed operands of different sign values, the output for MAXAB, MINAB and MINZAB instructions may be incorrect. If the operands are either all negative or all positive, the output is correct.

Work around

None.

Affected Silicon Revisions

A0	A2						
X	X						

15. Module: CPU

When using Byte mode instructions, the upper byte of the destination register may not be persistent.

Work around

None.

Affected Silicon Revisions

A0	A2						
X	X						

16. Module: DMA

The DMA receives multiple continuous triggers from ADC until the trigger event from ADC is cleared. The OVRUNIF flag (DMAINTn[3]) will be set. When the OVRUNIF bit changes state, from '0' to '1', a DMA interrupt is generated.

Work around

Ignore the OVRUNIF bit and the first DMA interrupt. Clear the ADC trigger source, ANxRDY, with a DMA read of the ADC buffer, ADCBUFx, for the corresponding ADC channel.

Affected Silicon Revisions

A0	A2						
X							

17. Module: I^2C

All instances of I^2C/SMBus may exhibit errors and should not be used. When operating I^2C/SMBus in a noisy environment, the I^2C module may exhibit various errors. These errors may include, but are not limited to, corrupted data, unintended interrupts or the I^2C bus getting hung up due to injected noise. Examples of system noise include, but are not limited to, PWM outputs or other pins toggled at high speed adjacent to the I^2C pins. Both Master and Slave I^2C/SMBus modes may exhibit this issue.

Work around

If I^2C is required, use a software I^2C implementation. An example I^2C software library is available from Microchip:
www.microchip.com/dsPIC33C_I2C_SoftwareLibrary

Affected Silicon Revisions

A0	A2						
X							

18. Module: Oscillator

At PLL start-up, the main and auxiliary PLL VCO dividers may occasionally halt and not provide a clock output. The VCO and AVCO dividers can be selected as clock sources for different peripheral modules, including the ADC, PWM, DAC, UART, etc. VCO and AVCO dividers, FVCO/2, FVCO/3, FVCO/4, FVCODIV, AFVCO/2, AFVCO/3, AFVCO/4 and AFVCODIV outputs, are affected.

Work around

1. Use another clock source, such as the FOSC, PLL or APLL output (FPLLO and AFPLLO) instead of the VCO or AVCO dividers.
2. If the application requires the VCO or AVCO divider, test this clock source. System resources, such as a timer, I/O pin state or interrupts can be used to detect and verify peripheral activity for presence of the VCO divider clock output. Any type of Reset may recover the VCO divider clock (Software Reset, WDT, $\overline{MCLR}$ or POR).

Affected Silicon Revisions

A0	A2						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70005363**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (1/2019)

Initial version of this document; issued for revision A0.

Rev B Document (2/2019)

Updated device data sheet revision from B to C.

Rev C Document (3/2019)

Added silicon issue 16 (DMA).

Rev D Document (1/2020)

Added silicon issue 17 (I^2C).

Rev E Document (6/2020)

Added silicon issue 18 (Oscillator).

Removed silicon issue 4 (Oscillator) since it is no longer applicable.

Rev F Document (7/2020)

Added silicon revision A2.

NOTES:

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SYST-28MDSQ101 - ERRATA - dsPIC33CK64MP105 Family Silicon Errata and Data Sheet Clarification

Affected Catalog Part Numbers(CPN)

DSPIC33CK32MP102-E/2N
DSPIC33CK32MP102-E/M6
DSPIC33CK32MP102-E/SS
DSPIC33CK32MP102-H/2N
DSPIC33CK32MP102-H/M6
DSPIC33CK32MP102-H/SS
DSPIC33CK32MP102-I/2N
DSPIC33CK32MP102-I/M6
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