Cypress Semiconductor Corporation – An Infineon Technologies Company
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PRODUCT INFORMATION NOTIFICATION

PIN: PIN202702 **Date:** July 06, 2020

Subject: Datasheet Specification Changes for Select 4-Mbit MoBL® SRAM Industrial Parts

To: VICKI KNAUF
IHS
lcsourcing@ihs.com

Change Type: Minor

Description of Change:
Cypress announces datasheet changes for the industrial-grade 90nm 3.0V and 5.0V 4-Mbit MoBL® family of asynchronous SRAMs. The intent behind these changes is to ensure consistency in the current and future 4-Mbit MoBL SRAM products. Details on the updates to some DC specifications have been provided as an attachment to this notification.

There are no changes to ordering part numbers. Product datasheets can be downloaded from the Cypress Website (www.cypress.com).

Part Numbers Affected: 50
See the attached 'Affected Parts List' file for a list of all part numbers affected by this change.

Approximate Implementation Date:
This change will be implemented effective with the date of this notification.

Anticipated Impact:
Products manufactured are completely compatible with existing product from form, fit, functional, parametric, and quality performance perspectives.

Cypress also recommends that customers take this opportunity to review these changes against current application notes, system design considerations and customer environment conditions to assess impact (if any) to their application.

Method of Identification:
Cypress maintains traceability of product to wafer level, including wafer fabrication location, through the lot number marked on the package.

Response Required:
This is an information only announcement. No response is required.

For additional information regarding this change, contact your local sales representative or contact the PCN Administrator at pcn_adm@cypress.com.

Sincerely,

Cypress PCN Administration

Item	Marketing Part Number	Description
1	CY62146ELL-45ZSXI	4-Mbit (256K × 16) Static RAM
2	CY62146ELL-45ZSXIT	4-Mbit (256K × 16) Static RAM
3	CY62146ESL-45ZSXI	4-Mbit (256K × 16) Static RAM
4	CY62146ESL-45ZSXIT	4-Mbit (256K × 16) Static RAM
5	CY62146EV30LL-45BVXI	4-Mbit (256K × 16) Static RAM
6	CY62146EV30LL-45BVXIT	4-Mbit (256K × 16) Static RAM
7	CY62146EV30LL-45ZSXI	4-Mbit (256K × 16) Static RAM
8	CY62146EV30LL-45ZSXIT	4-Mbit (256K × 16) Static RAM
9	CY621472E30LL-45ZSXI	4-Mbit (256K × 16) Static RAM
10	CY621472E30LL-45ZSXIT	4-Mbit (256K × 16) Static RAM
11	CY62147EV30LL-45B2XI	4-Mbit (256K × 16) Static RAM
12	CY62147EV30LL-45B2XIT	4-Mbit (256K × 16) Static RAM
13	CY62147EV30LL-45BVI	4-Mbit (256K × 16) Static RAM
14	CY62147EV30LL-45BVIT	4-Mbit (256K × 16) Static RAM
15	CY62147EV30LL-45BVXI	4-Mbit (256K × 16) Static RAM
16	CY62147EV30LL-45BVXIT	4-Mbit (256K × 16) Static RAM
17	CY62147EV30LL-45ZSXI	4-Mbit (256K × 16) Static RAM
18	CY62147EV30LL-45ZSXIT	4-Mbit (256K × 16) Static RAM
19	CY62148ELL-45ZSXI	4-Mbit (512K × 8) Static RAM
20	CY62148ELL-45ZSXIT	4-Mbit (512K × 8) Static RAM
21	CY62148ELL-55SXI	4-Mbit (512K × 8) Static RAM
22	CY62148ELL-55SXIT	4-Mbit (512K × 8) Static RAM
23	CY62148ESL-55ZAXI	4-Mbit (512K × 8) Static RAM
24	CY62148ESL-55ZAXIT	4-Mbit (512K × 8) Static RAM
25	CY62148EV30LL-45BVI	4-Mbit (512K × 8) Static RAM
26	CY62148EV30LL-45BVIT	4-Mbit (512K × 8) Static RAM
27	CY62148EV30LL-45BVXI	4-Mbit (512K × 8) Static RAM
28	CY62148EV30LL-45BVXIT	4-Mbit (512K × 8) Static RAM
29	CY62148EV30LL-45ZSXI	4-Mbit (512K × 8) Static RAM
30	CY62148EV30LL-45ZSXIT	4-Mbit (512K × 8) Static RAM
31	CY62148EV30LL-55SXI	4-Mbit (512K × 8) Static RAM
32	CY62148EV30LL-55SXIT	4-Mbit (512K × 8) Static RAM
33	CG7689AA	4-Mbit (256K × 16) Static RAM
34	CG7689AAT	4-Mbit (256K × 16) Static RAM
35	CG7690AA	4-Mbit (256K × 16) Static RAM
36	CG7690AAT	4-Mbit (256K × 16) Static RAM
37	CG7780AA	4-Mbit (256K × 16) Static RAM
38	CG7782AA	4-Mbit (256K × 16) Static RAM
39	CG7782AAT	4-Mbit (256K × 16) Static RAM
40	CG8187AA	4-Mbit (256K × 16) Static RAM
41	CG8187AAT	4-Mbit (256K × 16) Static RAM
42	CG8202AA	4-Mbit (256K × 16) Static RAM
43	CG8202AAT	4-Mbit (256K × 16) Static RAM
44	CG8830AM	4-Mbit (256K × 16) Static RAM
45	CG8830AMT	4-Mbit (256K × 16) Static RAM
46	CG8875AM	4-Mbit (512K × 8) Static RAM
47	CG8875AMT	4-Mbit (512K × 8) Static RAM
48	CG8887AM	4-Mbit (512K × 8) Static RAM
49	CG9079AA	4-Mbit (256K × 16) Static RAM
50	CG9079AAT	4-Mbit (256K × 16) Static RAM

DC Electrical Characteristics

				Current Spec			New Spec			Unit
Parameter	**Description**	**Test Condition**		**Minimum**	**Typical**	**Maximum**	**Minimum**	**Typical**	**Maximum**	
I_{cc}	V_{cc} operating supply current	$f = f_{max} = 1/t_{RC}$	$V_{CC} = V_{CC(max)}$	-	15	20	-	15	20	mA
		$f = 1$ MHz	$I_{OUT} = 0$ mA CMOS levels	-	2	2.5	-	3.5	6	mA
I_{SB1}	Automatic /CE power-down current – CMOS inputs	/CE ≥ V_{CC} – 0.2 V, $V_{IN} \geq V_{CC} - 0.2$ V, $V_{IN} \leq 0.2$ V, $f = f_{max}$ (address and data only), f = 0 (/OE, /BHE, /BLE and /WE), $V_{CC} = 3.60$ V		-	1	7	-	2.5	7	µA
I_{SB2}	Automatic /CE power-down current – CMOS inputs	/CE ≥ V_{CC} – 0.2 V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, f = 0, $V_{CC} = 3.60$ V		-	1	7	-	2.5	7	µA

Data Retention Specification

				Current Spec			New Spec			Unit
Parameter	**Description**	**Test Condition**		**Minimum**	**Typical**	**Maximum**	**Minimum**	**Typical**	**Maximum**	
I_{CCDR}	Data retention current	/CE ≥ V_{CC} – 0.2 V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	$V_{CC} = V_{DR}$	-	1	7	-	3	8.8	µA

Please note that Cypress is an Infineon Technologies Company.

The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

CY62147EV30 MoBL

4-Mbit (256K × 16) Static RAM

Features

- Very high speed: 45 ns
- Temperature ranges
  - Industrial: –40 °C to +85 °C
- Wide voltage range: 2.20 V to 3.60 V
- Pin compatible with CY62147DV30
- Ultra low standby power
  - Typical standby current: 2.5 µA
  - Maximum standby current: 7 µA (Industrial)
- Ultra low active power
  - Typical active current: 3.5 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}$ [1] and $\overline{OE}$ features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 48-ball very fine ball grid array (VFBGA) (single/dual CE option) and 44-pin thin small outline package (TSOP) II packages
- Byte power-down feature

Functional Description

The CY62147EV30 is a high performance CMOS static RAM (SRAM) organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra low active current. It is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99 percent when deselected ($\overline{CE}$ HIGH or both $\overline{BLE}$ and $\overline{BHE}$ are HIGH). The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when:

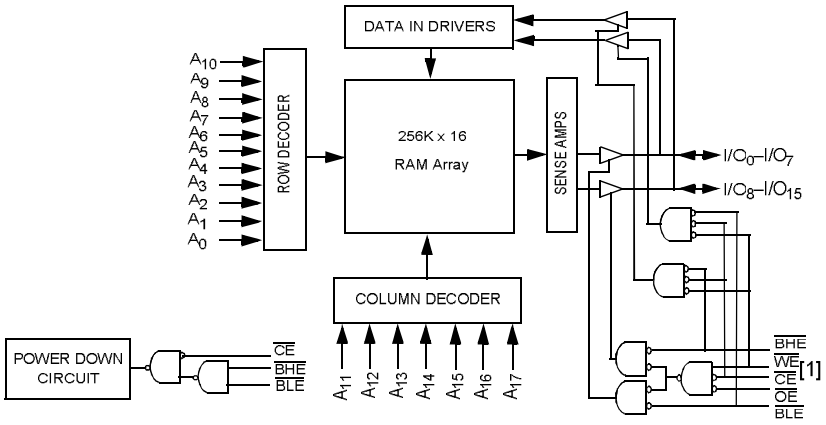
- Deselected ($\overline{CE}$ HIGH)
- Outputs are disabled ($\overline{OE}$ HIGH)
- Both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH)
- Write operation is active ($\overline{CE}$ LOW and $\overline{WE}$ LOW)

To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{17}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{17}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appear on I/O_0 to I/O_7. If Byte High enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See the Truth Table on page 11 for a complete description of read and write modes.

For a complete list of related documentation, click here.

Logic Block Diagram



Note

1. BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE_1}$ and CE_2 such that when $\overline{CE_1}$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH.

Contents

Product Portfolio

Product	Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
						f = 1 MHz		f = f_{max}			
		Min	Typ [2]	Max		Typ [2]	Max	Typ [2]	Max	Typ [2]	Max
CY62147EV30LL	Industrial	2.2	3.0	3.6	45	3.5	6	15	20	2.5	7

Pin Configurations

Figure 1. 48-ball VFBGA pinout (Single Chip Enable) [3, 4]

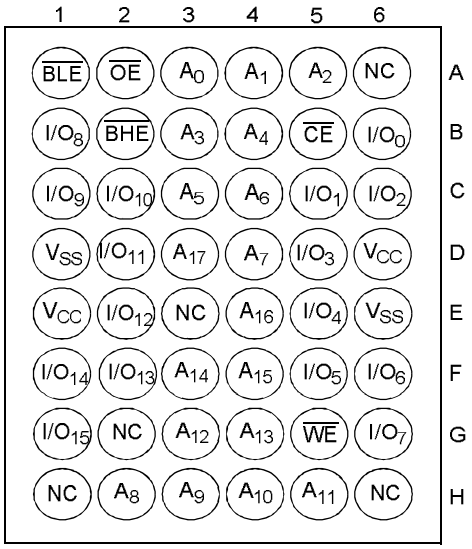


Figure 2. 48-ball VFBGA pinout (Dual Chip Enable) [3, 4]

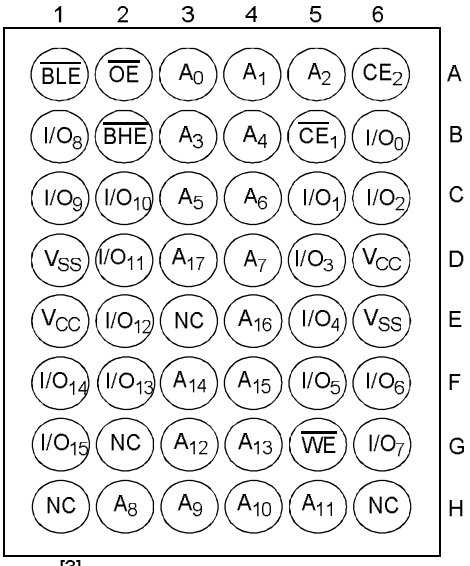
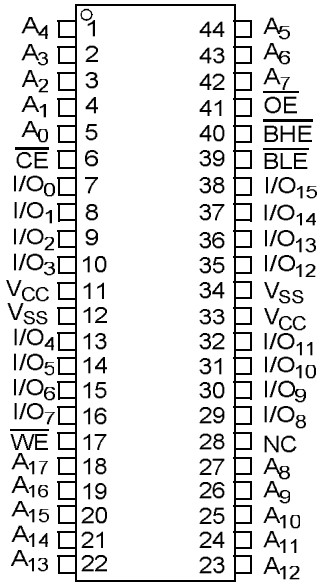


Figure 3. 44-pin TSOP II pinout [3]



Notes
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.
3. NC pins are not connected on the die.
4. Pins H1, G2, and H6 in the BGA package are address expansion pins for 8Mb, 16Mb, and 32Mb, respectively.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to + 150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential ..... –0.3 V to + 3.9 V ($V_{CC(max)}$ + 0.3 V)

DC voltage applied to outputs in High Z state [5, 6] ..... –0.3 V to 3.9 V ($V_{CC(max)}$ + 0.3 V)

DC input voltage [5, 6] ..... –0.3 V to 3.9 V ($V_{CC(max)}$ + 0.3 V)

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC} [7]
CY62147EV30LL	Industrial	–40 °C to +85 °C	2.2 V to 3.6 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		45 ns (Industrial)			Unit
				Min	Typ [8]	Max	
V_{OH}	Output HIGH voltage	I_{OH} = –0.1 mA		2.0	–	–	V
		I_{OH} = –1.0 mA, $V_{CC} \geq$ 2.70 V		2.4	–	–	V
V_{OL}	Output LOW voltage	I_{OL} = 0.1 mA		–	–	0.4	V
		I_{OL} = 2.1 mA, V_{CC} = 2.70 V		–	–	0.4	V
V_{IH}	Input HIGH voltage	V_{CC} = 2.2 V to 2.7 V		1.8	–	V_{CC} + 0.3	V
		V_{CC}= 2.7 V to 3.6 V		2.2	–	V_{CC} + 0.3	V
V_{IL}	Input LOW voltage	V_{CC} = 2.2 V to 2.7 V		–0.3	–	0.6	V
		V_{CC}= 2.7 V to 3.6 V		–0.3	–	0.8	V
I_{IX}	Input leakage current	GND $\leq V_I \leq V_{CC}$		–1	–	+1	µA
I_{OZ}	Output leakage current	GND $\leq V_O \leq V_{CC}$, output disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	f = f_{max} = $1/t_{RC}$	V_{CC} = $V_{CC(max)}$, I_{OUT} = 0 mA, CMOS levels	–	15	20	mA
		f = 1 MHz		–	3.5	6	
I_{SB1} [9]	Automatic $\overline{CE}$ power-down current – CMOS inputs	$\overline{CE} \geq V_{CC}$ – 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V, $V_{IN} \leq$ 0.2 V, f = f_{max} (address and data only), f = 0 ($\overline{OE}$, $\overline{BHE}$, $\overline{BLE}$ and $\overline{WE}$), V_{CC} = 3.60 V		–	2.5	7	µA
I_{SB2} [9]	Automatic $\overline{CE}$ power-down current – CMOS inputs	$\overline{CE} \geq V_{CC}$ – 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V or $V_{IN} \leq$ 0.2 V, f = 0, V_{CC} = 3.60 V		–	2.5	7	µA

Notes

5. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
6. $V_{IH(max)}$ = V_{CC} + 0.75 V for pulse durations less than 20 ns.
7. Full device AC operation assumes a minimum of 100 µs ramp time from 0 to $V_{CC(min)}$ and 200 µs wait time after V_{CC} stabilization.
8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
9. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

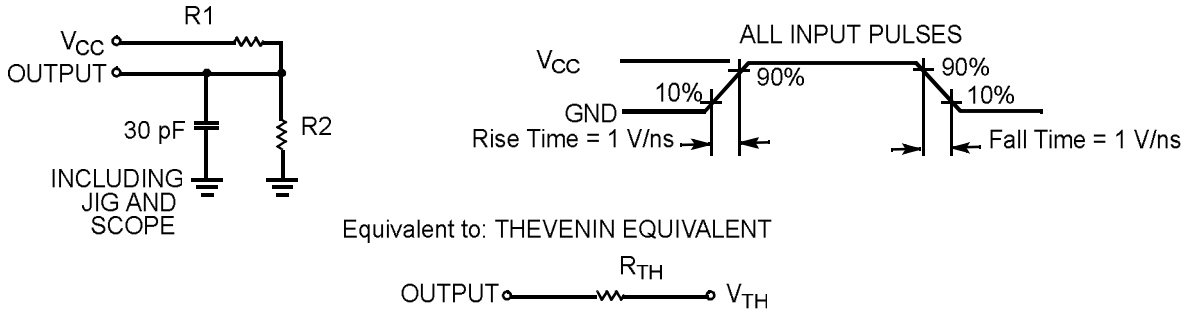
Parameter [10]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [10]	Description	Test Conditions	48-ball VFBGA Package	44-pin TSOP II Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	42.10	55.52	°C/W
Θ_{JC}	Thermal resistance (junction to case)		23.45	16.03	°C/W

AC Test Load and Waveforms

Figure 4. AC Test Load and Waveforms



Parameters	2.50 V	3.0 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Note
10. Tested initially and after any design or process changes that may affect these parameters.

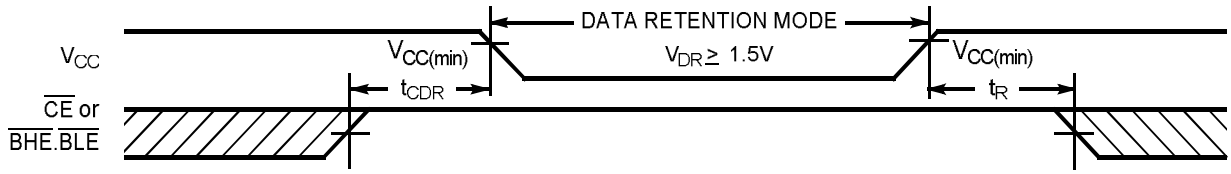
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ [11]	Max	Unit
V_{DR}	V_{CC} for data retention		1.5	–	–	V
I_{CCDR} [12]	Data retention current	V_{CC} = 1.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	3	8.8	µA
t_{CDR} [13]	Chip deselect to data retention time		0	–	–	ns
t_R [14]	Operation recovery time		45	–	–	ns

Data Retention Waveform

Figure 5. Data Retention Waveform [15, 16]



Notes

11. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
12. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
13. Tested initially and after any design or process changes that may affect these parameters.
14. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.
15. BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and $\overline{CE}_2$ such that when $\overline{CE}_1$ is LOW and $\overline{CE}_2$ is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH.
16. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

Switching Characteristics

Over the Operating Range

Parameter [17, 18]	Description	45 ns (Industrial)		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	45	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z [19]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z [19, 20]	–	18	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z [19]	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z [19, 20]	–	18	ns
t_{PU}	$\overline{CE}$ LOW to power-up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down	–	45	ns
t_{DBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to data valid	–	45	ns
t_{LZBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to low Z [19, 21]	5	–	ns
t_{HZBE}	$\overline{BLE}$/$\overline{BHE}$ HIGH to high Z [19, 20]	–	18	ns
Write Cycle [22, 23]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	ns
t_{BW}	$\overline{BLE}$/$\overline{BHE}$ LOW to write end	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z [19, 20]	–	18	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z [19]	10	–	ns

Notes

17. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1V/ns) or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the Figure 4 on page 5.
18. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Notes AN13842 and AN66311. However, the issue has been fixed and in production now, and hence, these Application Notes are no longer applicable. They are available for download on our website as they contain information on the date code of the parts, beyond which the fix has been in production.
19. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
20. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
21. If both byte enables are toggled together, this value is 10 ns.
22. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$, or both = V_{IL}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
23. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 6. Read Cycle No. 1 (Address Transition Controlled) [24, 25]

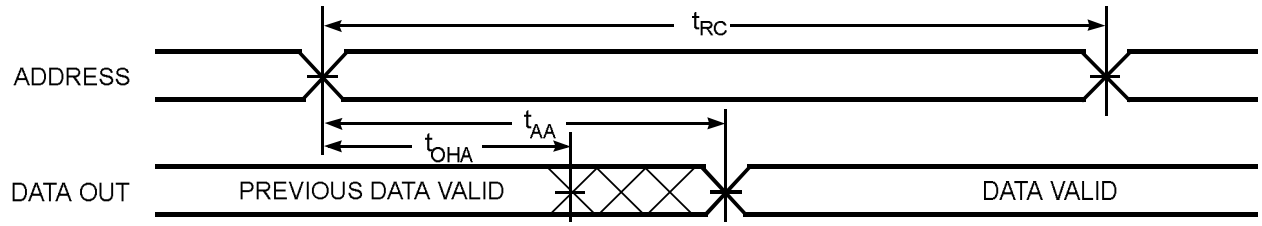
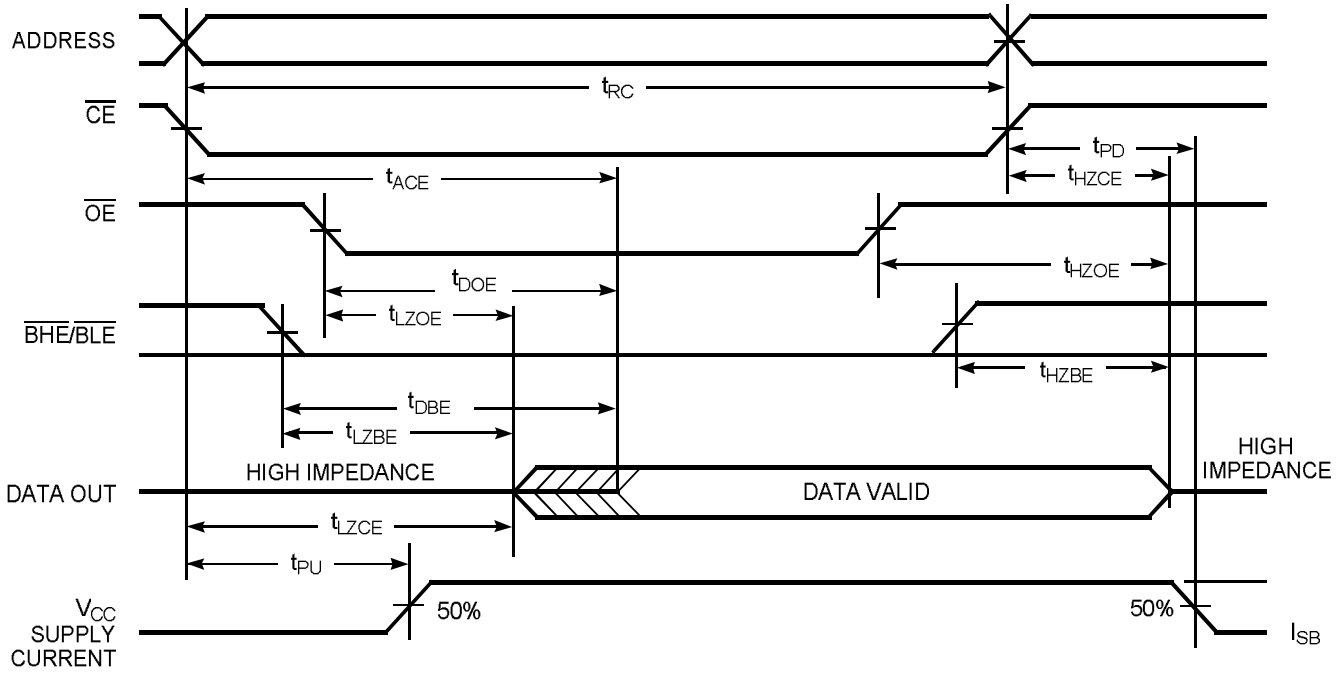


Figure 7. Read Cycle No. 2 ($\overline{OE}$ Controlled) [25, 26, 27]



Notes
24. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$, or both = V_{IL}.
25. $\overline{WE}$ is HIGH for read cycle.
26. BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE_1}$ and CE_2 such that when $\overline{CE_1}$ is LOW and CE_2 is HIGH, CE is LOW. For all other cases CE is HIGH.
27. Address valid before or similar to $\overline{CE}$ and $\overline{BHE}$, $\overline{BLE}$ transition LOW.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 1 ($\overline{WE}$ Controlled) [28, 29, 30, 31]

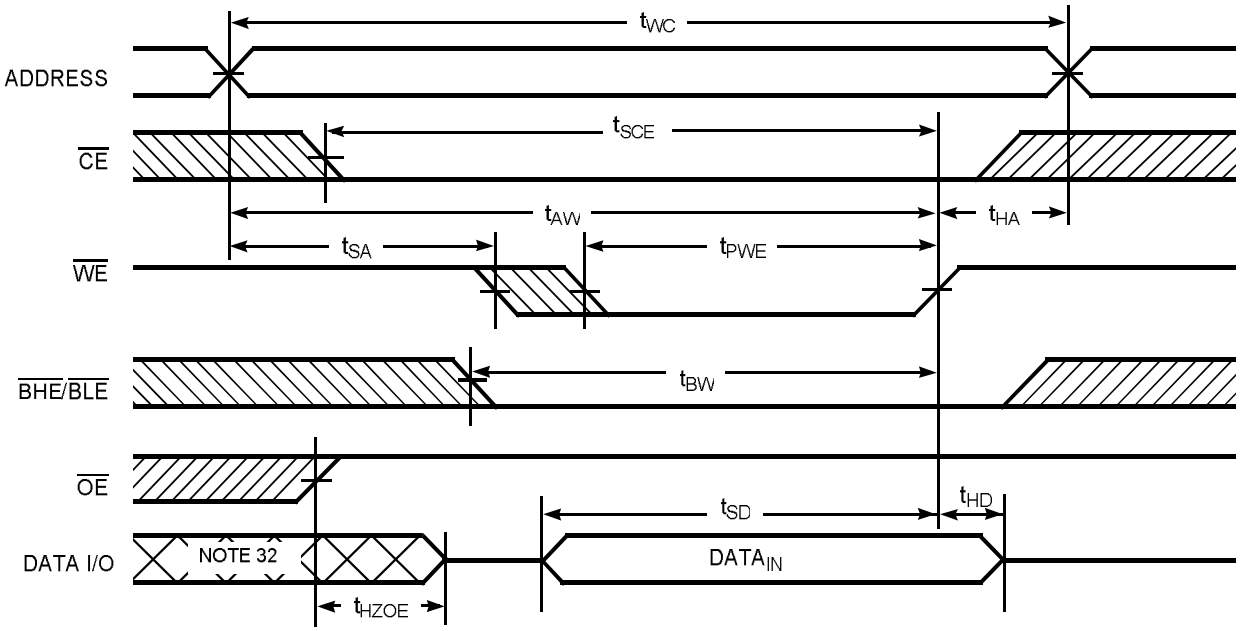
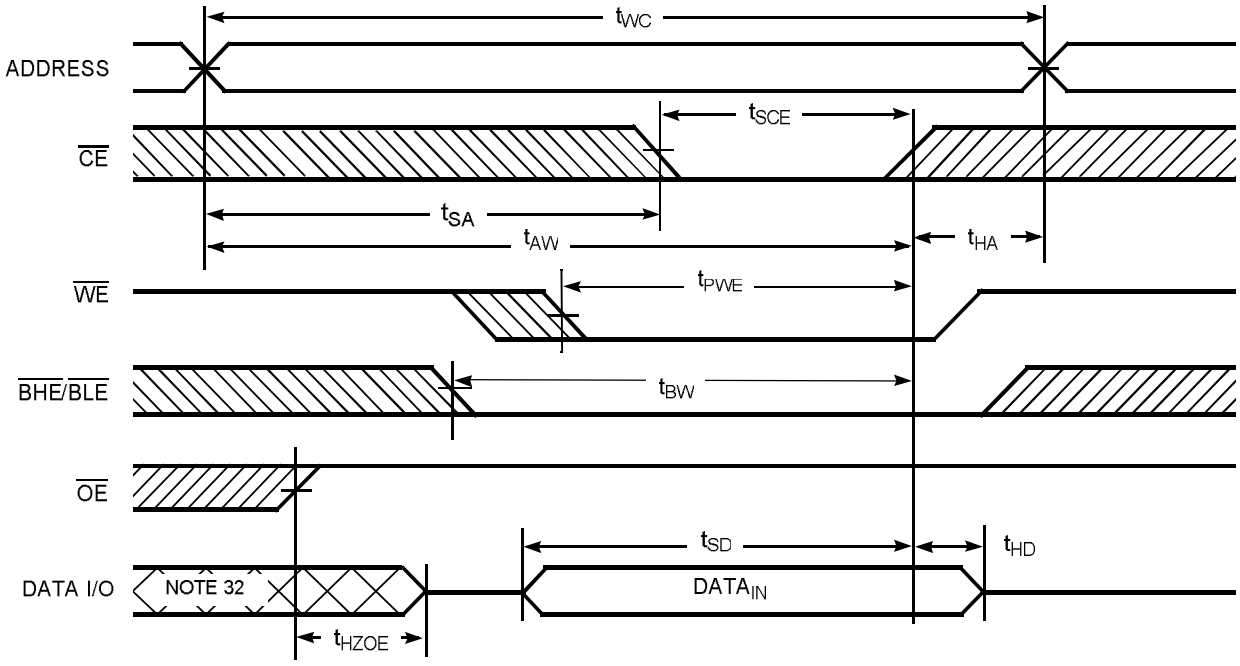


Figure 9. Write Cycle No. 2 ($\overline{CE}$ Controlled) [28, 29, 30, 31]



Notes

28. BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE_1}$ and CE_2 such that when $\overline{CE_1}$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH.
29. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$, or both = V_{IL}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
30. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
31. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
32. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 10. Write Cycle No. 3 (WE Controlled, OE LOW) [33, 34, 35]

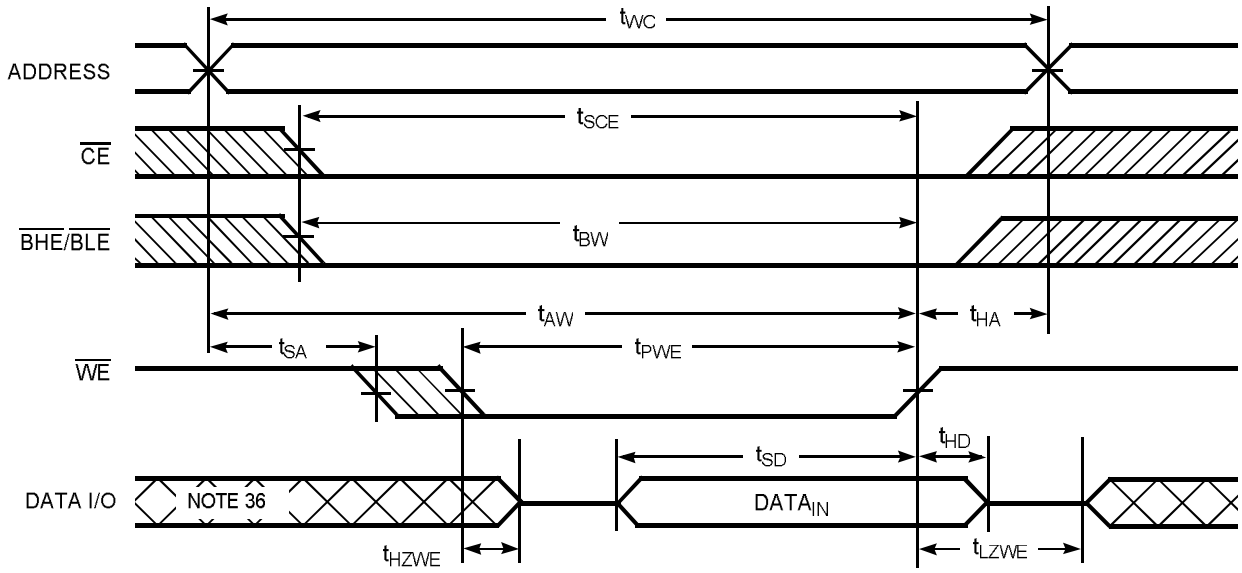
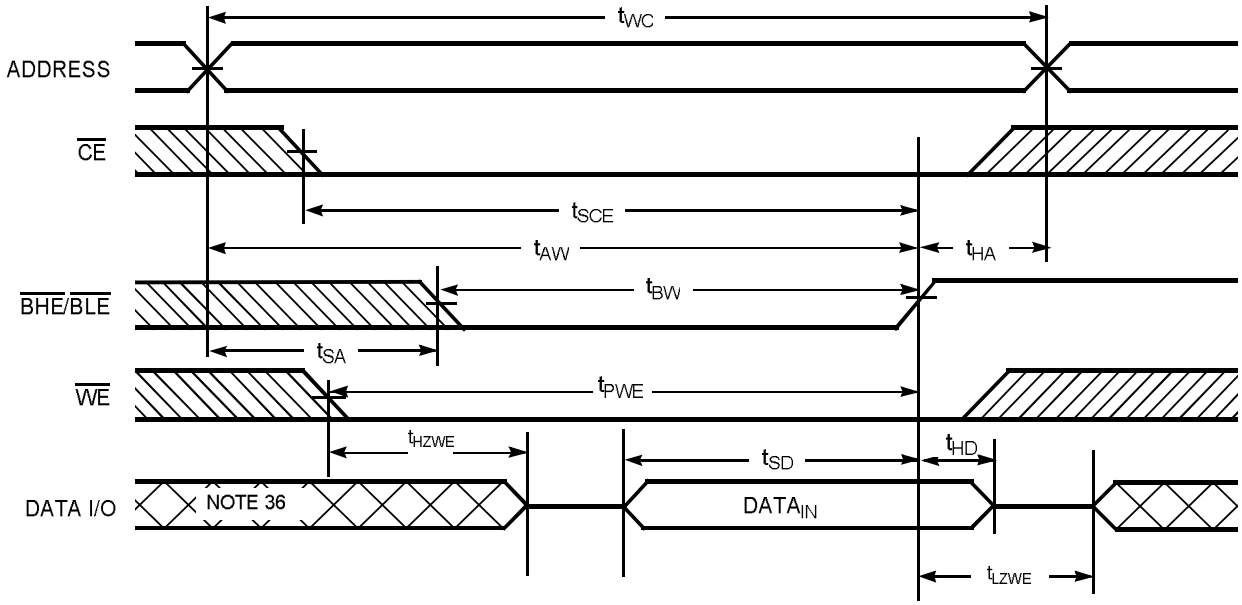


Figure 11. Write Cycle No. 4 (BHE/BLE Controlled) [33, 34]



Notes

33. BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH.
34. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
35. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE}.
36. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{CE}$ [37, 38]	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	I/Os	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
L	X	X	H	H	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	L	L	L	Data out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data out (I/O_0–I/O_7); I/O_8–I/O_{15} in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Output disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output disabled	Active (I_{CC})
L	L	X	L	L	Data in (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data in (I/O_0–I/O_7); I/O_8–I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data in (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Write	Active (I_{CC})

Notes

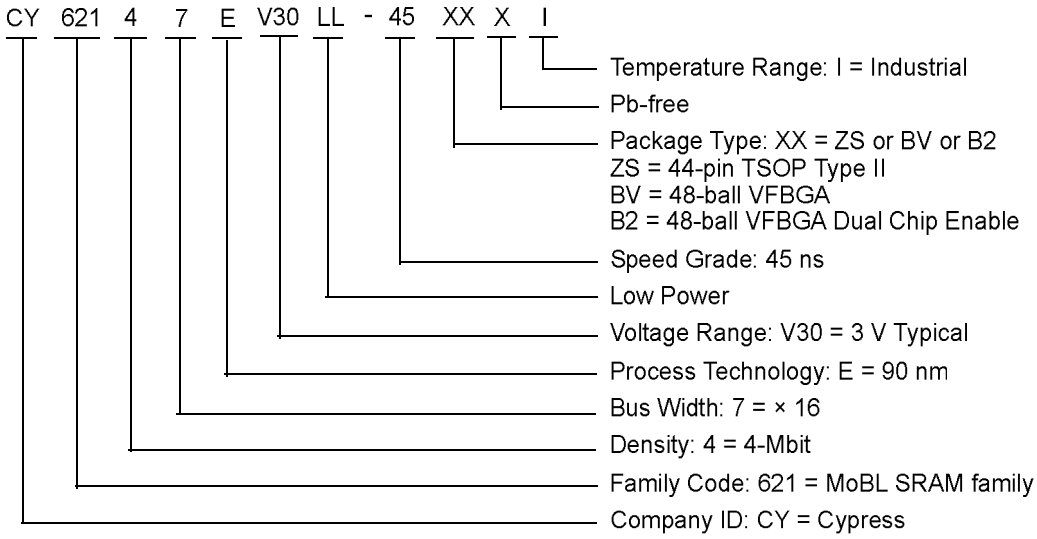
37. BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH.
38. For the Dual Chip Enable device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH. Intermediate voltage levels are not permitted on any of the Chip Enable pins ($\overline{CE}$ for the Single Chip Enable device; $\overline{CE}_1$ and CE_2 for the Dual Chip Enable device).

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62147EV30LL-45BVI	51-85150	48-ball VFBGA [39]	Industrial
	CY62147EV30LL-45BVXI	51-85150	48-ball VFBGA (Pb-free) [39]	
	CY62147EV30LL-45B2XI	51-85150	48-ball VFBGA (Pb-free) [40]	
	CY62147EV30LL-45ZSXI	51-85087	44-pin TSOP Type II (Pb-free)	

Contact your local Cypress sales representative for availability of these parts.

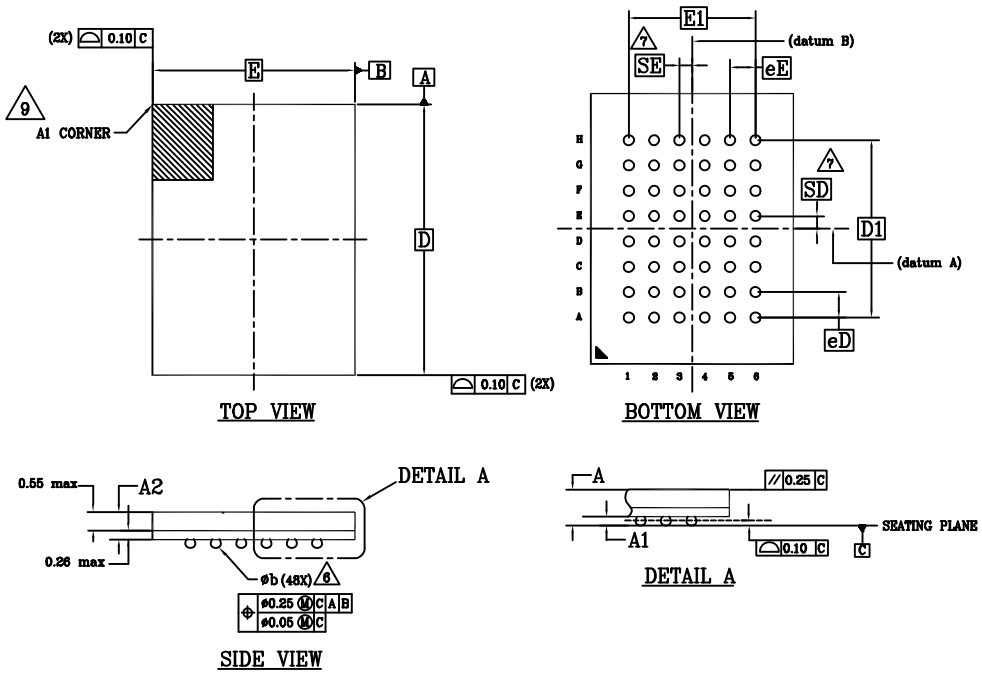
Ordering Code Definitions



Notes
39. This BGA package is offered with single chip enable.
40. This BGA package is offered with dual chip enable.

Package Diagrams

Figure 12. 48-ball VFBGA (6.0 × 8.0 × 1.0 mm) Package Outline, 51-85150



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.16	-	-
A2	-	-	0.81
D	8.00 BSC		
E	6.00 BSC		
D1	5.25 BSC		
E1	3.75 BSC		
MD	8		
ME	6		
n	48		
Ø b	0.25	0.30	0.35
eE	0.75 BSC		
eD	0.75 BSC		
SD	0.375 BSC		
SE	0.375 BSC		

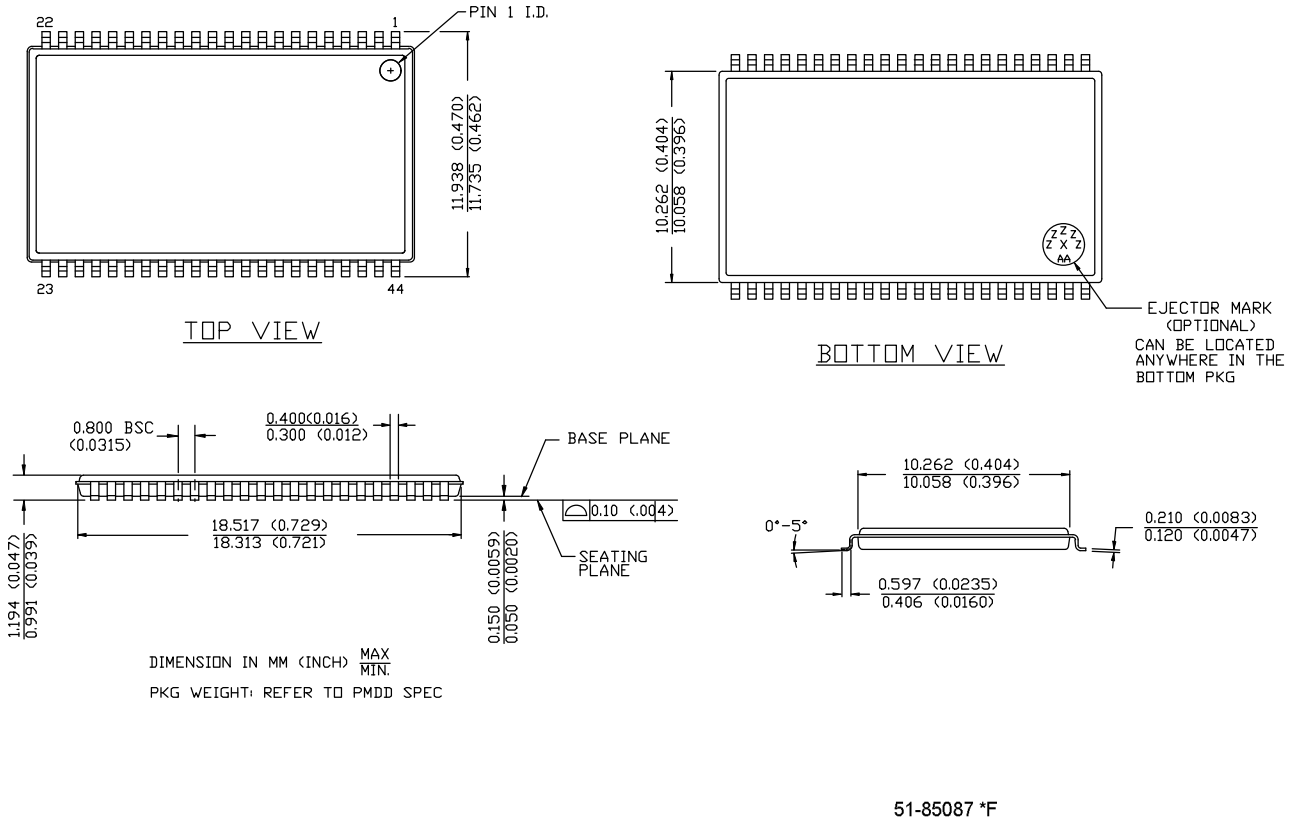
NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.

51-85150 *I

Package Diagrams (continued)

Figure 13. 44-pin TSOP II (18.4 × 10.2 × 1.194 mm) Package Outline, 51-85087



51-85087 *F

Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62147EV30 MoBL, 4-Mbit (256K × 16) Static RAM Document Number: 38-05440			
Revision	**ECN**	**Submission Date**	**Description of Change**
**	201861	01/13/2004	New data sheet.
*A	247009	07/27/2004	Changed status from Advanced Information to Preliminary. Updated Operating Range: Updated Note 7 (Replaced 100 µs with 200 µs). Updated Data Retention Characteristics: Changed maximum value of I_{CCDR} parameter from 2.0 µA to 2.5 µA. Changed minimum value of t_R parameter from 100 µs to t_{RC} ns. Updated Switching Characteristics: Changed minimum value of t_{OHA} parameter from 6 ns to 10 ns corresponding to both 35 ns and 45 ns speed bins. Changed maximum value of t_{DOE} parameter from 15 ns to 18 ns corresponding to 35 ns speed bin. Changed maximum value of t_{HZOE}, t_{HZBE}, t_{HZWE} parameters from 12 ns to 15 ns corresponding to 35 ns speed bin and from 15 ns to 18 ns corresponding to 45 ns speed bin. Changed minimum value of t_{SCE}, t_{BW} parameters from 25 ns to 30 ns corresponding to 35 ns speed bin and from 40 ns to 35 ns corresponding to 45 ns speed bin. Changed maximum value of t_{HZCE} parameter from 12 ns to 18 ns corresponding to 35 ns speed bin and from 15 ns to 22 ns corresponding to 45 ns speed bin. Changed minimum value of t_{SD} parameter from 15 ns to 18 ns corresponding to 35 ns speed bin and from 20 ns to 22 ns corresponding to 45 ns speed bin. Removed Note "If both Byte Enables ($\overline{BHE}$ and $\overline{BLE}$) are toggled together then this value is 6 ns min. Otherwise this value is 3 ns min." and its reference in t_{LZBE} parameter. Updated Ordering Information: Updated part numbers.
*B	414807	12/16/2005	Changed status from Preliminary to Final. Removed 35 ns speed bin related information in all instances across the document. Removed "L" version (of CY62147EV30) related information in all instances across the document. Updated Product Portfolio: Changed typical value of "Operating I_{CC}" from 1.5 mA to 2 mA corresponding to "f = 1 MHz". Changed maximum value of "Operating I_{CC}" from 2 mA to 2.5 mA corresponding to "f = 1 MHz". Changed typical value of "Operating I_{CC}" from 12 mA to 15 mA corresponding to "f = f_{max}". Updated Pin Configurations: Updated figure "48-ball VFBGA pinout" (Replaced DNU with NC in ball E3). Removed Note "DNU pins have to be left floating or tied to V_{SS} to ensure proper application." and its reference. Updated Electrical Characteristics: Changed typical value of I_{CC} parameter from 12 mA to 15 mA corresponding to Test Condition "f = f_{max}". Changed typical value of I_{CC} parameter from 1.5 mA to 2 mA corresponding to Test Condition "f = 1 MHz". Changed maximum value of I_{CC} parameter from 2 mA to 2.5 mA corresponding to Test Condition "f = 1 MHz". Changed typical value of I_{SB1}, I_{SB2} parameters from 0.7 µA to 1 µA. Changed maximum value of I_{SB1}, I_{SB2} parameters from 2.5 µA to 7 µA. Updated AC Test Load and Waveforms: Changed AC Test Load Capacitance from 50 pF to 30 pF. Updated Data Retention Characteristics: Added typical value of I_{CCDR} parameter. Changed maximum value of I_{CCDR} parameter from 2.5 µA to 7 µA.

Document History Page (continued)

Document Title: CY62147EV30 MoBL, 4-Mbit (256K × 16) Static RAM Document Number: 38-05440			
Revision	**ECN**	**Submission Date**	**Description of Change**
*B (cont.)	414807	12/16/2005	Updated Switching Characteristics: Changed minimum value of t_{LZOE} parameter from 3 ns to 5 ns. Changed minimum value of t_{LZCE}, t_{LZBE}, t_{LZWE} parameters from 6 ns to 10 ns. Changed maximum value of t_{HZCE} parameter from 22 ns to 18 ns. Changed minimum value of t_{PWE} parameter from 30 ns to 35 ns. Changed minimum value of t_{SD} parameter from 22 ns to 25 ns. Updated Ordering Information: Updated part numbers. Removed “Package Name” column. Added “Package Diagram” column. Updated Package Diagrams: spec 51-85150 – Changed revision from *B to *D. Updated to new template.
*C	464503	05/25/2006	Added Automotive-E Temperature Range related information in all instances across the document and assigned Preliminary status (shaded the area) in required places. Added 55 ns speed bin related information in all instances across the document. Updated Ordering Information: Updated part numbers.
*D	925501	04/09/2007	Added Automotive-A Temperature Range related information in all instances across the document and assigned Preliminary status (shaded the area) in required places. Updated Electrical Characteristics: Added Note 9 and referred the same note in I_{SB2} parameter. Updated Data Retention Characteristics: Added Note 12 and referred the same note in I_{CCDR} parameter. Updated Switching Characteristics: Added Note 18 and referred the same note in “Parameter” column.
*E	1045701	05/07/2007	Changed status of Automotive-A and Automotive-E Temperature Range related information from Preliminary to Final (unshaded the area).
*F	2577505	10/03/2008	Updated Ordering Information: Updated part numbers. Updated to new template.
*G	2681901	04/01/2009	Updated Ordering Information: Updated part numbers.
*H	2886488	03/02/2010	Updated Truth Table: Added Note 38 and referred the same note in “$\overline{CE}$” column. Updated Package Diagrams: spec 51-85150 – Changed revision from *D to *E. spec 51-85087 – Changed revision from *A to *C. Updated to new template.
*I	3109050	12/13/2010	Changed Table Footnotes to Notes in all instances across the document. Updated Ordering Information: No change in part numbers. Added Ordering Code Definitions. Updated Package Diagrams: spec 51-85150 – Changed revision from *E to *F.
*J	3123973	01/31/2011	Removed Automotive-A and Automotive-E Temperature Range related information in all instances across the document. Updated Ordering Information: Updated part numbers. Added Acronyms and Units of Measure.

Document History Page (continued)

Document Title: CY62147EV30 MoBL, 4-Mbit (256K × 16) Static RAM Document Number: 38-05440			
Revision	**ECN**	**Submission Date**	**Description of Change**
*K	3296744	08/09/2011	Updated Functional Description: Updated description. Updated Electrical Characteristics: Updated Note 9. Referred Note 9 in I_{SB1} parameter. Updated Data Retention Characteristics: Updated Note 12. Updated Switching Characteristics: Added Note 21 and referred the same note in the description of t_{LZBE} parameter. Completing Sunset Review.
*L	3456837	12/06/2011	Updated Package Diagrams: spec 51-85150 – Changed revision from *F to *G. spec 51-85087 – Changed revision from *C to *D. Updated to new template.
*M	3724736	08/23/2012	Fixed typo errors. Minor clean-up. Completing Sunset Review.
*N	4102445	08/22/2013	Updated Switching Characteristics: Updated Note 18. Updated Package Diagrams: spec 51-85150 – Changed revision from *G to *H. spec 51-85087 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.
*O	4576526	11/21/2014	Updated Functional Description: Added "For a complete list of related documentation, click here." at the end. Updated Switching Characteristics: Added Note 23 and referred the same note in "Write Cycle". Updated Switching Waveforms: Added Note 35 and referred the same note in Figure 10.
*P	4918858	09/14/2015	Updated Switching Waveforms: Updated Figure 11 (Updated caption only (Removed "$\overline{OE}$ LOW")). Updated to new template. Completing Sunset Review.
*Q	5445135	09/22/2016	Updated Thermal Resistance: Updated values of Θ_{JA} and Θ_{JC} parameters corresponding to all packages. Updated to new template. Completing Sunset Review.
*R	5984537	12/05/2017	Updated Cypress Logo and Copyright.
*S	6548255	04/17/2019	Updated Package Diagrams: spec 51-85150 – Changed revision from *H to *I. Updated to new template.
*T	6899706	06/26/2020	Updated Features: Changed value of "Typical standby current" from 1 µA to 2.5 µA. Changed value of "Typical active current" from 2 mA to 3.5 mA. Updated Product Portfolio: Changed typical value of "Operating I_{CC}" from 2 mA to 3.5 mA corresponding to "f = 1 MHz". Changed maximum value of "Operating I_{CC}" from 2.5 mA to 6 mA corresponding to "f = 1 MHz". Changed typical value of "Standby I_{SB2}" from 1 µA to 2.5 µA.

Document History Page (continued)

Document Title: CY62147EV30 MoBL, 4-Mbit (256K × 16) Static RAM Document Number: 38-05440			
Revision	**ECN**	**Submission Date**	**Description of Change**
*T (cont.)	6899706	06/26/2020	Updated Electrical Characteristics: Changed typical value of I_{CC} parameter from 2 mA to 3.5 mA corresponding to Test Condition "f = 1 MHz". Changed maximum value of I_{CC} parameter from 2.5 mA to 6 mA corresponding to Test Condition "f = 1 MHz". Changed typical value of I_{SB1} parameter from 1 µA to 2.5 µA. Changed typical value of I_{SB2} parameter from 1 µA to 2.5 µA. Updated Data Retention Characteristics: Changed typical value of I_{CCDR} parameter from 0.8 µA to 3 µA. Changed maximum value of I_{CCDR} parameter from 7 µA to 8.8 µA. Updated Package Diagrams: spec 51-85087 – Changed revision from *E to *F. Updated to new template.

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Continuity of ordering part numbers

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CY62146E MoBL

4-Mbit (256K × 16) Static RAM

Features

- Very high speed: 45 ns
- Wide voltage range: 4.5 V to 5.5 V
- Ultra low standby power
  - Typical standby current: 2.5 µA
  - Maximum standby current: 7 µA
- Ultra low active power
  - Typical active current: 3.5 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 44-pin thin small outline package (TSOP) Type II package

Functional Description

The CY62146E is a high performance CMOS static RAM organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra low active current. It is ideal for providing More Battery Life™ (MoBL®) in portable applications. The device also has an automatic power down feature that reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected ($\overline{CE}$ HIGH). The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH) or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

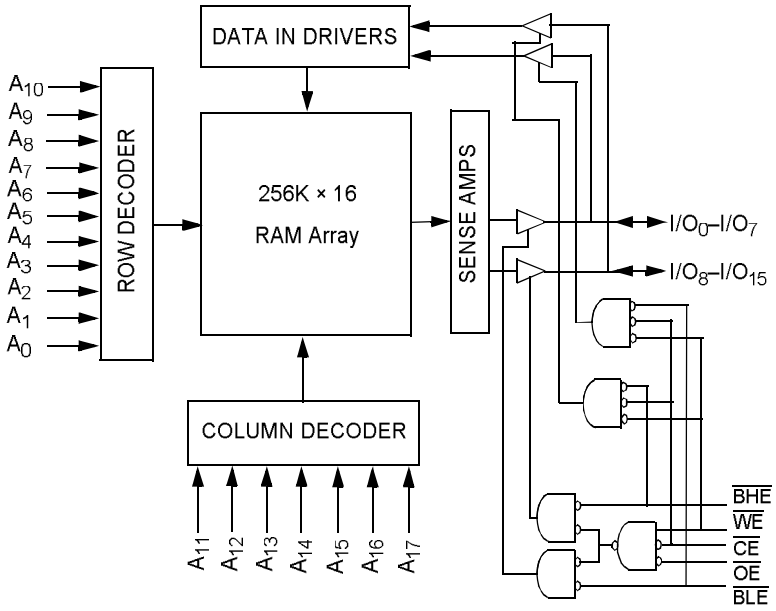
To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{17}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{17}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appears on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See Truth Table on page 11 for a complete description of read and write modes.

The CY62146E device is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please Electrical Characteristics on page 4 for more details and suggested alternatives.

For a complete list of related documentation, click here.

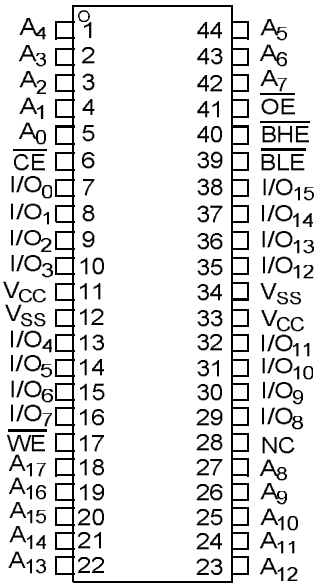
Logic Block Diagram



Contents

Pin Configurations

Figure 1. 44-pin TSOP II pinout (Top View) [1]



Product Portfolio

Product	Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I_{CC}, (mA)				Standby, I_{SB2} (µA)	
						f = 1 MHz		f = f_{max}			
		Min	Typ [2]	Max		Typ [2]	Max	Typ [2]	Max	Typ [2]	Max
CY62146ELL	Industrial/ Automotive-A	4.5	5.0	5.5	45	3.5	6	15	20	2.5	7

Notes
1. NC pins are not connected on the die.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential .....–0.5 V to 6.0 V

DC voltage applied to outputs in high Z state [3, 4] .....–0.5 V to 6.0 V

DC input voltage [3, 4] .....–0.5 V to 6.0 V

Output current into outputs (LOW) .....20 mA

Static discharge voltage (MIL-STD-883, Method 3015) ..... >2001 V

Latch-up current ..... >200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[5]
CY62146ELL	Industrial/ Automotive-A	–40 °C to +85 °C	4.5 V–5.5 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		45 ns (Industrial/Automotive-A)			Unit
				Min	Typ[6]	Max	
V_{OH}	Output high voltage	V_{CC} = 4.5 V	I_{OH} = –1.0 mA	2.4	–	–	V
		V_{CC} = 5.5 V	I_{OH} = –0.1 mA	–	–	3.4 [7]	
V_{OL}	Output low voltage	I_{OL} = 2.1 mA		–	–	0.4	V
V_{IH}	Input high voltage	4.5 ≤ V_{CC} ≤ 5.5		2.2	–	V_{CC} + 0.5	V
V_{IL}	Input low voltage	4.5 ≤ V_{CC} ≤ 5.5		–0.5	–	0.8	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–1	–	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, output disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	f = f_{max} = 1/t_{RC}	V_{CC} = V_{CCmax}	–	15	20	mA
		f = 1 MHz	I_{OUT} = 0 mA, CMOS levels	–	3.5	6	
I_{SB2} [8]	Automatic CE power down current – CMOS inputs	$\overline{CE}$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0, V_{CC} = $V_{CC(max)}$		–	2.5	7	µA

Notes

3. V_{IL}(min) = –2.0 V for pulse durations less than 20 ns for I < 30 mA.
4. V_{IH}(max) = V_{CC} + 0.75 V for pulse durations less than 20 ns.
5. Full Device AC operation assumes a minimum of 100 µs ramp time from 0 to V_{CC} (min) and 200 µs wait time after V_{CC} stabilization.
6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
7. Please note that the maximum V_{OH} limit does not exceed minimum CMOS V_{IH} of 3.5 V. If you are interfacing this SRAM with 5 V legacy processors that require a minimum V_{IH} of 3.5 V, please refer to Application Note AN6081 for technical details and options you may consider.
8. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB2}/I_{CCDR} spec. Other inputs are left floating.

Capacitance

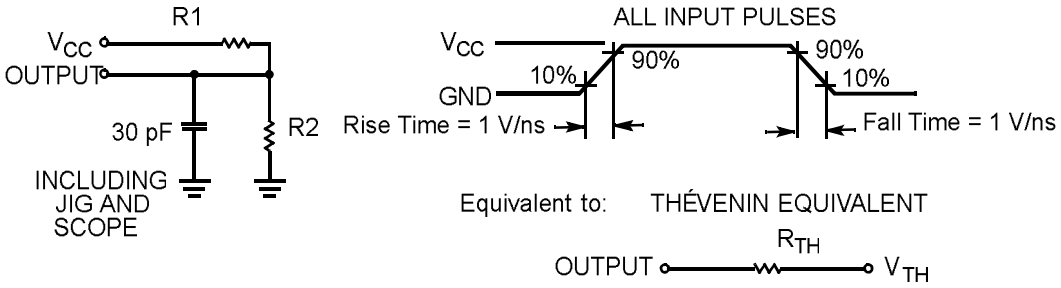
Parameter [9]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [9]	Description	Test Conditions	44-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	55.52	°C/W
Θ_{JC}	Thermal resistance (junction to case)		16.03	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameters	5.0 V	Unit
R1	1800	Ω
R2	990	Ω
R_{TH}	639	Ω
V_{TH}	1.77	V

Note
9. Tested initially after any design or process changes that may affect these parameters.

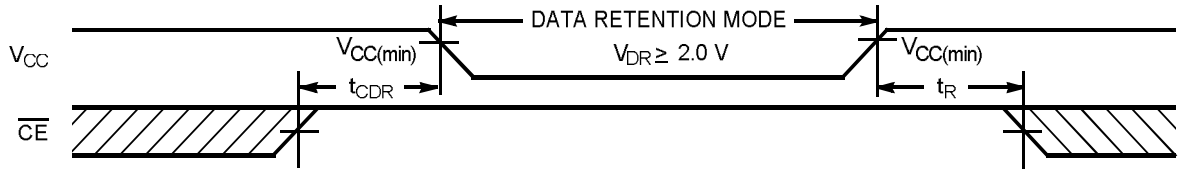
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ [10]	Max	Unit
V_{DR}	V_{CC} for data retention		2	–	–	V
I_{CCDR} [11]	Data retention current	V_{CC} = 2 V, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	3	8.8	µA
t_{CDR} [12]	Chip deselect to data retention time		0	–	–	ns
t_R [13]	Operation recovery time		45	–	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes

10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
11. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB2}/I_{CCDR} spec. Other inputs are left floating.
12. Tested initially and after any design or process changes that may affect these parameters.
13. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.

Switching Characteristics

Over the Operating Range

Parameter [14, 15]	Description	45 ns (Industrial/Automotive-A)		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	45	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[16]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[16, 17]	–	18	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[16]	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[16, 17]	–	18	ns
t_{PU}	$\overline{CE}$ LOW to power-up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down	–	45	ns
t_{DBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to data valid	–	22	ns
t_{LZBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to Low Z[16]	5	–	ns
t_{HZBE}	$\overline{BLE}$/$\overline{BHE}$ HIGH to High Z[16, 17]	–	18	ns
Write Cycle[18, 19]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	ns
t_{BW}	$\overline{BLE}$/$\overline{BHE}$ LOW to write end	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [16, 17]	–	18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [16]	10	–	ns

Notes

14. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1 V/ns) or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3 V, and output loading of the specified I_{OL}/I_{OH} as shown in Figure 2 on page 5.
15. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Notes AN13842 and AN66311. However, the issue has been fixed and in production now, and hence, these Application Notes are no longer applicable. They are available for download on our website as they contain information on the date code of the parts, beyond which the fix has been in production.
16. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
17. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
18. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
19. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [20, 21]

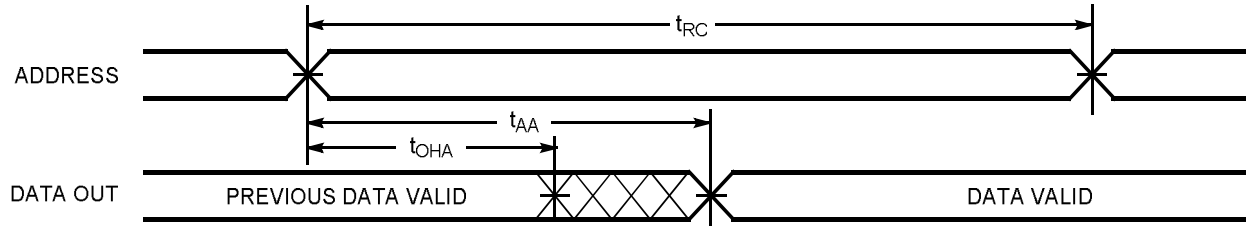
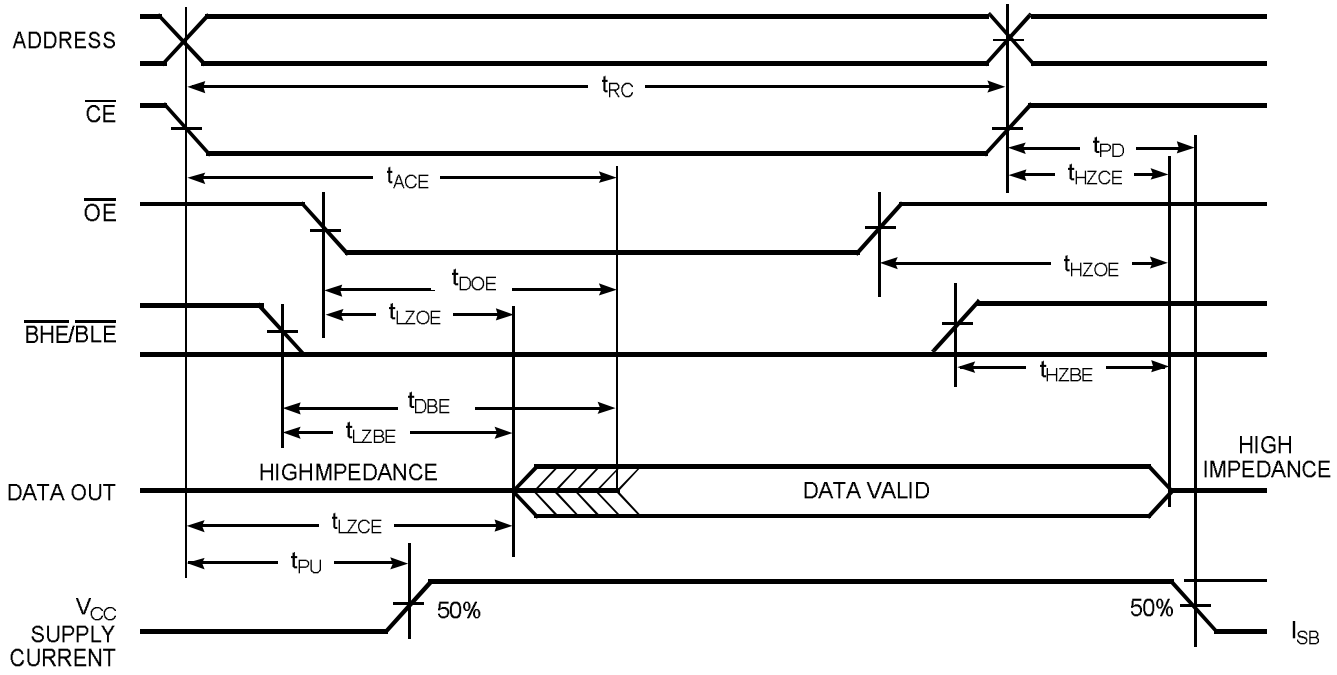


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [21, 22]



Notes
20. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$, or both = V_{IL}.
21. $\overline{WE}$ is HIGH for read cycle.
22. Address valid before or similar to $\overline{CE}$, $\overline{BHE}$, $\overline{BLE}$ transition LOW.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ($\overline{WE}$ Controlled) [23, 24, 25]

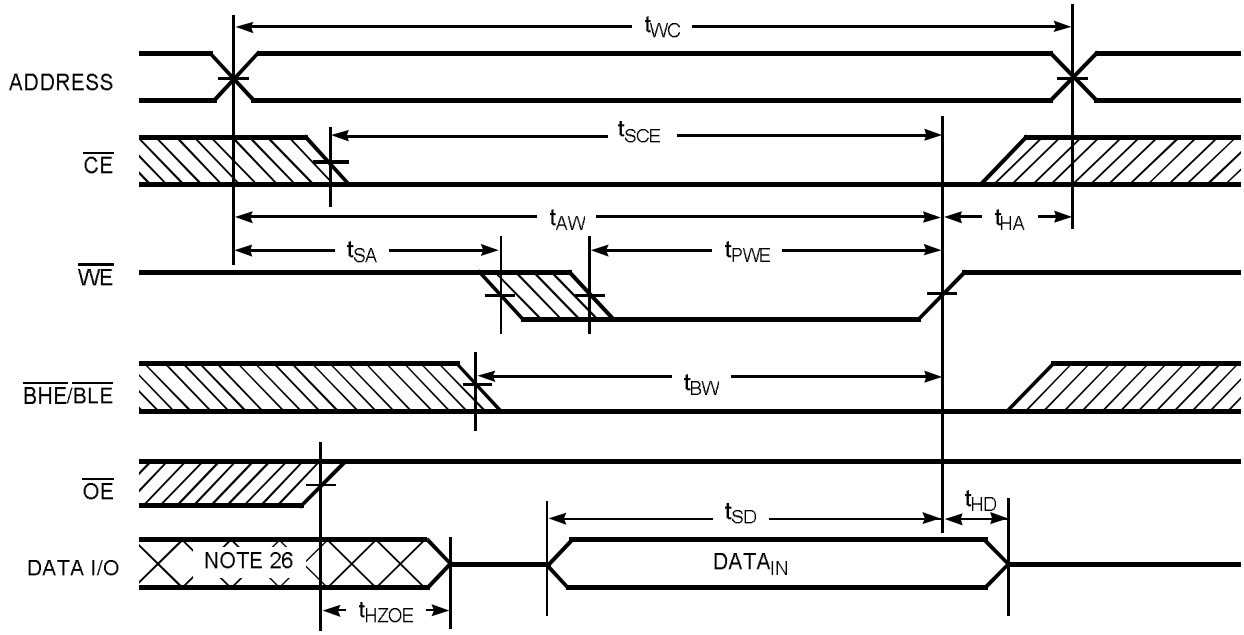
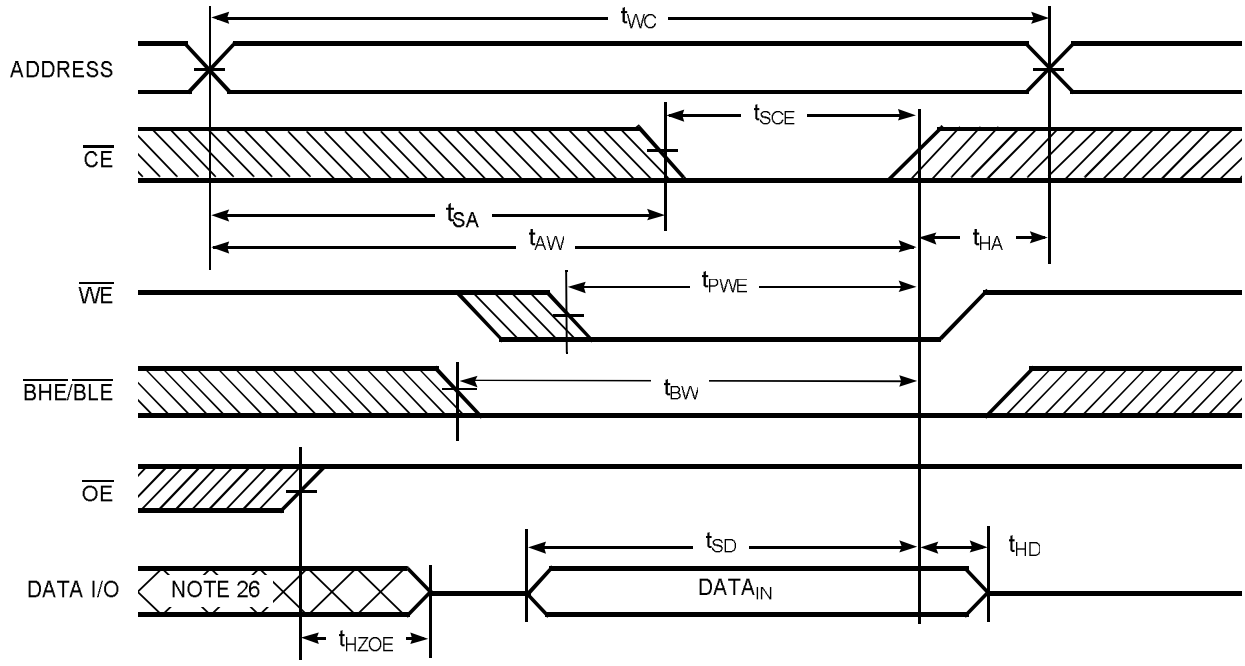


Figure 7. Write Cycle No. 2 ($\overline{CE}$ Controlled) [23, 24, 25]



Notes

23. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
24. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
25. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}. All signals must be active to initiate a write and any of these signals can terminate the write by going inactive. The input setup and hold timing must be referenced to the edge of the signal that terminate the write.
26. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 (WE Controlled, OE LOW) [27, 28, 30]

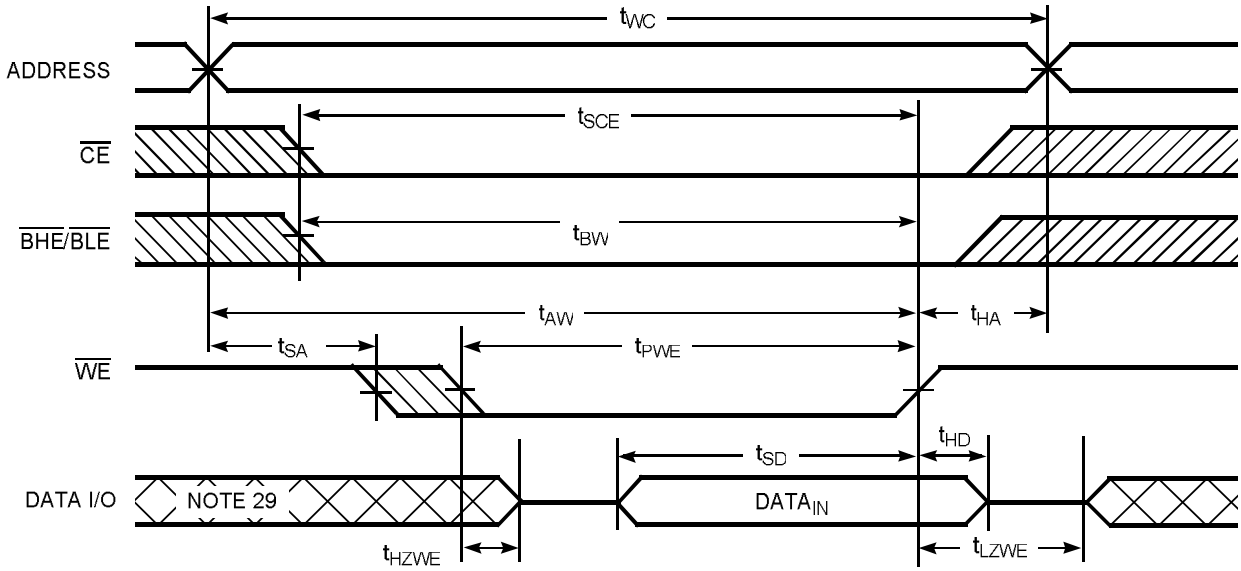
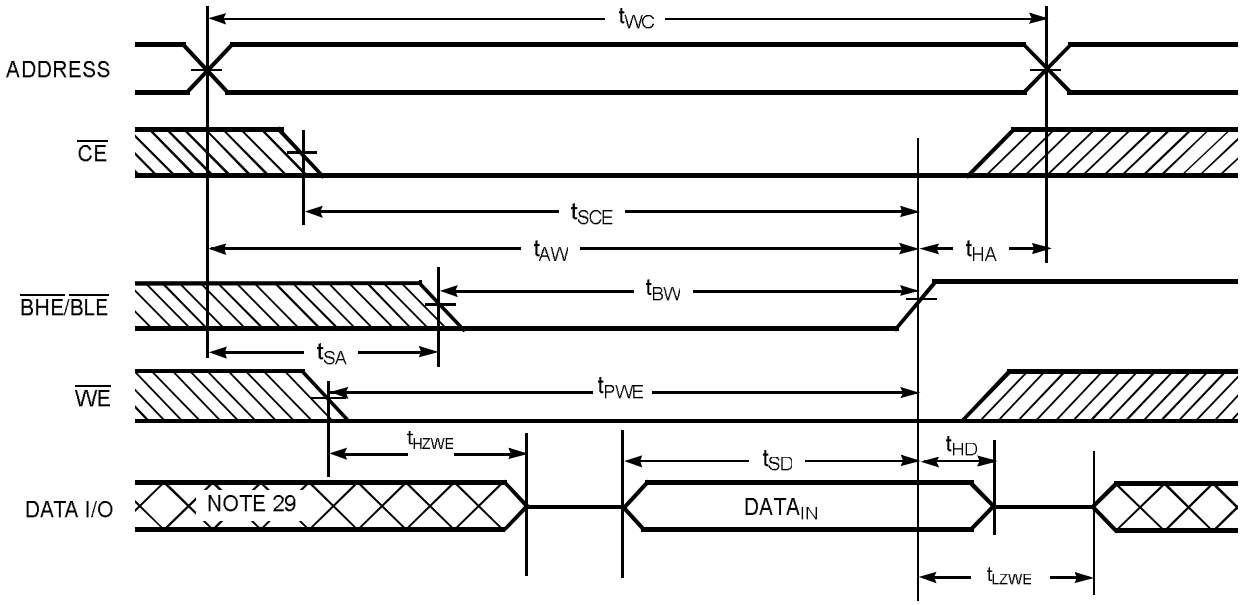


Figure 9. Write Cycle No. 4 (BHE/BLE Controlled, OE LOW) [27, 28]



Notes

27. If CE goes HIGH simultaneously with WE = V_{IH}, the output remains in a high impedance state.
28. The internal write time of the memory is defined by the overlap of WE, CE = V_{IL}, BHE, BLE or both = V_{IL}. All signals must be active to initiate a write and any of these signals can terminate the write by going inactive. The input setup and hold timing must be referenced to the edge of the signal that terminate the write.
29. During this period, the I/Os are in output state. Do not apply input signals.
30. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE}.

Truth Table

$\overline{CE}$[31]	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X[31]	X[31]	High Z	Deselect/power down	Standby (I_{SB})
L	X	X	H	H	High Z	Output disabled	Active (I_{CC})
L	H	L	L	L	Data out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data out (I/O_0–I/O_7); I/O_8–I/O_{15} in High-Z	Read	Active (I_{CC})
L	H	L	L	H	Data out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High-Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Output disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output disabled	Active (I_{CC})
L	L	X	L	L	Data in (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data in (I/O_0–I/O_7); I/O_8–I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data in (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Write	Active (I_{CC})

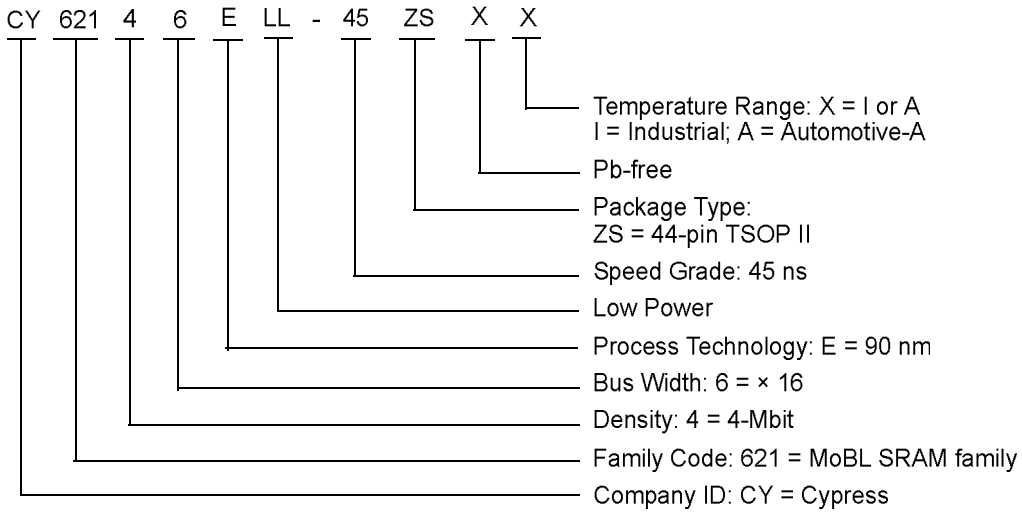
Note
31. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) must be at CMOS levels (not floating) to meet the I_{SB2} / I_{CCDR} spec. Intermediate voltage levels on these pins is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62146ELL-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	Industrial

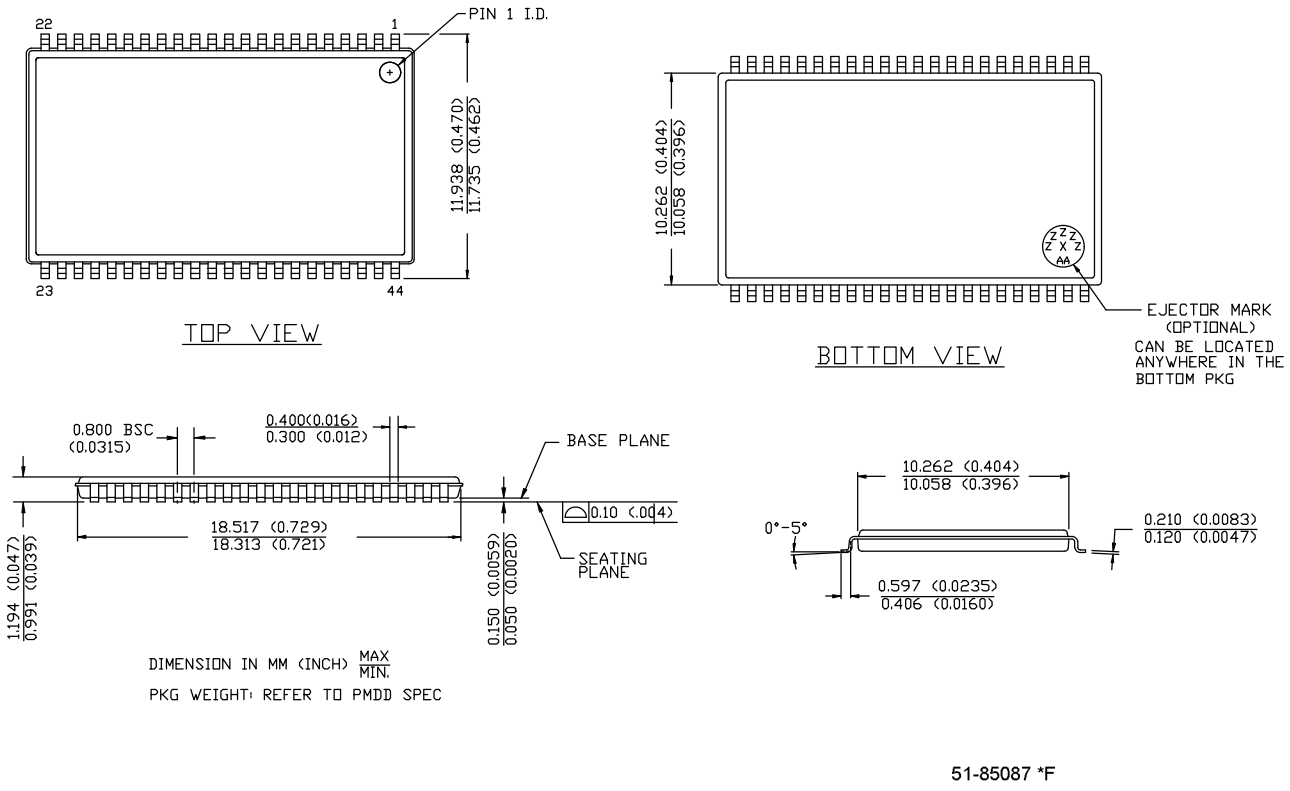
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagram

Figure 10. 44-pin TSOP II (18.4 × 10.2 × 1.194 mm) Package Outline, 51-85087



Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Gird Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62146E MoBL, 4-Mbit (256K × 16) Static RAM Document Number: 001-07970			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
**	463213	05/19/2006	New data sheet.
*A	684343	01/17/2007	Added Automotive-A Temperature Range related information in all instances across the document and made the information Preliminary (by shading in required places). Updated Ordering Information: Updated part numbers.
*B	925501	04/09/2007	Updated Electrical Characteristics: Added Note 8 and referred the same note in I_{SB2} parameter. Updated Data Retention Characteristics: Added Note 11 and referred the same note in I_{CCDR} parameter. Updated Switching Characteristics: Added Note 15 and referred the same note in “Parameter” column.
*C	1045260	05/07/2007	Changed status of Automotive-A Temperature Range related information from Preliminary to Final (by unshading in required places). Updated Ordering Information: No change in part numbers. Unshaded the Automotive-A MPNs (Changed status from Preliminary to Final).
*D	2073548	02/06/2008	Updated Data Retention Waveform: Updated Figure 3 (Corrected typo). Removed Note “$\overline{BHE}$. $\overline{BLE}$ is the AND of $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling the chip enable signals or by disabling $\overline{BHE}$ and $\overline{BLE}$.” and its reference. Updated to new template.
*E	2943752	06/03/2010	Updated Truth Table: Added Note 31 and referred the same note in “$\overline{CE}$” column. Updated Package Diagram: spec 51-85087 – Changed revision from *A to *C. Updated to new template.
*F	3109050	12/13/2010	Changed Table Footnotes to Notes in all instances across the document. Updated Ordering Information: No change in part numbers. Added Ordering Code Definitions.
*G	3149059	01/20/2011	Updated Ordering Information: No change in part numbers. Updated Ordering Code Definitions (Corrected Errors). Added Acronyms and Units of Measure. Updated to new template. Completing Sunset Review.
*H	3296704	06/29/2011	Updated Functional Description: Updated description (Removed “For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.”).
*I	3921993	03/05/2013	Updated Switching Waveforms: Added Note 25 and referred the same note in Figure 6, Figure 7. Removed Note “$\overline{WE}$ is HIGH for read cycle.” and its references in Figure 6, Figure 7. Added Note 28 and referred the same note in Figure 8, Figure 9. Updated Package Diagram: spec 51-85087 – Changed revision from *C to *E. Completing Sunset Review.

Document History Page (continued)

Document Title: CY62146E MoBL, 4-Mbit (256K × 16) Static RAM Document Number: 001-07970			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
*J	4013949	06/04/2013	Updated Functional Description: Updated description. Updated Electrical Characteristics: Added one more Test Condition "V_{CC} = 5.5 V, I_{OH} = –0.1 mA" for V_{OH} parameter and added maximum value corresponding to that Test Condition. Added Note 7 and referred the same note in maximum value for V_{OH} parameter corresponding to Test Condition "V_{CC} = 5.5 V, I_{OH} = –0.1 mA".
*K	4102022	08/14/2013	Updated Switching Characteristics: Updated Note 15. Updated to new template.
*L	4576478	11/21/2014	Updated Functional Description: Added "For a complete list of related documentation, click here." at the end. Updated Switching Characteristics: Added Note 19 and referred the same note in "Write Cycle". Updated Switching Waveforms: Added Note 30 and referred the same note in Figure 8.
*M	5196888	04/14/2016	Updated Thermal Resistance: Updated values of Θ_{JA} and Θ_{JC} parameters in "44-pin TSOP II" column. Updated to new template. Completing Sunset Review.
*N	6049346	01/29/2018	Updated Ordering Information: Updated part numbers. Updated to new template. Completing Sunset Review.
*O	6560791	04/29/2019	Updated to new template.
*P	6906316	06/26/2020	Updated Features: Changed value of Typical standby current from 1 µA to 2.5 µA. Changed value of Typical active current from 2 mA to 3.5 mA. Updated Product Portfolio: Changed typical value of Operating I_{CC} from 2 mA to 3.5 mA corresponding to "f = 1 MHz". Changed maximum value of Operating I_{CC} from 2.5 mA to 6 mA corresponding to "f = 1 MHz". Changed typical value of Standby, I_{SB2} from 1 µA to 2.5 µA. Updated Electrical Characteristics: Changed typical value of I_{CC} parameter from 2 mA to 3.5 mA corresponding to Test Condition "f = 1 MHz". Changed maximum value of I_{CC} parameter from 2.5 mA to 6 mA corresponding to Test Condition "f = 1 MHz". Changed typical value of I_{SB2} parameter from 1 µA to 2.5 µA. Updated Data Retention Characteristics: Changed typical value of I_{CCDR} parameter from 1 µA to 3 µA. Changed maximum value of I_{CCDR} parameter from 7 µA to 8.8 µA. Updated Package Diagram: spec 51-85087 – Changed revision from *E to *F. Updated to new template.

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CY62146ESL MoBL

4-Mbit (256K × 16) Static RAM

Features

- Very high speed: 45 ns
- Wide voltage range: 2.2 V to 3.6 V and 4.5 V to 5.5 V
- Ultra low standby power
  - Typical Standby current: 2.5 µA
  - Maximum Standby current: 7 µA
- Ultra low active power
  - Typical active current: 3.5 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 44-pin thin small outline package (TSOP) II package

Functional Description

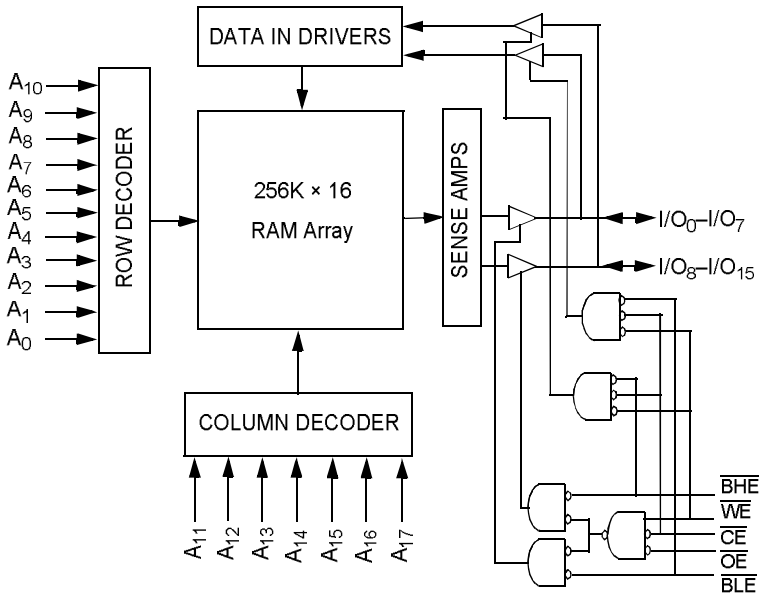
The CY62146ESL is a high performance CMOS static RAM organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected ($\overline{CE}$ HIGH). The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH) or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{17}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{17}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appears on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See the Truth Table on page 11 for a complete description of read and write modes.

For a complete list of related documentation, click here.

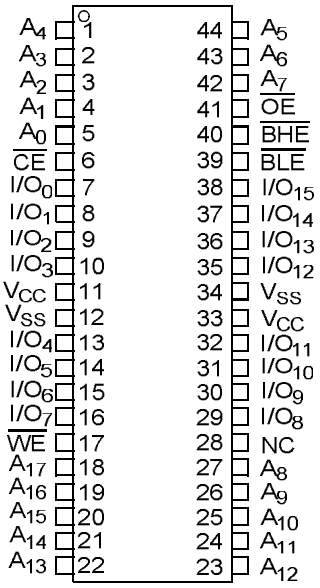
Logic Block Diagram



Contents

Pin Configurations

Figure 1. 44-pin TSOP II pinout (Top View) [1]



Product Portfolio

Product	Range	V_{CC} Range (V) [2]	Speed (ns)	Power Dissipation					
				Operating I_{CC}, (mA)				Standby, I_{SB2} (µA)	
				f = 1MHz		f = f_{max}			
				Typ [3]	Max	Typ [3]	Max	Typ [3]	Max
CY62146ESL	Industrial	2.2 V–3.6 V and 4.5 V–5.5 V	45	3.5	6	15	20	2.5	7

Notes
1. NC pins are not connected on the die.
2. Datasheet specifications are not guaranteed for V_{CC} in the range of 3.6 V to 4.5 V.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V, and V_{CC} = 5 V, T_A = 25 °C.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential .....–0.5 V to 6.0 V

DC voltage applied to outputs in High Z State [4, 5] .....–0.5 V to 6.0 V

DC input voltage [4, 5] .....–0.5 V to 6.0 V

Output current into outputs (LOW) .....20 mA

Static discharge voltage (MIL-STD-883, Method 3015) ..... >2001 V

Latch up current ..... >200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[6]
CY62146ESL	Industrial	–40 °C to +85 °C	2.2 V–3.6 V, and 4.5 V–5.5 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		45 ns			Unit
				Min	Typ [7]	Max	
V_{OH}	Output high voltage	$2.2 \le V_{CC} \le 2.7$	I_{OH} = –0.1 mA	2.0	–	–	V
		$2.7 \le V_{CC} \le 3.6$	I_{OH} = –1.0 mA	2.4	–	–	
		$4.5 \le V_{CC} \le 5.5$	I_{OH} = –1.0 mA	2.4	–	–	
V_{OL}	Output low voltage	$2.2 \le V_{CC} \le 2.7$	I_{OL} = 0.1 mA	–	–	0.4	V
		$2.7 \le V_{CC} \le 3.6$	I_{OL} = 2.1mA	–	–	0.4	
		$4.5 \le V_{CC} \le 5.5$	I_{OL} = 2.1mA	–	–	0.4	
V_{IH}	Input high voltage	$2.2 \le V_{CC} \le 2.7$		1.8	–	V_{CC} + 0.3	V
		$2.7 \le V_{CC} \le 3.6$		2.2	–	V_{CC} + 0.3	
		$4.5 \le V_{CC} \le 5.5$		2.2	–	V_{CC} + 0.5	
V_{IL}	Input low voltage	$2.2 \le V_{CC} \le 2.7$		–0.3	–	0.6	V
		$2.7 \le V_{CC} \le 3.6$		–0.3	–	0.8	
		$4.5 \le V_{CC} \le 5.5$		–0.5	–	0.8	
I_{IX}	Input Leakage Current	$GND \le V_I \le V_{CC}$		–1	–	+1	µA
I_{OZ}	Output Leakage Current	$GND \le V_O \le V_{CC}$, Output Disabled		–1	–	+1	µA
I_{CC}	V_{CC} Operating Supply Current	$f = f_{max} = 1/t_{RC}$	$V_{CC} = V_{CCmax}$, I_{OUT} = 0 mA, CMOS levels	–	15	20	mA
		f = 1 MHz		–	3.5	6	
I_{SB1}[8]	Automatic CE Power down Current – CMOS Inputs	$\overline{CE} \ge V_{CC}$ – 0.2 V, $V_{IN} \ge V_{CC}$ – 0.2 V or $V_{IN} \le$ 0.2 V, f = f_{max} (Address and Data Only), f = 0 ($\overline{OE}$, $\overline{BHE}$, $\overline{BLE}$ and $\overline{WE}$), $V_{CC} = V_{CC(max)}$		–	2.5	7	µA
I_{SB2}[8]	Automatic CE Power down Current – CMOS Inputs	$\overline{CE} \ge V_{CC}$ – 0.2 V, $V_{IN} \ge V_{CC}$ – 0.2 V or $V_{IN} \le$ 0.2 V, f = 0, $V_{CC} = V_{CC(max)}$		–	2.5	7	µA

Notes

4. V_{IL}(min) = –2.0V for pulse durations less than 20 ns.
5. V_{IH}(max) = V_{CC} + 0.75 V for pulse durations less than 20 ns.
6. Full Device AC operation assumes a 100 µs ramp time from 0 to V_{CC} (min) and 200 µs wait time after V_{CC} stabilization.
7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V, and V_{CC} = 5 V, T_A = 25 °C.
8. Chip enable ($\overline{CE}$) must be HIGH at CMOS level to meet the I_{SB1}/I_{SB2}/I_{CCDR} spec. Other inputs can be left floating.

Capacitance

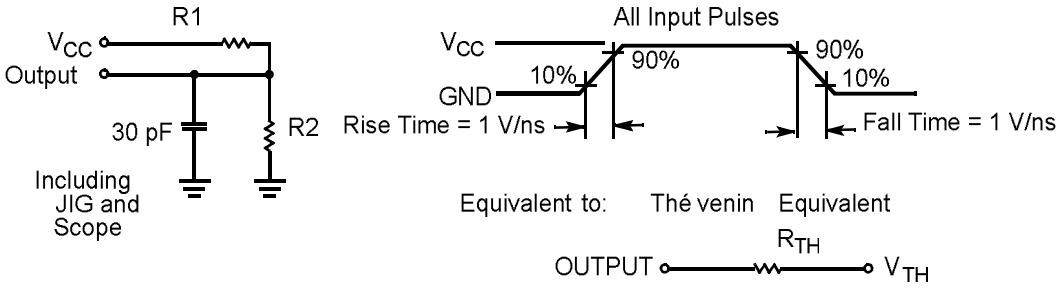
Parameter [9]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [9]	Description	Test Conditions	TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	57.92	°C/W
Θ_{JC}	Thermal resistance (junction to case)		17.44	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameter	2.5 V	3.0 V	5.0 V	Unit
R1	16667	1103	1800	Ω
R2	15385	1554	990	Ω
R_{TH}	8000	645	639	Ω
V_{TH}	1.20	1.75	1.77	V

Note
9. Tested initially and after any design or process changes that may affect these parameters.

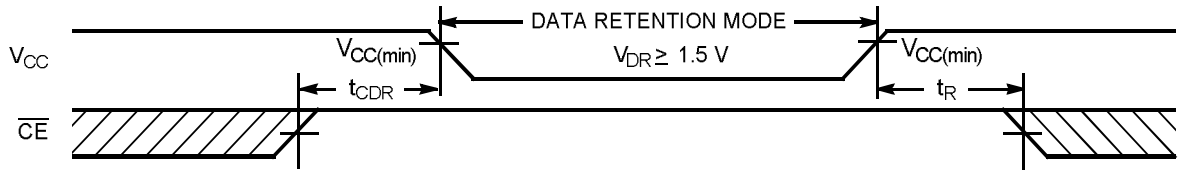
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions		Min	Typ [10]	Max	Unit
V_{DR}	V_{CC} for data retention			1.5	–	–	V
I_{CCDR} [11]	Data retention current	$\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	V_{CC} = 1.5 V	–	3	8.8	µA
t_{CDR} [12]	Chip deselect to data retention time			0	–	–	ns
t_R [13]	Operation recovery time			45	–	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes

10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V, and V_{CC} = 5 V, T_A = 25 °C.
11. Chip enable ($\overline{CE}$) must be HIGH at CMOS level to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
12. Tested initially and after any design or process changes that may affect these parameters.
13. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.

Switching Characteristics

Over the Operating Range

Parameter [14, 15]	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	45	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z [16]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [16, 17]	–	18	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z [16]	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z [16, 17]	–	18	ns
t_{PU}	$\overline{CE}$ LOW to power up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power down	–	45	ns
t_{DBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to data valid	–	22	ns
t_{LZBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to Low Z [16]	5	–	ns
t_{HZBE}	$\overline{BLE}$/$\overline{BHE}$ HIGH to High Z [16, 17]	–	18	ns
Write Cycle [18, 19]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to Write Start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	ns
t_{BW}	$\overline{BLE}$/$\overline{BHE}$ LOW to write end	35	–	ns
t_{SD}	Data Setup to write end	25	–	ns
t_{HD}	Data Hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [16, 17]	–	18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [16]	10	–	ns

Notes

14. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Note AN66311. However, the issue has been fixed and in production now, and hence, this Application Note is no longer applicable. It is available for download on our website as it contains information on the date code of the parts, beyond which the fix has been in production.
15. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3 V, and output loading of the specified I_{OL}/I_{OH} as shown in the Figure 2 on page 5.
16. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
17. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
18. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
19. The minimum write cycle time for Write Cycle No. 4 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [20, 21]

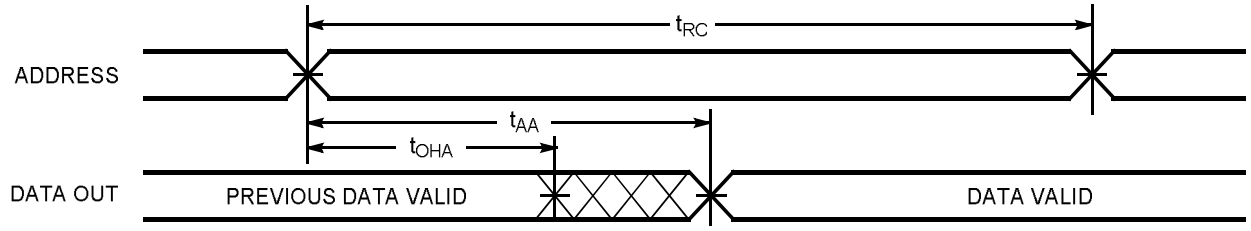
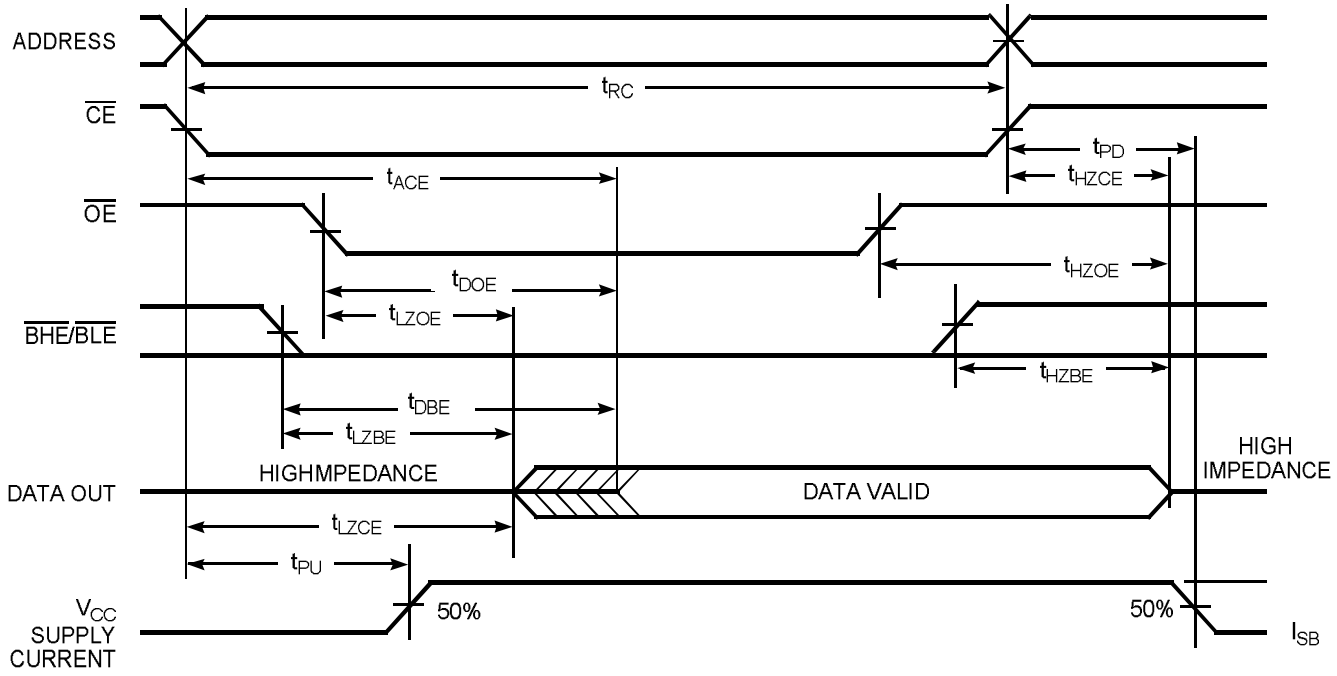


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [21, 22]



Notes
20. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$, or both = V_{IL}.
21. $\overline{WE}$ is HIGH for read cycle.
22. Address valid before or similar to $\overline{CE}$, $\overline{BHE}$, $\overline{BLE}$ transition LOW.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ($\overline{WE}$ Controlled) [23, 24]

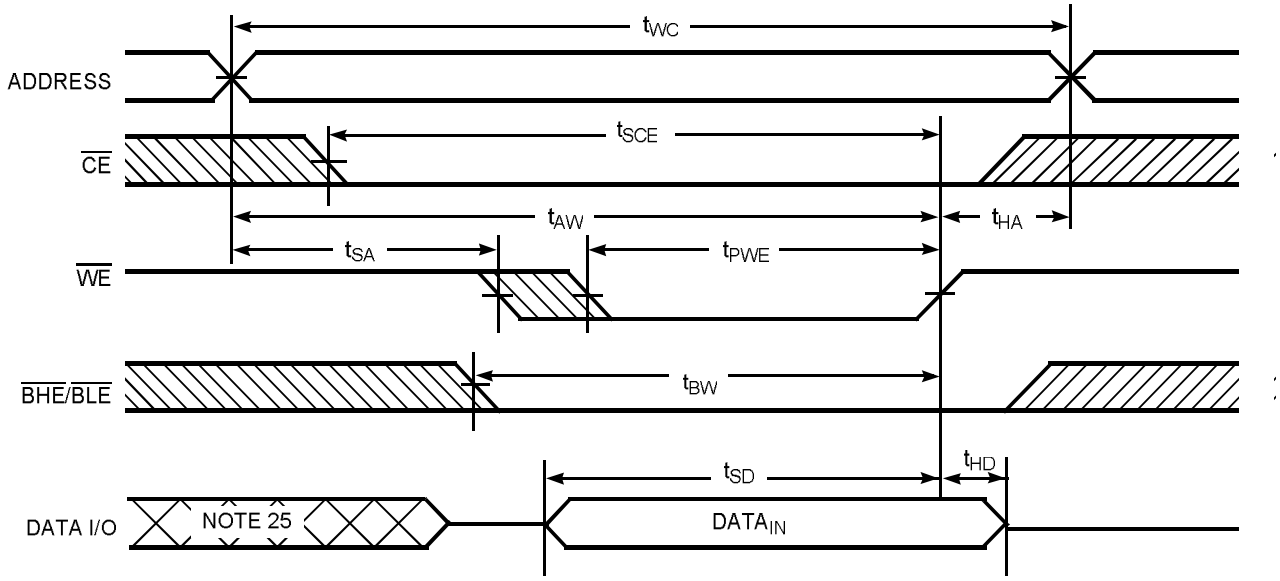
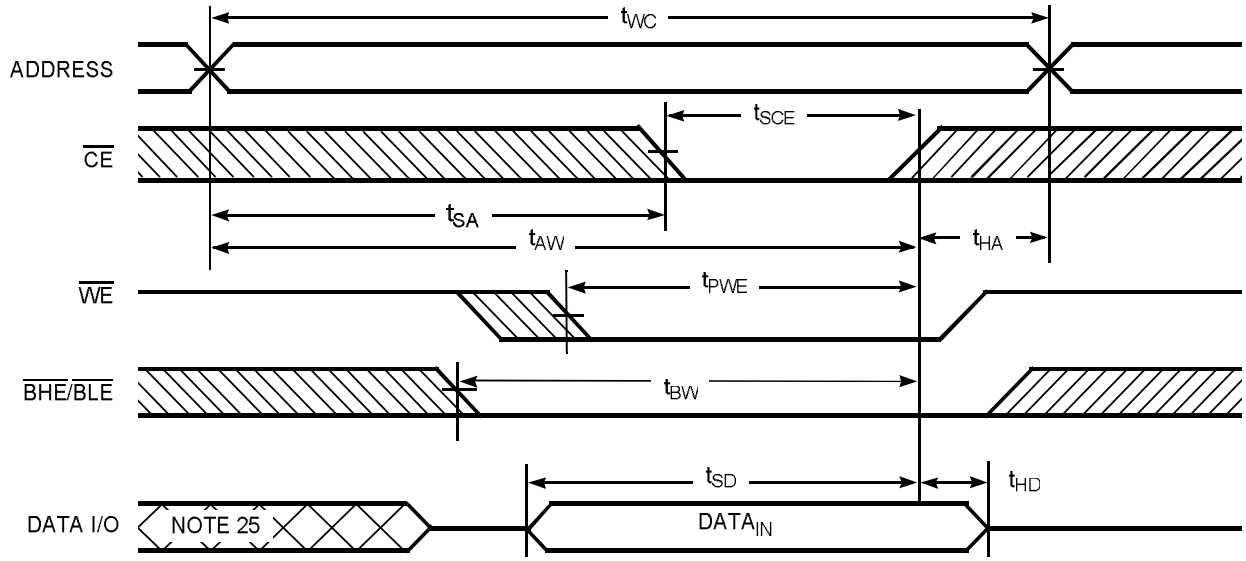


Figure 7. Write Cycle No. 2 ($\overline{CE}$ Controlled) [23, 24]



Notes

23. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
24. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
25. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 (BHE/BLE Controlled) [26]

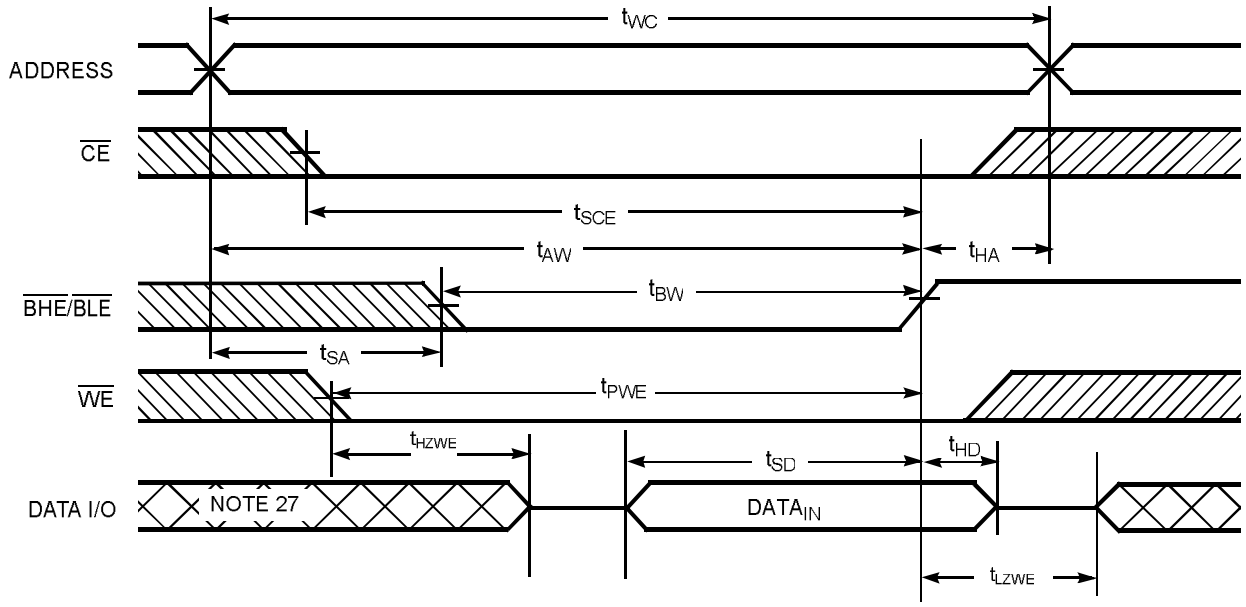
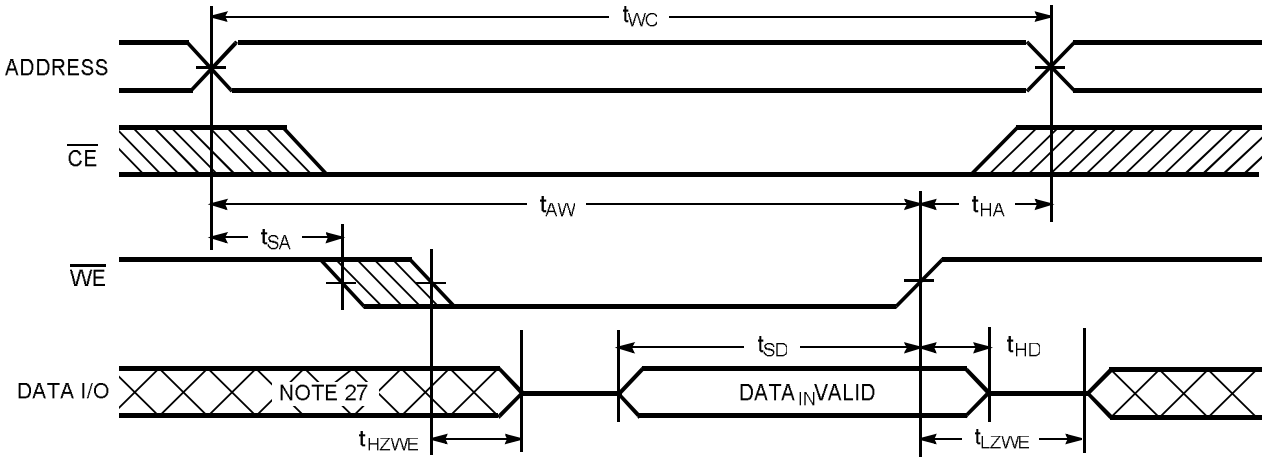


Figure 9. Write Cycle No. 4 (WE Controlled, OE LOW) [28]



Notes
26. If CE goes HIGH simultaneously with WE = V_{IH}, the output remains in a high impedance state.
27. During this period, the I/Os are in output state. Do not apply input signals.
28. The minimum write cycle time for Write Cycle No. 4 (WE Controlled, OE LOW) is the sum of t_{HZWE} and t_{SD}.

Truth Table

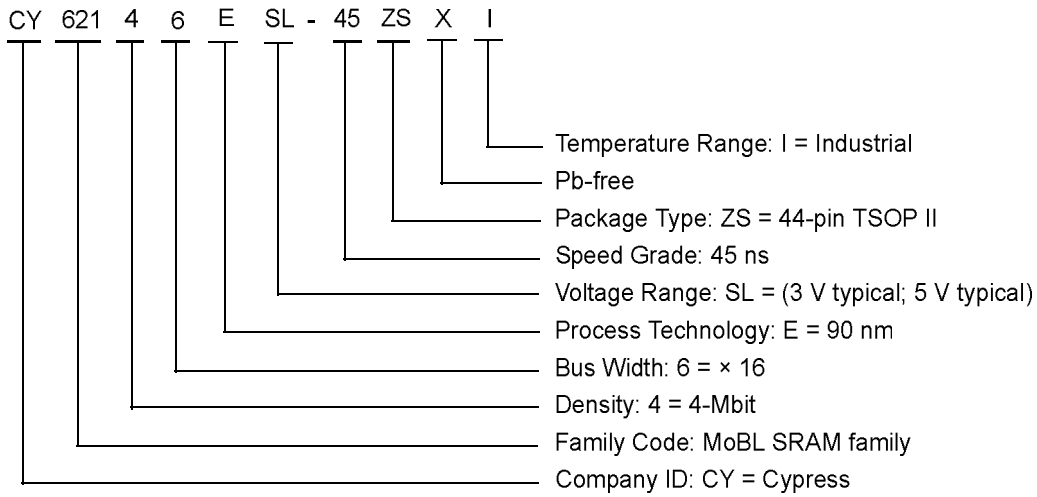
$\overline{CE}$ [29]	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High-Z	Deselect/Power down	Standby (I_{SB})
L	X	X	H	H	High-Z	Output disabled	Active (I_{CC})
L	H	L	L	L	Data Out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O_0–I/O_7); I/O_8–I/O_{15} in High-Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High-Z	Read	Active (I_{CC})
L	H	H	L	L	High-Z	Output disabled	Active (I_{CC})
L	H	H	H	L	High-Z	Output disabled	Active (I_{CC})
L	H	H	L	H	High-Z	Output disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O_0–I/O_7); I/O_8–I/O_{15} in High-Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (I/O_8–I/O_{15}); I/O_0–I/O_7 in High-Z	Write	Active (I_{CC})

Note
29. Chip enable must be at CMOS levels (not floating). Intermediate voltage levels on this pin is not permitted.

Ordering Information

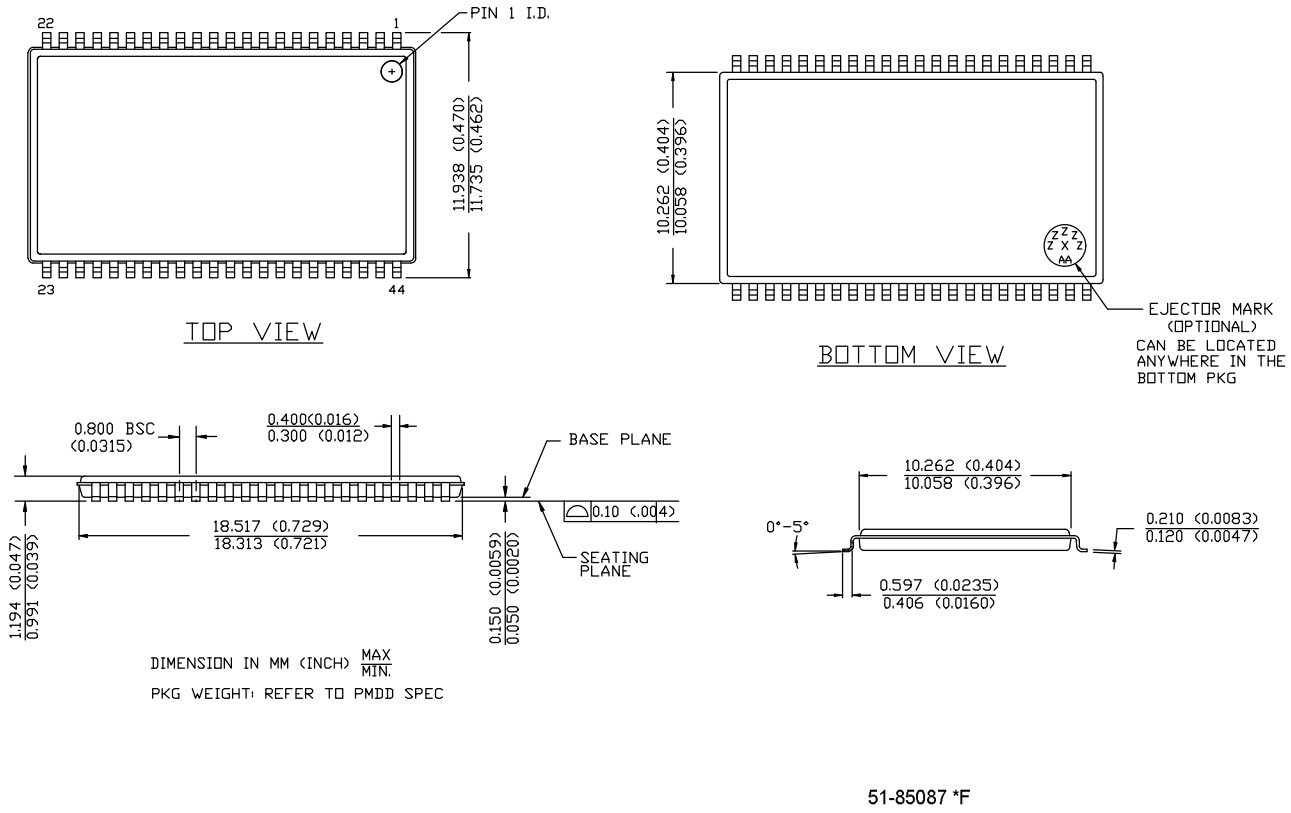
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62146ESL-45ZSXI	51-85087	44-pin TSOP Type II (Pb-free)	Industrial

Ordering Code Definitions



Package Diagram

Figure 10. 44-pin TSOP II (18.4 × 10.2 × 1.194 mm) Package Outline, 51-85087



Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62146ESL MoBL, 4-Mbit (256K × 16) Static RAM Document Number: 001-43142			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
**	1875228	01/02/2008	New data sheet.
*A	2944332	06/04/2010	Updated Electrical Characteristics: Added Note 8 and referred the same note in I_{SB2} parameter. Updated Truth Table: Added Note 29 and referred the same note in $\overline{CE}$ column. Updated Package Diagram: spec 51-85087 – Changed revision from *A to *C. Added Acronyms. Updated to new template.
*B	3109186	12/13/2010	Changed Table Footnotes to Footnotes. Updated Ordering Information: No change in part numbers. Added Ordering Code Definitions. Completing Sunset Review.
*C	3296704	06/29/2011	Updated Functional Description: Updated description (Removed “For best practice recommendations, refer to the Cypress Application Note AN1064, SRAM System Guidelines.”). Updated Electrical Characteristics: Updated Note 8 (Added I_{SB1}) and referred the same note in I_{SB1} parameter. Updated Capacitance: Added Note 9 and referred the same note in parameter column. Updated Thermal Resistance: Added Note 9 and referred the same note in parameter column. Updated Data Retention Characteristics: Added Note 11 and referred the same note in I_{CCDR} parameter. Changed minimum value of t_R parameter from t_{RC} to 45 ns. Updated Switching Characteristics: Moved Note 14 to parameter column. Added Units of Measure.
*D	3903350	02/13/2013	Updated Switching Waveforms: Updated Figure 6 (Removed $\overline{OE}$ signal). Updated Figure 7 (Removed $\overline{OE}$ signal). Removed the Note “Data I/O is high impedance if $\overline{OE}$ = V_{IH}.” and its reference in Figure 6, Figure 7. Removed the figure “Write Cycle 3: $\overline{WE}$ controlled, $\overline{OE}$ LOW”. Updated Figure 8 (Removed “$\overline{OE}$ LOW” in caption only). Updated Package Diagram: spec 51-85087 – Changed revision from *C to *E. Completing Sunset Review.
*E	4100920	08/21/2013	Updated Switching Characteristics: Added Note 14 and referred the same note in “Parameter” column. Updated to new template.
*F	4576406	01/16/2015	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated Switching Characteristics: Added Note 19 and referred the same note in “Write Cycle”. Updated Switching Waveforms: Added Figure 9. Added Note 28 and referred the same note in Figure 9.

Document History Page (continued)

Document Title: CY62146ESL MoBL, 4-Mbit (256K × 16) Static RAM Document Number: 001-43142			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
*G	5169392	03/10/2016	Updated Thermal Resistance: Replaced “two-layer” with “four-layer” in “Test Conditions” column. Changed value of Θ_{JA} parameter from 77 °C/W to 57.92 °C/W. Changed value of Θ_{JC} parameter from 13 °C/W to 17.44 °C/W. Updated to new template. Completing Sunset Review.
*H	5983493	12/04/2017	Updated Cypress Logo and Copyright.
*I	6529117	04/01/2019	Updated to new template. Completing Sunset Review.
*J	6906316	06/26/2020	Updated Features: Changed value of Typical standby current from 1 µA to 2.5 µA. Changed value of Typical active current from 2 mA to 3.5 mA. Updated Product Portfolio: Changed typical value of Operating I_{CC} from 2 mA to 3.5 mA corresponding to “f = 1 MHz”. Changed maximum value of Operating I_{CC} from 2.5 mA to 6 mA corresponding to “f = 1 MHz”. Changed typical value of Standby, I_{SB2} from 1 µA to 2.5 µA. Updated Electrical Characteristics: Changed typical value of I_{CC} parameter from 2 mA to 3.5 mA corresponding to Test Condition “f = 1 MHz”. Changed maximum value of I_{CC} parameter from 2.5 mA to 6 mA corresponding to Test Condition “f = 1 MHz”. Changed typical value of I_{SB1} parameter from 1 µA to 2.5 µA. Changed typical value of I_{SB2} parameter from 1 µA to 2.5 µA. Updated Data Retention Characteristics: Changed typical value of I_{CCDR} parameter from 1 µA to 3 µA. Changed maximum value of I_{CCDR} parameter from 7 µA to 8.8 µA. Updated Package Diagram: spec 51-85087 – Changed revision from *E to *F. Updated to new template.

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CY62148ESL MoBL

4-Mbit (512K × 8) Static RAM

Features

- Higher speed up to 55 ns
- Wide voltage range: 2.2 V to 3.6 V and 4.5 V to 5.5 V
- Ultra low standby power
  - Typical standby current: 2.5 µA
  - Maximum standby current: 7 µA
- Ultra low active power
  - Typical active current: 3.5 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 32-pin shrunk thin small outline package (STSOP) package

Functional Description

The CY62148ESL is a high performance CMOS static RAM organized as 512K words by 8-bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications. The device also has an automatic power-down feature that significantly reduces power consumption. Placing the device in standby mode reduces power consumption by more than 99 percent when deselected ($\overline{CE}$ HIGH). The eight input and output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

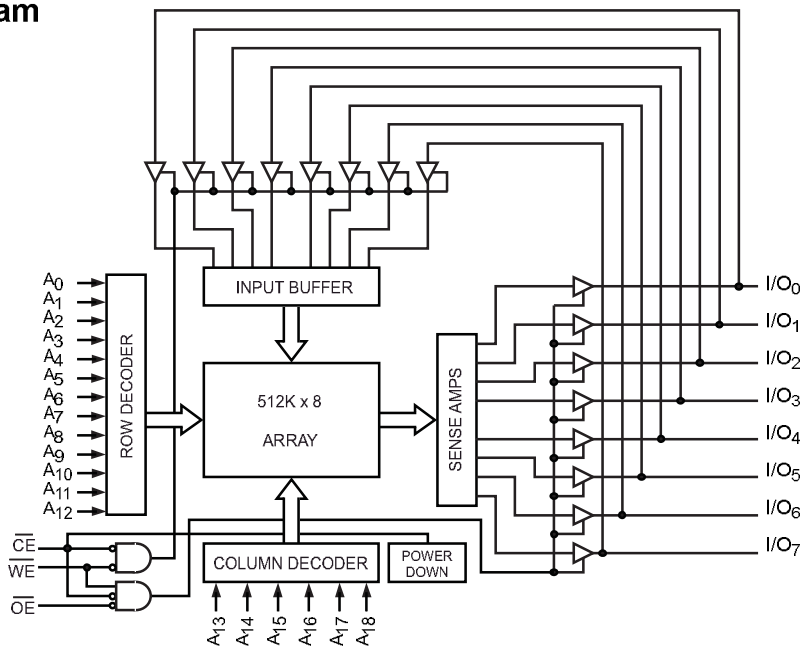
To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

The CY62148ESL device is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please see Electrical Characteristics on page 4 for more details and suggested alternatives.

For a complete list of related resources, click here.

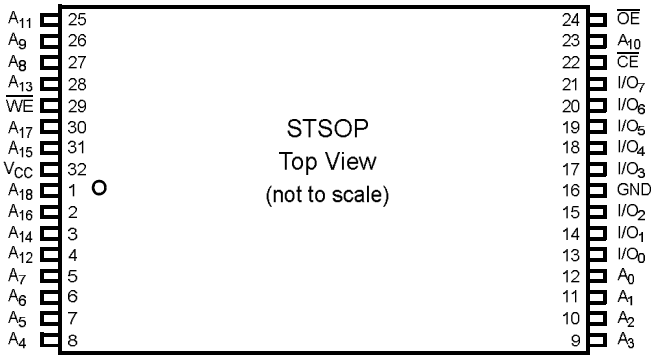
Logic Block Diagram



Contents

Pin Configuration

Figure 1. 32-pin STSOP (Top View) pinout



Product Portfolio

Product	Range	V_{CC} Range (V) [1]	Speed (ns)	Power Dissipation					
				Operating I_{CC}, (mA)				Standby, I_{SB2} (µA)	
				f = 1 MHz		f = f_{max}			
				Typ [2]	Max	Typ [2]	Max	Typ [2]	Max
CY62148ESL	Industrial/ Automotive-A	2.2 V to 3.6 V and 4.5 V to 5.5 V	55	3.5	6	15	20	2.5	7

Notes
1. Data sheet specifications are not guaranteed for V_{CC} in the range of 3.6 V to 4.5 V.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ... 55 °C to +125 °C

Supply voltage to ground potential ..... –0.5 V to 6.0 V

DC voltage applied to outputs in high Z state [3, 4] ..... –0.5 V to 6.0 V

DC input voltage [3, 4] ..... –0.5 V to 6.0 V

Output current into outputs (low) .....20 mA

Static discharge voltage (MIL-STD-883, Method 3015) .....> 2001 V

Latch-up current .....> 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[5]
CY62148ESL	Industrial/ Automotive-A	–40 °C to +85 °C	2.2 V to 3.6 V, and 4.5 V to 5.5 V

Electrical Characteristics

Over the operating range

Parameter	Description	Test Conditions		55 ns (Industrial/Automotive-A)			Unit
				Min	Typ [6]	Max	
V_{OH}	Output HIGH voltage	$2.2 \le V_{CC} \le 2.7$	$I_{OH} = -0.1$ mA	2.0	–	–	V
		$2.7 \le V_{CC} \le 3.6$	$I_{OH} = -1.0$ mA	2.4	–	–	
		$4.5 \le V_{CC} \le 5.5$	$I_{OH} = -1.0$ mA	2.4	–	–	
		$4.5 \le V_{CC} \le 5.5$	$I_{OH} = -0.1$ mA	–	–	3.4 [7]	
V_{OL}	Output LOW voltage	$2.2 \le V_{CC} \le 2.7$	$I_{OL} = 0.1$ mA	–	–	0.4	V
		$2.7 \le V_{CC} \le 3.6$	$I_{OL} = 2.1$ mA	–	–	0.4	
		$4.5 \le V_{CC} \le 5.5$	$I_{OL} = 2.1$ mA	–	–	0.4	
V_{IH}	Input HIGH voltage	$2.2 \le V_{CC} \le 2.7$		1.8	–	$V_{CC} + 0.3$	V
		$2.7 \le V_{CC} \le 3.6$		2.2	–	$V_{CC} + 0.3$	
		$4.5 \le V_{CC} \le 5.5$		2.2	–	$V_{CC} + 0.5$	
V_{IL} [8]	Input LOW voltage	$2.2 \le V_{CC} \le 2.7$		–0.3	–	0.4	V
		$2.7 \le V_{CC} \le 3.6$		–0.3	–	0.6	
		$4.5 \le V_{CC} \le 5.5$		–0.5	–	0.6	
I_{IX}	Input leakage current	$GND \le V_{IN} \le V_{CC}$		–1	–	+1	µA
I_{OZ}	Output leakage current	$GND \le V_O \le V_{CC}$, output disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	$f = f_{max} = 1/t_{RC}$	$V_{CC} = V_{CCmax}$, $I_{OUT} = 0$ mA, CMOS levels	–	15	20	mA
		f = 1 MHz		–	3.5	6	
I_{SB1}[9]	Automatic CE power-down current – CMOS inputs	$\overline{CE} \ge V_{CC} - 0.2$ V, $V_{IN} \ge V_{CC} - 0.2$ V or $V_{IN} \le 0.2$ V, f = f_{max} (address and data only), f = 0 ($\overline{OE}$ and $\overline{WE}$), $V_{CC} = V_{CC(max)}$		–	2.5	7	µA
				–			
I_{SB2}[9]	Automatic CE power-down current – CMOS inputs	$\overline{CE} \ge V_{CC} - 0.2$ V, $V_{IN} \ge V_{CC} - 0.2$ V or $V_{IN} \le 0.2$ V, f = 0, $V_{CC} = V_{CC(max)}$		–	2.5	7	µA
				–			

Notes

3. $V_{IL(min)} = -2.0$ V for pulse durations less than 20 ns.
4. $V_{IH(max)} = V_{CC} + 0.75$ V for pulse durations less than 20 ns.
5. Full device AC operation assumes a minimum of 100 µs ramp time from 0 to $V_{CC(min)}$ and 200 µs wait time after V_{CC} stabilization.
6. Typical values are included for reference and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.
7. Please note that the maximum VOH limit does not exceed minimum CMOS VIH of 3.5 V. If you are interfacing this SRAM with 5 V legacy processors that require a minimum VIH of 3.5 V, please refer to Application Note AN6081 for technical details and options you may consider
8. Under DC conditions the device meets a V_{IL} of 0.8 V (for V_{CC} range of 2.7 V to 3.6 V and 4.5 V to 5.5 V) and 0.6 V (for V_{CC} range of 2.2 V to 2.7 V). However, in dynamic conditions Input LOW voltage applied to the device must not be higher than 0.6 V and 0.4 V for the above ranges.
9. Chip enable ($\overline{CE}$) must be HIGH at CMOS level to meet the $I_{SB1}/I_{SB2}/I_{CCDR}$ spec. Other inputs can be left floating.

Capacitance

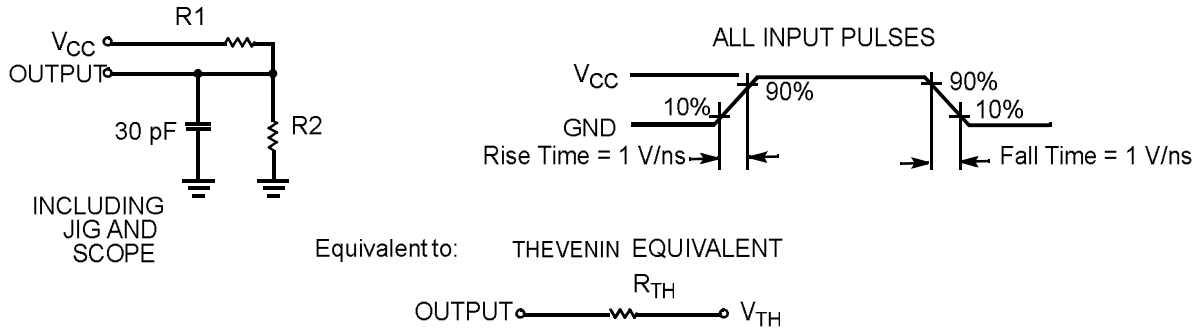
Parameter [10]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(Typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [10]	Description	Test Conditions	32-pin STSOP	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	49.02	°C/W
Θ_{JC}	Thermal resistance (junction to case)		14.07	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameter	2.5 V	3.0 V	5.0 V	Unit
R1	16667	1103	1800	Ω
R2	15385	1554	990	Ω
R_{TH}	8000	645	639	Ω
V_{TH}	1.20	1.75	1.77	V

Note
10. Tested initially and after any design or process changes that may affect these parameters.

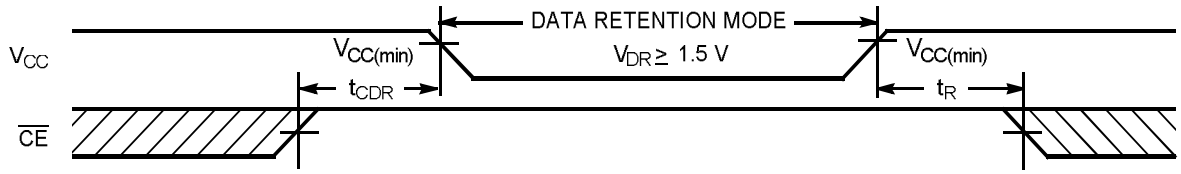
Data Retention Characteristics

Over the operating range

Parameter	Description	Conditions		Min	Typ [11]	Max	Unit
V_{DR}	V_{CC} for data retention			1.5	–	–	V
I_{CCDR} [12]	Data retention current	$\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, $V_{CC} = 1.5$ V	Industrial / Automotive-A	–	3	8.8	µA
t_{CDR}	Chip deselect to data retention time			0	–	–	ns
t_R [13]	Operation recovery time			55	–	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes

11. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.
12. Chip enable ($\overline{CE}$) must be HIGH at CMOS level to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
13. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.

Switching Characteristics

Over the operating range

Parameter [14, 15]	Description	55 ns (Industrial / Automotive-A)		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	55	–	ns
t_{AA}	Address to data valid	–	55	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	25	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z [16]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z [16, 17]	–	20	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z [16]	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z [16, 17]	–	20	ns
t_{PU}	$\overline{CE}$ LOW to power-up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-up	–	55	ns
Write Cycle [18, 19]				
t_{WC}	Write cycle time	55	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	40	–	ns
t_{AW}	Address setup to write end	40	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	40	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z [16, 17]	–	20	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z [16]	10	–	ns

Notes

14. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the chip enable signal as described in the Application Note AN66311. However, the issue has been fixed and in production now, and hence, this Application Notes is no longer applicable. It is available for download on our website as it contains information on the date code of the parts, beyond which the fix has been in production.
15. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in Figure 2 on page 5.
16. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
17. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the output enter a high impedance state.
18. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
19. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [20, 21]

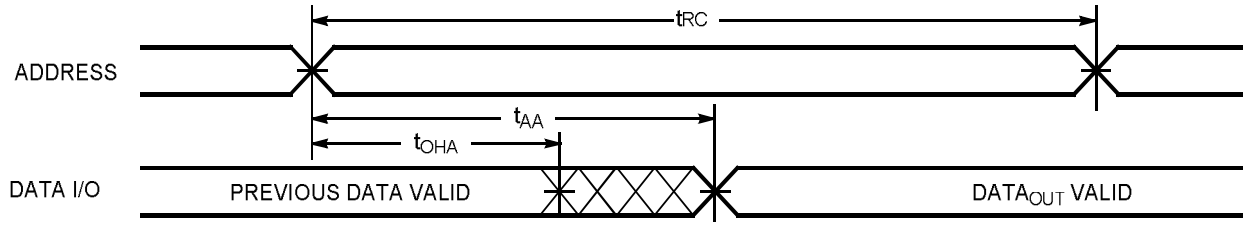
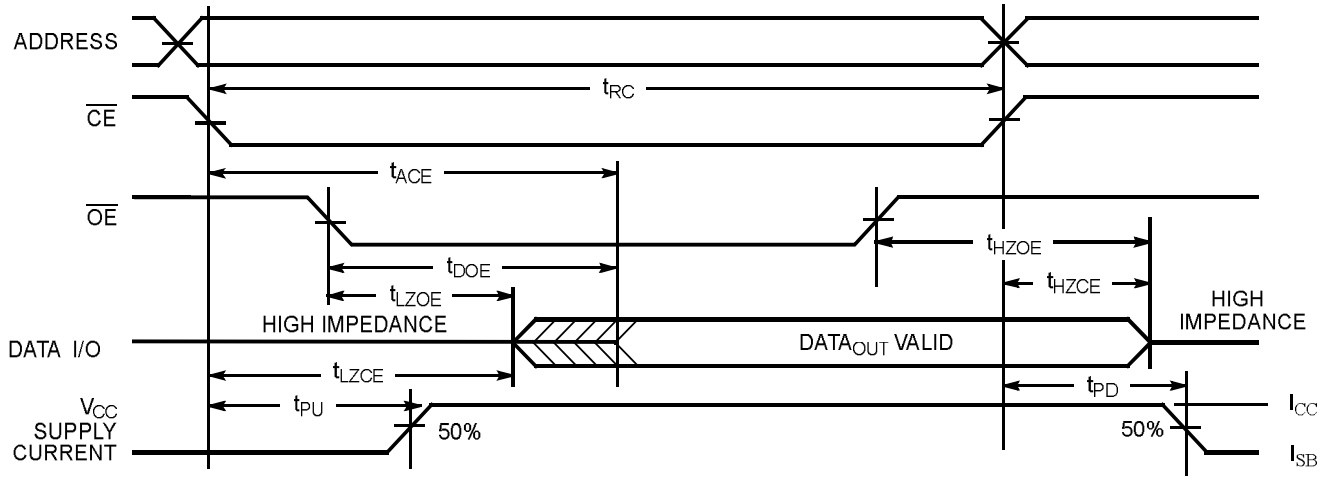


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [21, 22]



Notes
20. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
21. $\overline{WE}$ is HIGH for read cycles.
22. Address valid before or similar to $\overline{CE}$ transition LOW.
23. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
24. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
25. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ($\overline{CE}$ Controlled) [26, 27]

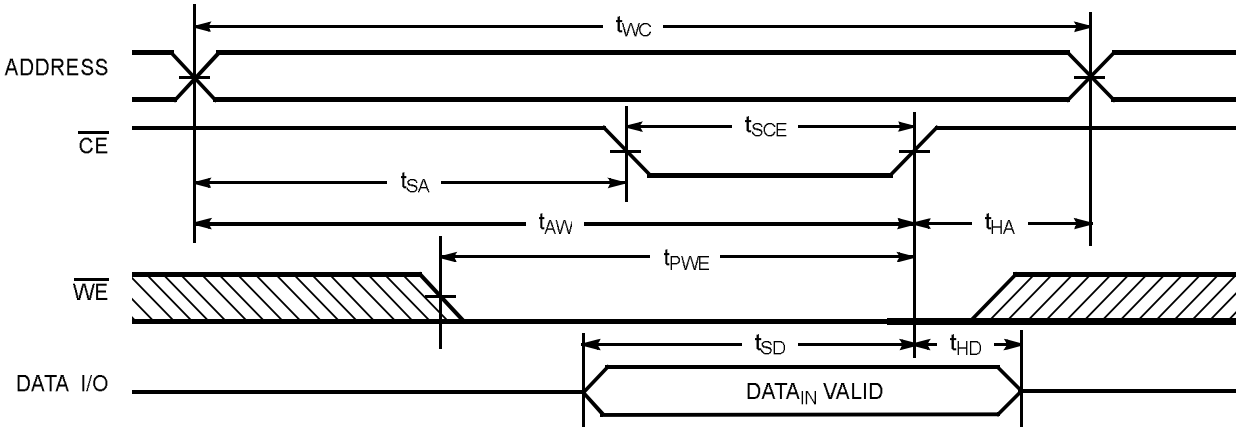
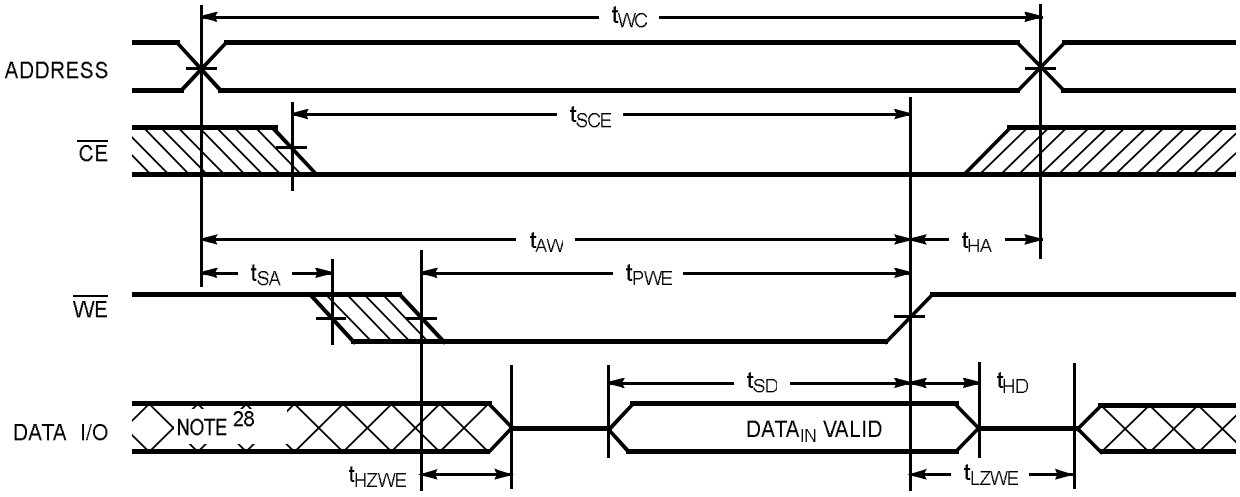


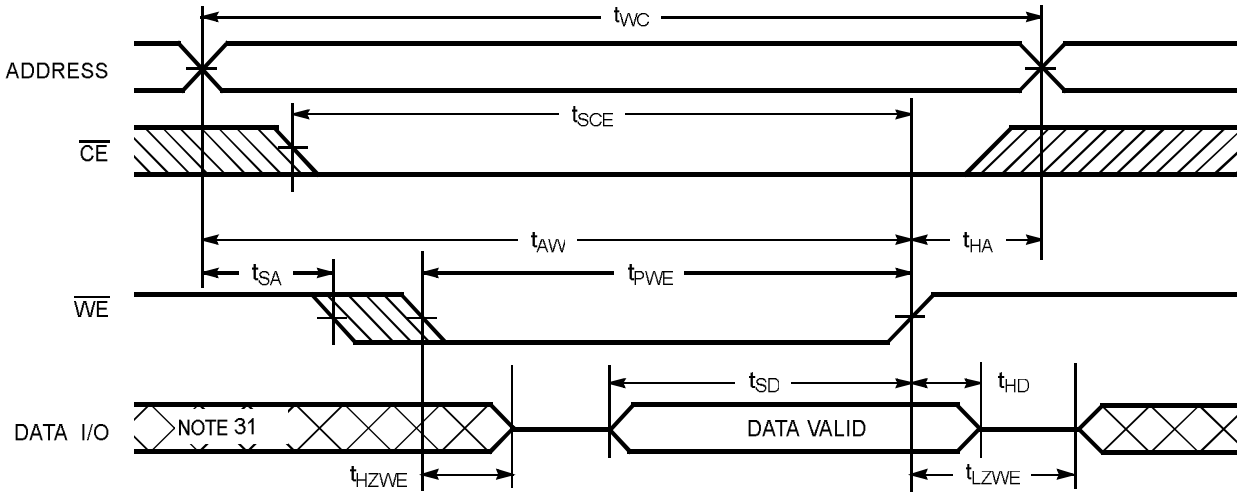
Figure 7. Write Cycle No. 2 ($\overline{WE}$ Controlled) [27]



Notes
26. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
27. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
28. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [29, 30]



Notes
29. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
30. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE}.
31. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Mode	Power
H [32]	X	X	High Z	Deselect/power-down	Standby (I_{SB})
L	H	L	Data out	Read	Active (I_{CC})
L	H	H	High Z	Output disabled	Active (I_{CC})
L	L	X	Data in	Write	Active (I_{CC})

Note
32. Chip enable ($\overline{CE}$) must be HIGH at CMOS level to meet the I_{SB1}/ I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

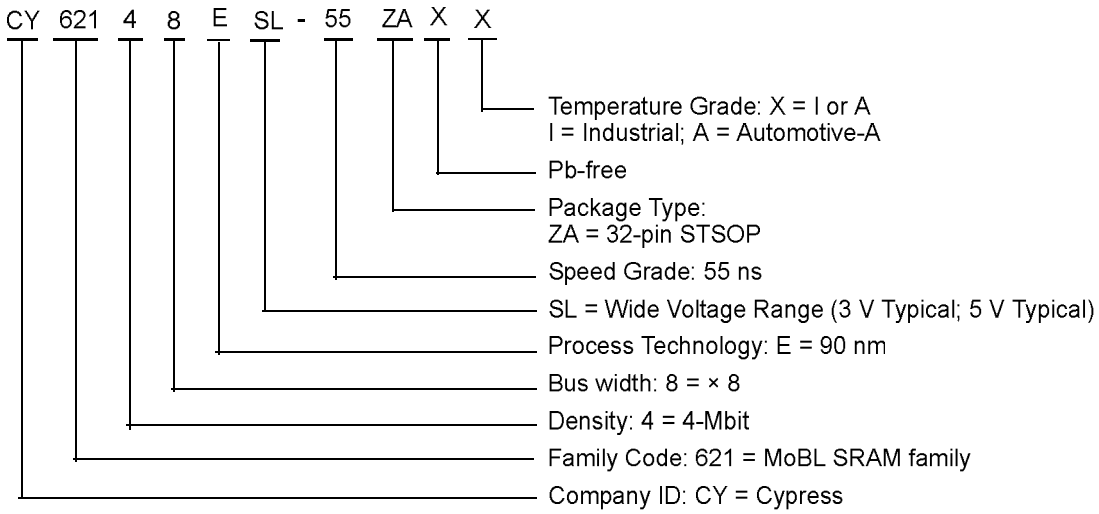
Ordering Information

Table 1 lists the CY62148ESL MoBL key package features and ordering codes. The table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products.

Table 1. Key features and Ordering Information

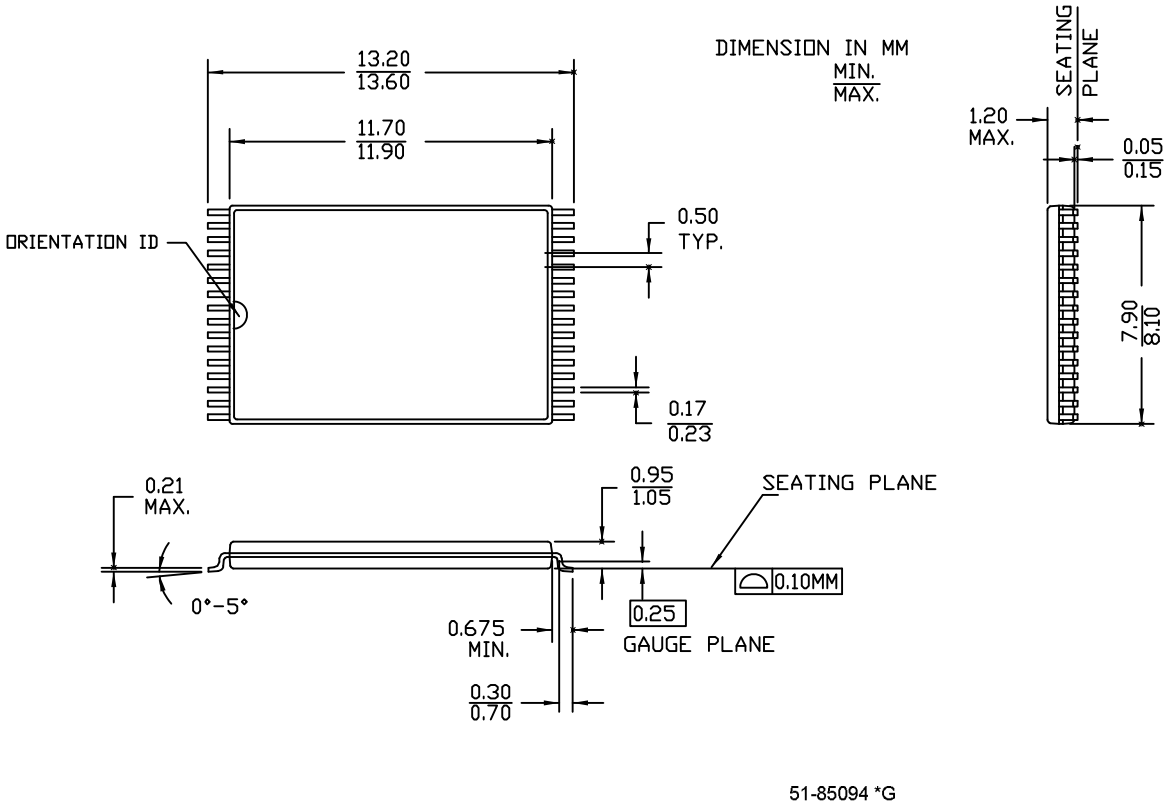
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62148ESL-55ZAXI	51-85094	32-pin STSOP (Pb-free)	Industrial
	CY62148ESL-55ZAXA	51-85094	32-pin STSOP (Pb-free)	Automotive-A

Ordering Code Definitions



Package Diagram

Figure 9. 32-pin STSOP (8 × 13.4 × 1.2 mm) ZA32 Package Outline, 51-85094



Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62148ESL MoBL, 4-Mbit (512K × 8) Static RAM Document Number: 001-50045			
Rev.	**ECN**	**Submission Date**	**Description of Change**
**	2612938	01/21/2009	New data sheet.
*A	2800124	11/06/2009	Updated Product Portfolio (Included Automotive-A information). Updated Operating Range (Included Automotive-A information). Updated Ordering Information: Updated part numbers.
*B	2947039	06/10/2010	Updated Electrical Characteristics: Added Note 9 and referred the same note in I_{SB2} parameter. Updated Truth Table: Added Note 32 and referred the same note in "$\overline{CE}$" column. Updated Package Diagram: spec 51-85094 – Changed revision from *D to *E.
*C	3006318	08/23/2010	Updated Electrical Characteristics: Updated Note 9 and referred the same note in I_{SB1} parameter. Updated Data Retention Characteristics: Added Note 12 and referred the same note in I_{CCDR} parameter. Updated Ordering Information: No change in part numbers. Added Ordering Code Definitions. Added Acronyms and Units of Measure. Updated to new template.
*D	3296704	06/29/2011	Updated Functional Description: Removed "For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines." at the end. Updated Ordering Information: No change in part numbers. Updated Ordering Code Definitions. Updated Package Diagram: spec 51-85094 – Changed revision from *E to *F.
*E	3515577	02/03/2012	Updated Switching Waveforms: Updated Figure 4. Updated Figure 5. Updated Figure 6. Updated Figure 7. Updated Figure 8. Completing Sunset Review.
*F	3548240	03/12/2012	Updated Electrical Characteristics: Updated Note 8 (Removed "Refer to AN13470 for details.").
*G	3897076	02/06/2013	Updated Switching Waveforms: Removed figure "Write Cycle No. 1 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)". Updated Figure 7 (Updated caption only). Completing Sunset Review.
*H	4039358	07/01/2013	Updated Functional Description: Updated description. Updated Electrical Characteristics: Added one more Test Condition "$4.5 \le V_{CC} \le 5.5$" for V_{OH} parameter and added maximum value corresponding to that Test Condition. Added Note 7 and referred the same note in maximum value for V_{OH} parameter corresponding to Test Condition "$4.5 \le V_{CC} \le 5.5$". Updated to new template.
*I	4099182	08/19/2013	Updated Switching Characteristics: Added Note 14 and referred the same note in "Parameter" column.

Document History Page (continued)

Document Title: CY62148ESL MoBL, 4-Mbit (512K × 8) Static RAM Document Number: 001-50045			
Rev.	**ECN**	**Submission Date**	**Description of Change**
*J	4779516	05/28/2015	Updated Functional Description: Added "For a complete list of related resources, click here." at the end. Updated AC Test Loads and Waveforms: Updated Figure 2. Updated Switching Characteristics: Added Note 19 and referred the same note in "Write Cycle". Updated Switching Waveforms: Added Figure 8. Added Note 29, 30, 31 and referred the same note in Figure 8. Updated Package Diagram: spec 51-85094 – Changed revision from *F to *G. Updated to new template.
*K	6906316	06/26/2020	Updated Features: Changed value of Typical standby current from 1 µA to 2.5 µA. Changed value of Typical active current from 2 mA to 3.5 mA. Updated Product Portfolio: Changed typical value of Operating I_{CC} from 2 mA to 3.5 mA corresponding to "f = 1 MHz". Changed maximum value of Operating I_{CC} from 2.5 mA to 6 mA corresponding to "f = 1 MHz". Changed typical value of Standby, I_{SB2} from 1 µA to 2.5 µA. Updated Electrical Characteristics: Changed typical value of I_{CC} parameter from 2 mA to 3.5 mA corresponding to Test Condition "f = 1 MHz". Changed maximum value of I_{CC} parameter from 2.5 mA to 6 mA corresponding to Test Condition "f = 1 MHz". Changed typical value of I_{SB1} parameter from 1 µA to 2.5 µA. Changed typical value of I_{SB2} parameter from 1 µA to 2.5 µA. Updated Data Retention Characteristics: Changed typical value of I_{CCDR} parameter from 1 µA to 3 µA. Changed maximum value of I_{CCDR} parameter from 7 µA to 8.8 µA. Updated to new template.

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Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

CY621472E30 MoBL

4-Mbit (256K × 16) Static RAM

Features

- Very high speed: 45 ns
- Temperature range
  - Industrial: –40 °C to +85 °C
- Wide voltage range: 2.20 V to 3.60 V
- Ultra low standby power
  - Typical standby current: 2.5 µA
  - Maximum standby current: 7 µA (Industrial)
- Ultra low active power
  - Typical active current: 3.5 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ Features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 44-pin thin small outline package (TSOP) II package
- Byte power down feature

Functional Description

The CY621472E30 is a high performance CMOS static RAM (SRAM) organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra low active current. It is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99 percent when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW or both $\overline{BLE}$ and $\overline{BHE}$ are HIGH). The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when:

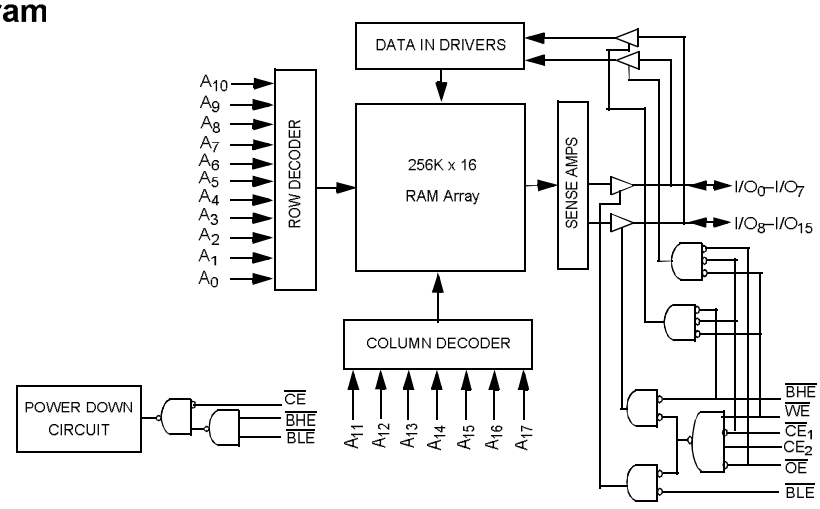
- Deselected ($\overline{CE}_1$ HIGH or CE_2 LOW)
- Outputs are disabled ($\overline{OE}$ HIGH)
- Both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH)
- Write operation is active ($\overline{CE}_1$ LOW and CE_2 HIGH and $\overline{WE}$ LOW)

To write to the device, take Chip Enable ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{17}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{17}).

To read from the device, take Chip Enable ($\overline{CE}_1$ LOW and CE_2 HIGH and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See the Truth Table on page 11 for a complete description of read and write modes.

For a complete list of related documentation, click here.

Logic Block Diagram



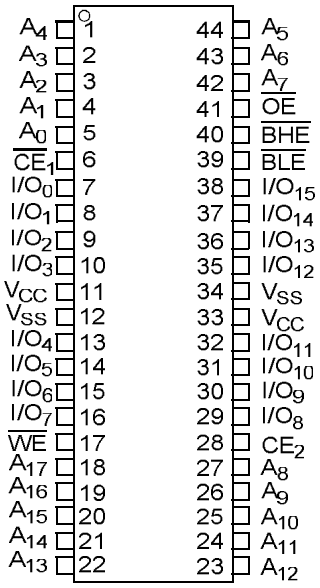
Contents

Product Portfolio

Product	Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
						f = 1 MHz		f = f_{max}			
		Min	Typ [1]	Max		Typ [1]	Max	Typ [1]	Max	Typ [1]	Max
CY621472E30LL	Industrial	2.2	3.0	3.6	45	3.5	6	15	20	2.5	7

Pin Configuration

Figure 1. 44-pin TSOP II pinout



Note
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential .....–0.3 V to +3.9 V (V_{CCmax} + 0.3 V)

DC Voltage Applied to Outputs in High Z State [2, 3] .....–0.3 V to 3.9 V (V_{CCmax} + 0.3 V)

DC input voltage [2, 3] .....–0.3 V to 3.9 V (V_{CCmax} + 0.3 V)

Output current into outputs (LOW) .....20 mA

Static discharge voltage (MIL-STD-883, Method 3015) ..... > 2001 V

Latch up current.....> 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC} [4]
CY621472E30LL	Industrial	–40 °C to +85 °C	2.2 V to 3.6 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		45 ns			Unit
				Min	Typ [5]	Max	
V_{OH}	Output HIGH voltage	I_{OH} = –0.1 mA		2.0	–	–	V
		I_{OH} = –1.0 mA, $V_{CC} \geq$ 2.70 V		2.4	–	–	V
V_{OL}	Output LOW voltage	I_{OL} = 0.1 mA		–	–	0.4	V
		I_{OL} = 2.1 mA, V_{CC} = 2.70 V		–	–	0.4	V
V_{IH}	Input HIGH voltage	V_{CC} = 2.2 V to 2.7 V		1.8	–	V_{CC} + 0.3	V
		V_{CC} = 2.7 V to 3.6 V		2.2	–	V_{CC} + 0.3	V
V_{IL}	Input LOW voltage	V_{CC} = 2.2 V to 2.7 V		–0.3	–	0.6	V
		V_{CC}= 2.7 V to 3.6 V		–0.3	–	0.8	V
I_{IX}	Input leakage current	GND $\leq V_I \leq V_{CC}$		–1	–	+1	µA
I_{OZ}	Output leakage current	GND $\leq V_O \leq V_{CC}$, Output Disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	f = f_{max} = $1/t_{RC}$	V_{CC} = $V_{CC(max)}$, I_{OUT} = 0 mA, CMOS levels	–	15	20	mA
		f = 1 MHz		–	3.5	6	
I_{SB1} [6]	Automatic CE power-down current – CMOS inputs	$\overline{CE_1} \geq V_{CC}$ – 0.2 V, $CE_2 \leq$ 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V, $V_{IN} \leq$ 0.2 V, f = f_{max} (address and data only), f = 0 ($\overline{OE}$, $\overline{BHE}$, $\overline{BLE}$ and $\overline{WE}$), V_{CC} = 3.60 V		–	2.5	7	µA
I_{SB2} [6]	Automatic CE Power down current – CMOS inputs	$\overline{CE_1} \geq V_{CC}$ – 0.2 V or $CE_2 \leq$ 0.2 V or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC}$ – 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V or $V_{IN} \leq$ 0.2 V, f = 0, V_{CC} = 3.60 V		–	2.5	7	µA

Notes

2. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
3. $V_{IH(max)}$ = V_{CC} + 0.75 V for pulse durations less than 20 ns.
4. Full device AC operation assumes a minimum of 100 µs ramp time from 0 to $V_{CC(min)}$ and 200 µs wait time after V_{CC} stabilization.
5. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
6. Chip enables ($\overline{CE_1}$ and CE_2) need to be tied to CMOS levels to meet the I_{SB1}/I_{SB2}/I_{CCDR} spec. Other inputs can be left floating.

Capacitance

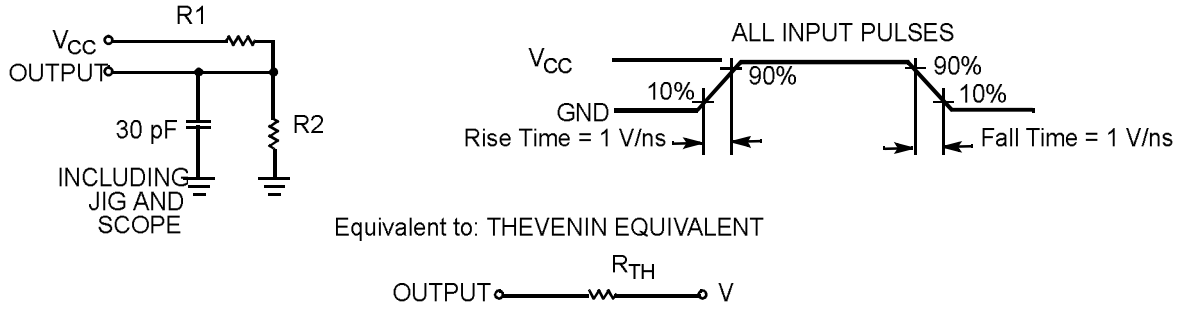
Parameter [7]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [7]	Description	Test Conditions	44-pin TSOP II Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	77	°C/W
Θ_{JC}	Thermal resistance (junction to case)		13	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameters	2.50 V	3.0 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Note
7. Tested initially and after any design or process changes that may affect these parameters.

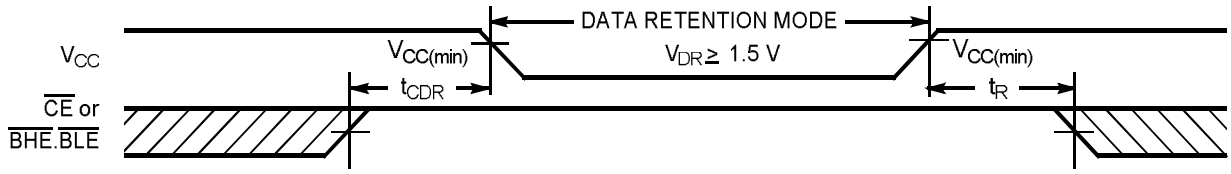
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ [8]	Max	Unit
V_{DR}	V_{CC} for data retention		1.5	–	–	V
I_{CCDR} [9]	Data retention current	V_{CC} = 1.5 V, $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	3	8.8	µA
t_{CDR} [10]	Chip deselect to data retention time		0	–	–	ns
t_R [11]	Operation recovery time		45	–	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform [12, 13]



Notes

8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
9. Chip enables ($\overline{CE}_1$ and CE_2) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
10. Tested initially and after any design or process changes that may affect these parameters.
11. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.
12. $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH.
13. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

Switching Characteristics

Over the Operating Range

Parameter [14]	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}_1$ LOW/CE_2 HIGH to data valid	–	45	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z [15]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [15, 16]	–	18	ns
t_{LZCE}	$\overline{CE}_1$ LOW/CE_2 HIGH to Low Z [15]	10	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH/CE_2 LOW to High Z [15, 16]	–	18	ns
t_{PU}	$\overline{CE}_1$ LOW/CE_2 HIGH to Power-up	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH/CE_2 LOW to Power-down	–	45	ns
t_{DBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to data valid	–	45	ns
t_{LZBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to Low Z [15, 17]	5	–	ns
t_{HZBE}	$\overline{BLE}$/$\overline{BHE}$ HIGH to High Z [15, 16]	–	18	ns
Write Cycle [18, 19]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	$\overline{CE}_1$ LOW/CE_2 HIGH to Write End	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	ns
t_{BW}	$\overline{BLE}$/$\overline{BHE}$ LOW to write end	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [15, 16]	–	18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [15]	10	–	ns

Notes

14. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1 V/ns) or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the Figure 2 on page 5.
15. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
16. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
17. If both byte enables are together, this value is 10 ns.
18. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$, or both = V_{IL}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
19. The minimum write cycle pulse width for WRITE Cycle 4 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [20, 21]

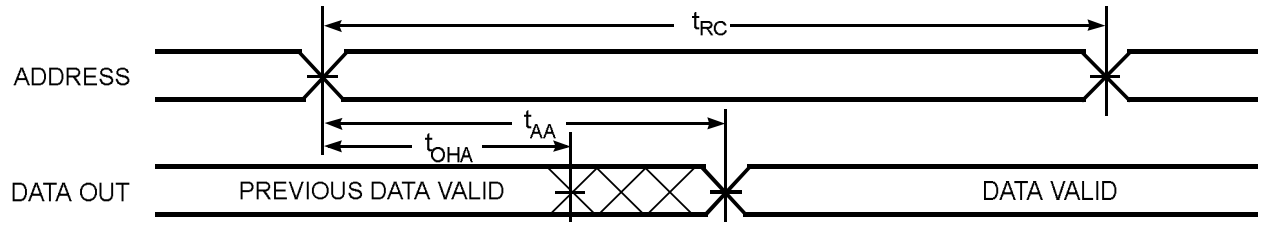
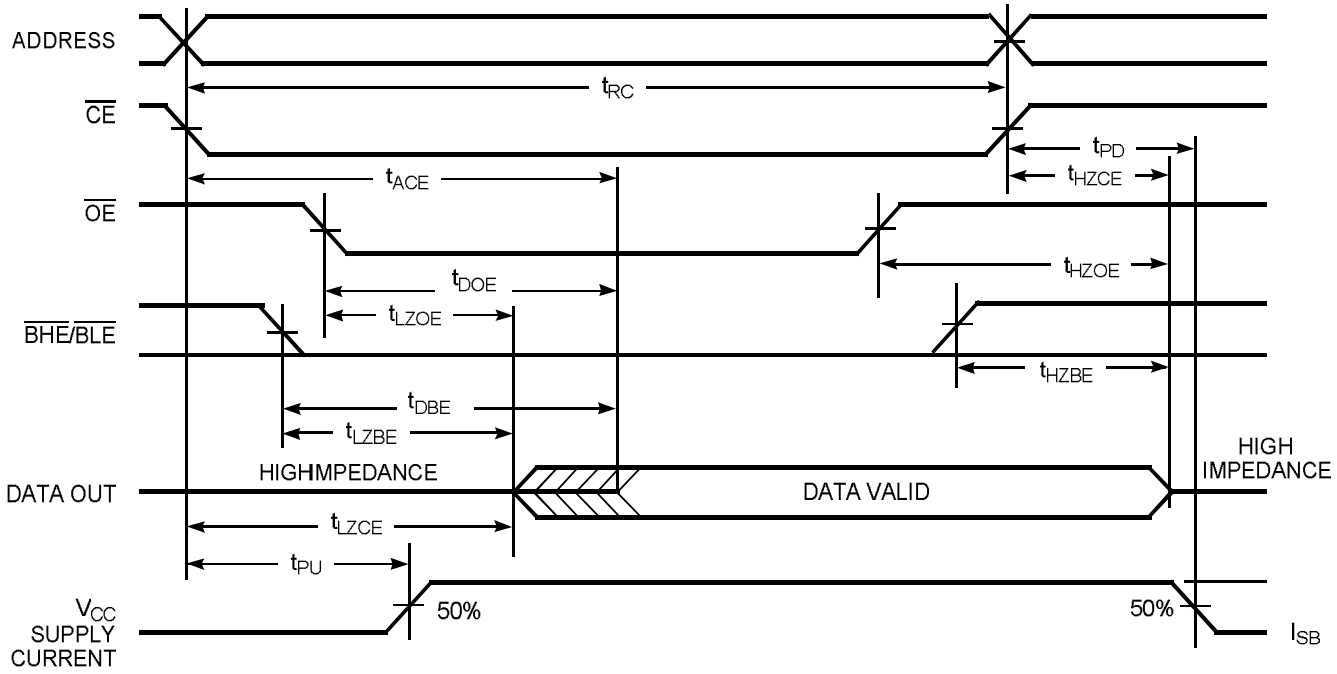


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [21, 22, 23]



Notes
20. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$, or both = V_{IL}.
21. $\overline{WE}$ is HIGH for read cycle.
22. $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH.
23. Address valid before or similar to $\overline{CE}$ and $\overline{BHE}$, $\overline{BLE}$ transition LOW.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ($\overline{WE}$ Controlled) [24, 25, 26, 27]

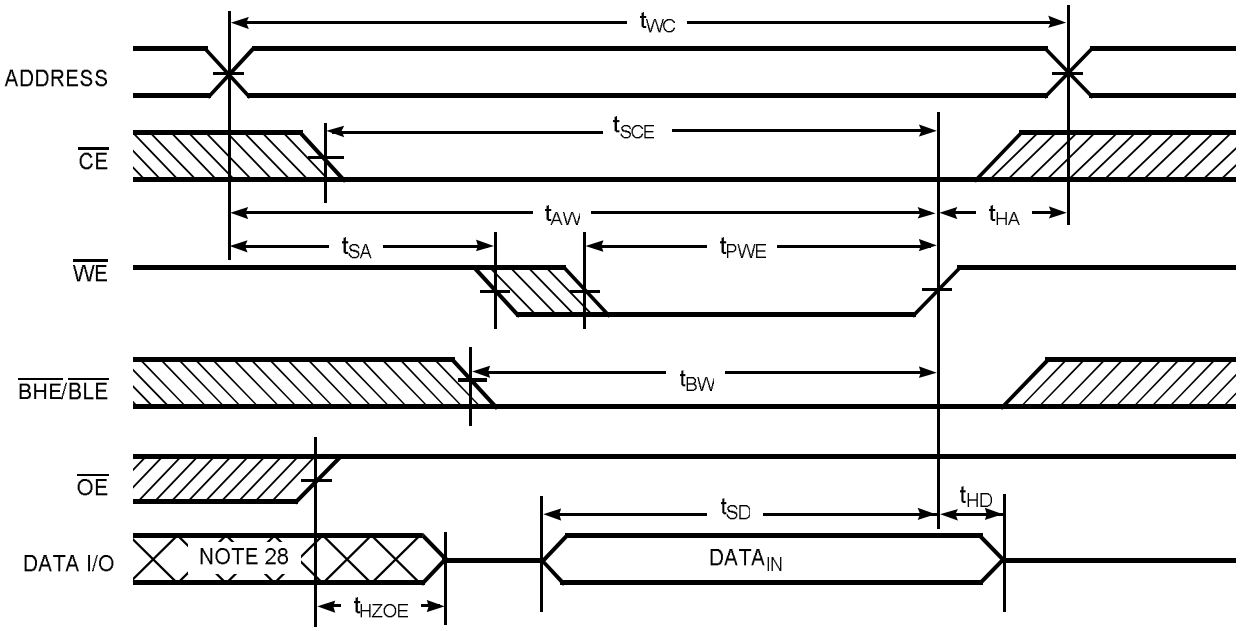
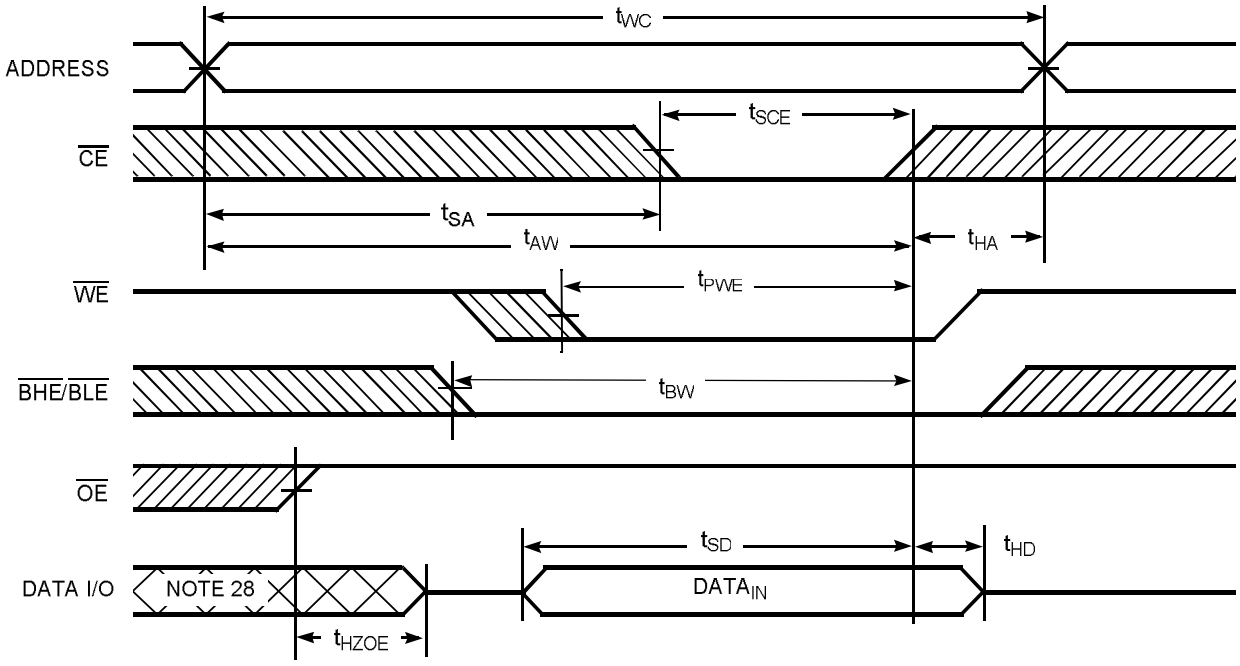


Figure 7. Write Cycle No. 2 ($\overline{CE}$ Controlled) [24, 25, 26, 27]



Notes

24. $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH.
25. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$, or both = V_{IL}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
26. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
27. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
28. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [29, 30, 31]

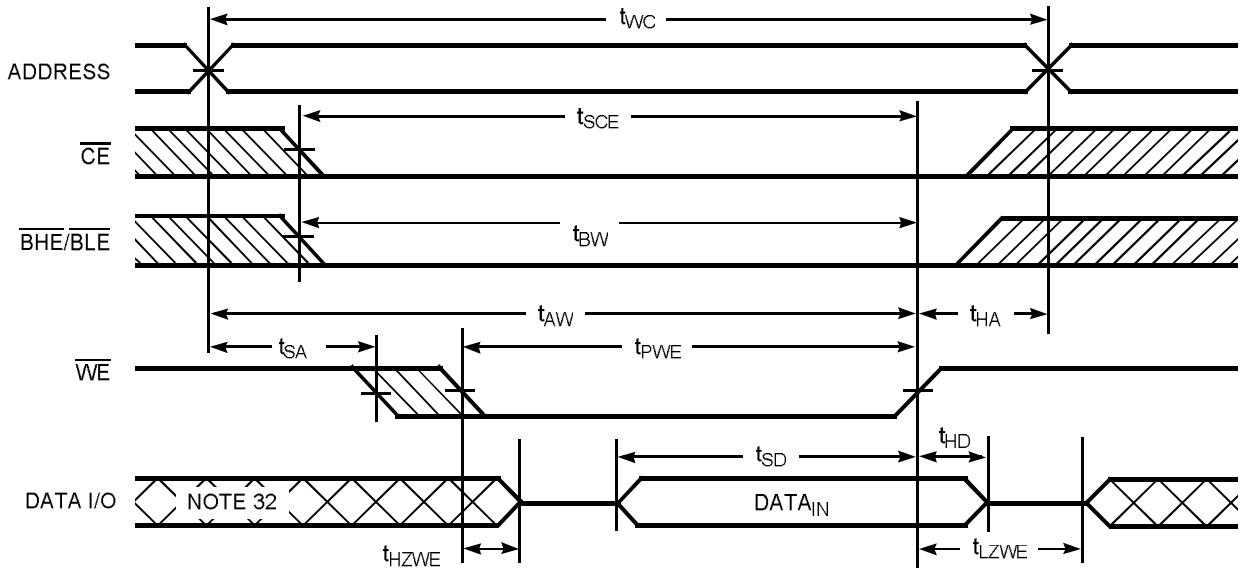
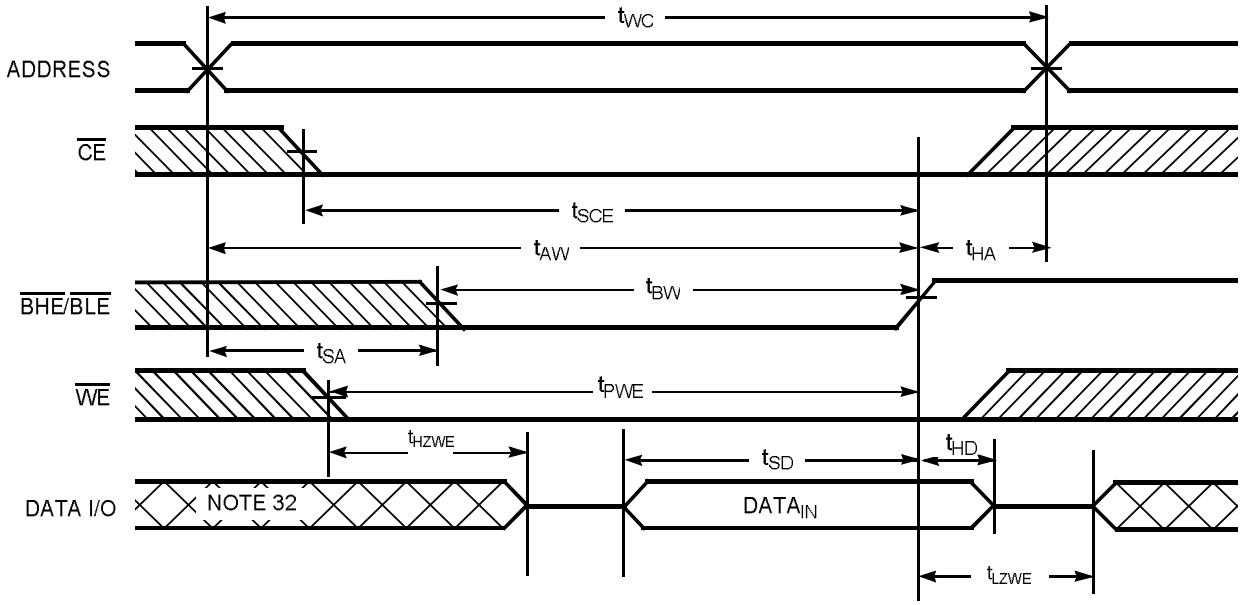


Figure 9. Write Cycle No. 4 ($\overline{BHE}/\overline{BLE}$ Controlled, $\overline{OE}$ LOW) [29, 30]



Notes

29. $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH.
30. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
31. The minimum write cycle pulse width should be equal to the sum of t_{HZWE} and t_{SD}.
32. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

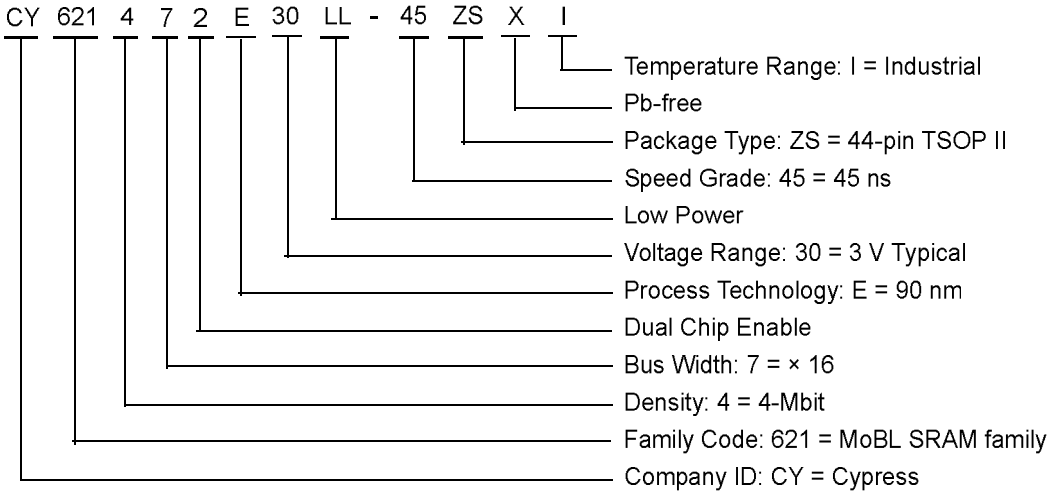
$\overline{CE1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	I/Os	Mode	Power
H	X[33]	X	X	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
X[33]	L	X	X	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
X[33]	X[33]	X	X	H	H	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	H	L	L	L	Data out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	Data out (I/O_0–I/O_7); I/O_8–I/O_{15} in High Z	Read	Active (I_{CC})
L	H	H	L	L	H	Data out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	H	L	L	High Z	Output disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output disabled	Active (I_{CC})
L	H	H	H	L	H	High Z	Output disabled	Active (I_{CC})
L	H	L	X	L	L	Data in (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	Data in (I/O_0–I/O_7); I/O_8–I/O_{15} in High Z	Write	Active (I_{CC})
L	H	L	X	L	H	Data in (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Write	Active (I_{CC})

Note
33. The 'X' (Don't care) state for the chip enables ($\overline{CE}_1$ and CE_2) in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

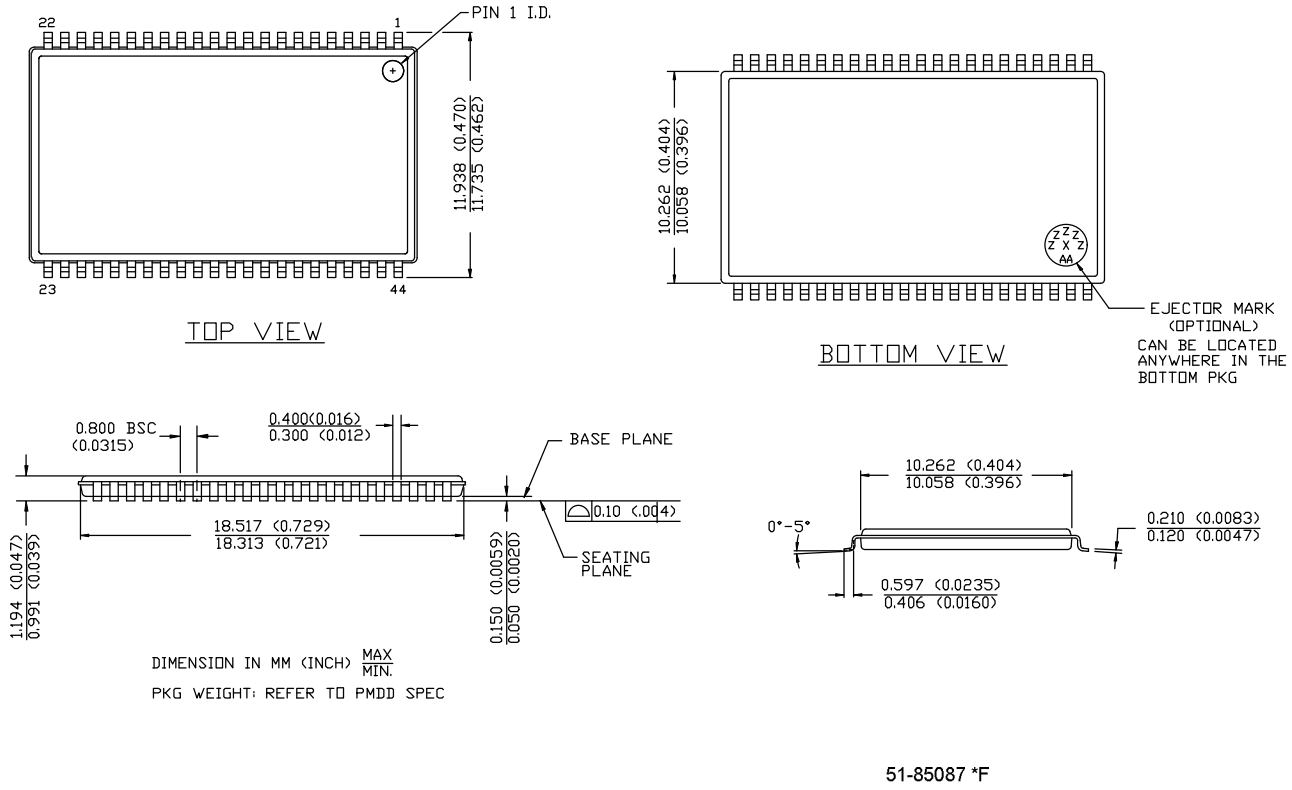
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY621472E30LL-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	Industrial

Ordering Code Definitions



Package Diagram

Figure 10. 44-pin TSOP II (18.4 × 10.2 × 1.194 mm) Package Outline, 51-85087



51-85087 *F

Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY621472E30 MoBL, 4-Mbit (256K × 16) Static RAM Document Number: 001-67798			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
**	3184883	03/01/2011	New data sheet.
*A	3223503	04/15/2011	Updated Truth Table: Removed overline bar for CE_2 in column heading. Updated to new template.
*B	3261142	05/19/2011	Updated Switching Characteristics: Changed minimum value of t_{LZBE} parameter from 10 ns to 5 ns. Added Ordering Information and Ordering Code Definitions. Added Acronyms and Units of Measure.
*C	3365953	09/08/2011	Changed status from Preliminary to Final. Updated Package Diagram: spec 51-85087 – Changed revision from *C to *D.
*D	3414567	10/20/2011	Replaced CY62147EV30 with CY621472E30 in all instances across the document.
*E	4331825	04/03/2014	Updated Switching Characteristics: Added Note 19 and referred the same note in “Write Cycle”. Updated Switching Waveforms: Added Note 31 and referred the same note in Figure 8. Updated Package Diagram: spec 51-85087 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.
*F	4573121	11/18/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*G	6906316	06/26/2020	Updated Features: Changed value of Typical standby current from 1 µA to 2.5 µA. Changed value of Typical active current from 2 mA to 3.5 mA. Updated Product Portfolio: Changed typical value of Operating I_{CC} from 2 mA to 3.5 mA corresponding to “f = 1 MHz”. Changed maximum value of Operating I_{CC} from 2.5 mA to 6 mA corresponding to “f = 1 MHz”. Changed typical value of Standby, I_{SB2} from 1 µA to 2.5 µA. Updated Electrical Characteristics: Changed typical value of I_{CC} parameter from 2 mA to 3.5 mA corresponding to Test Condition “f = 1 MHz”. Changed maximum value of I_{CC} parameter from 2.5 mA to 6 mA corresponding to Test Condition “f = 1 MHz”. Changed typical value of I_{SB1} parameter from 1 µA to 2.5 µA. Changed typical value of I_{SB2} parameter from 1 µA to 2.5 µA. Updated Data Retention Characteristics: Changed typical value of I_{CCDR} parameter from 0.8 µA to 3 µA. Changed maximum value of I_{CCDR} parameter from 7 µA to 8.8 µA. Updated Package Diagram: spec 51-85087 – Changed revision from *E to *F. Updated to new template.

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CY62148E MoBL

4-Mbit (512K × 8) Static RAM

Features

- Very high speed: 45 ns
- Voltage range: 4.5 V to 5.5 V
- Pin compatible with CY62148B
- Ultra low standby power
  - Typical standby current: 2.5 µA
  - Maximum standby current: 7 µA (Industrial)
- Ultra low active power
  - Typical active current: 3.5 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}$, and $\overline{OE}$ features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 32-pin thin small outline package (TSOP) II and 32-pin small-outline integrated circuit (SOIC)[1] packages

Functional Description

The CY62148E is a high performance CMOS static RAM organized as 512K words by 8-bits. This device features advanced circuit design to provide ultra low standby current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications. The device also has an automatic power-down feature that significantly reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected ($\overline{CE}$ HIGH). The eight input and output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), Outputs are disabled ($\overline{OE}$ HIGH), or during an active Write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

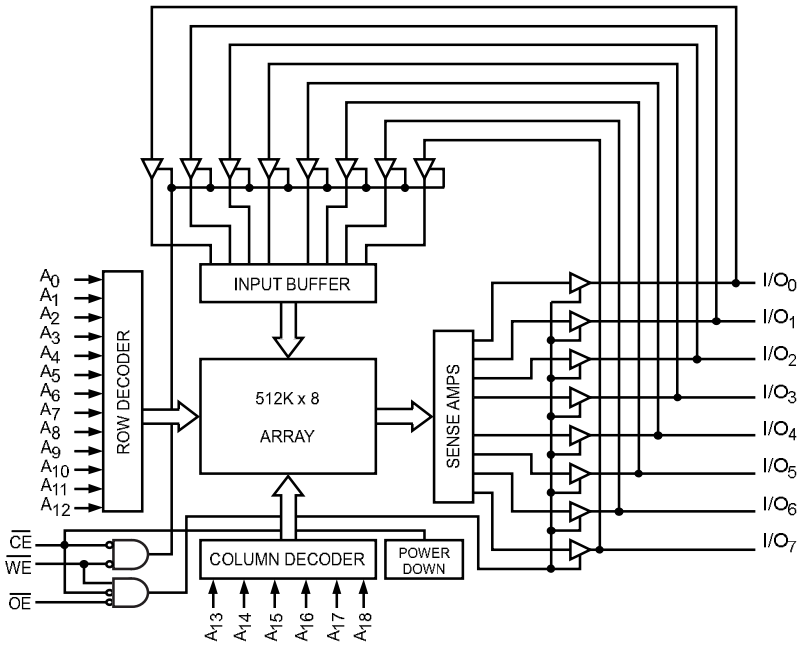
To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

The CY62148E device is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please see Electrical Characteristics on page 4 for more details and suggested alternatives.

For a complete list of related documentation, click here.

Logic Block Diagram



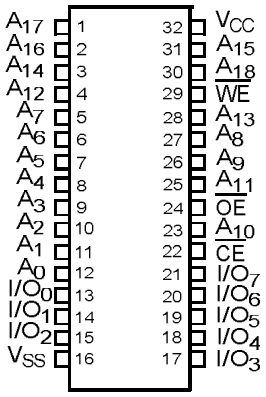
Note
1. SOIC package is available only in 55 ns speed bin.

Contents

Pin Configurations

Figure 1. 32-pin SOIC/TSOP II pinout [2]

Top View



Product Portfolio

Product		Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
							Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
							f = 1 MHz		f = f_{max}			
			Min	Typ [3]	Max		Typ [3]	Max	Typ [3]	Max	Typ [3]	Max
CY62148ELL	TSOP II	Industrial	4.5	5.0	5.5	45	3.5	6	15	20	2.5	7
CY62148ELL	SOIC	Industrial/ Automotive-A	4.5	5.0	5.5	55	3.5	6	15	20	2.5	7

Notes
2. SOIC package is available only in 55 ns speed bin.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential ..... –0.5 V to 6.0 V (V_{CCmax} + 0.5 V)

DC voltage applied to outputs in high Z state [4, 5] ..... –0.5 V to 6.0 V (V_{CCmax} + 0.5 V)

DC input voltage [4, 5] ..... –0.5 V to 6.0 V (V_{CCmax} + 0.5 V)

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC} [6]
CY62148E	Industrial/ Automotive-A	–40 °C to +85 °C	4.5 V to 5.5 V

Electrical Characteristics

Over the operating range

Parameter	Description	Test Conditions		45 ns			55 ns [7]			Unit
				Min	Typ [8]	Max	Min	Typ [8]	Max	
V_{OH} [9]	Output HIGH voltage	V_{CC} = 4.5 V, I_{OH} = –1 mA		2.4	–	–	2.4	–	–	V
		V_{CC} = 5.5 V, I_{OH} = –0.1 mA		–	–	3.4 [8]	–	–	3.4 [8]	V
V_{OL}	Output LOW voltage	I_{OL} = 2.1 mA		–	–	0.4	–	–	0.4	V
V_{IH}	Input HIGH voltage	V_{CC} = 4.5 V to 5.5 V		2.2	–	V_{CC} + 0.5	2.2	–	V_{CC} + 0.5	V
V_{IL}	Input LOW voltage	V_{CC} = 4.5 V to 5.5 V	For TSOPII package	–0.5	–	0.8	–	–	–	V
			For SOIC package	–	–	–	–0.5	–	0.6 [10]	
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–1	–	+1	–1	–	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, output disabled		–1	–	+1	–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	f = f_{max} = 1/t_{RC}	V_{CC} = $V_{CC(max)}$, I_{OUT} = 0 mA CMOS levels	–	15	20	–	15	20	mA
		f = 1 MHz		–	3.5	6	–	3.5	6	
I_{SB2} [11]	Automatic $\overline{CE}$ power-down current – CMOS inputs	$\overline{CE}$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0, V_{CC} = $V_{CC(max)}$		–	2.5	7	–	2.5	7	µA

Notes

4. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns for I ≤ 30 mA.
5. $V_{IH(max)}$ = V_{CC} + 0.75 V for pulse durations less than 20 ns.
6. Full device AC operation assumes a minimum of 100 µs ramp time from 0 to $V_{CC(min)}$ and 200 µs wait time after V_{CC} stabilization.
7. SOIC package is available only in 55 ns speed bin.
8. Typical values are included for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
9. Please note that the maximum V_{OH} limit for this device does not exceed minimum CMOS V_{IH} of 3.5V. If you are interfacing this SRAM with 5 V legacy processors that require a minimum V_{IH} of 3.5 V, please refer to Application Note AN6081 for technical details and options you may consider.
10. Under DC conditions the device meets a V_{IL} of 0.8 V. However, in dynamic conditions Input LOW Voltage applied to the device must not be higher than 0.6 V. This is applicable to SOIC package only.
11. Chip enable ($\overline{CE}$) must be HIGH at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

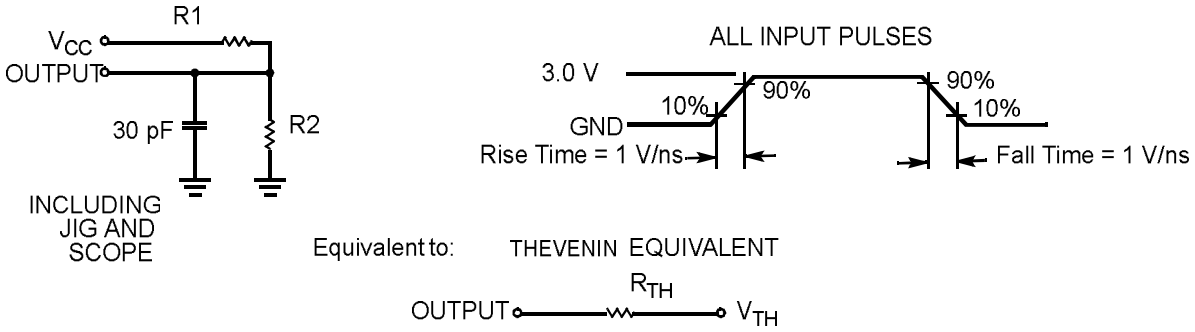
Parameter [12]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(Typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [12]	Description	Test Conditions	32-pin SOIC Package	32-pin TSOP II Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	51.57	59.10	°C/W
Θ_{JC}	Thermal resistance (junction to case)		25.01	12.19	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameter [12]	5.0 V	Unit
R1	1800	Ω
R2	990	Ω
R_{TH}	639	Ω
V_{TH}	1.77	V

Note
12. Tested initially and after any design or process changes that may affect these parameters.

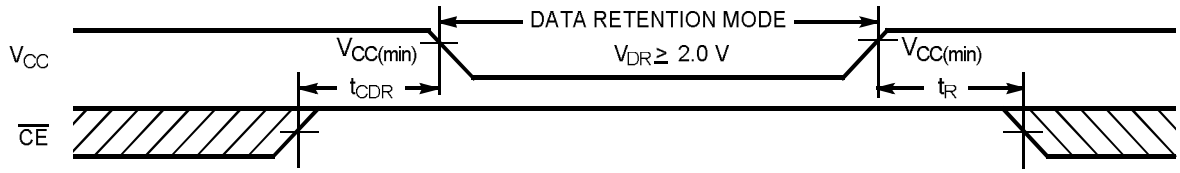
Data Retention Characteristics

Over the operating range

Parameter	Description	Conditions		Min	Typ [13]	Max	Unit
V_{DR}	V_{CC} for data retention			2	–	–	V
I_{CCDR}[14]	Data retention current	$V_{CC} = V_{DR}$, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	Industrial/ Automotive-A	–	3	8.8	µA
t_{CDR}	Chip deselect to data retention time			0	–	–	ns
t_R[15]	Operation recovery time			45/55	–	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes
13. Typical values are included for reference and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.
14. Chip enable ($\overline{CE}$) must be HIGH at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
15. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)}$ > 100 µs or stable at $V_{CC(min)}$ > 100 µs.

Switching Characteristics

Over the operating range

Parameter [16, 17]	Description	45 ns		55 ns [18]		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	45	–	55	–	ns
t_{AA}	Address to data valid	–	45	–	55	ns
t_{OHA}	Data hold from address change	10	–	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	45	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	–	25	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z [19]	5	–	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z [19, 20]	–	18	–	20	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z [19]	10	–	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z [19, 20]	–	18	–	20	ns
t_{PU}	$\overline{CE}$ LOW to power-up	0	–	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down	–	45	–	55	ns
Write Cycle [21, 22]						
t_{WC}	Write cycle time	45	–	55	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	35	–	40	–	ns
t_{AW}	Address setup to write end	35	–	40	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	40	–	ns
t_{SD}	Data setup to write end	25	–	25	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z [19, 20]	–	18	–	20	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z [19]	10	–	10	–	ns

Notes

16. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the chip enable signal as described in the Application Note AN66311. However, the issue has been fixed and in production now, and hence, this Application Notes is no longer applicable. It is available for download on our website as it contains information on the date code of the parts, beyond which the fix has been in production.
17. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3 V, and output loading of the specified I_{OL}/I_{OH} as shown in the Figure 2 on page 5.
18. SOIC package is available only in 55 ns speed bin.
19. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
20. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
21. The internal wre.ite time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
22. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [23, 24]

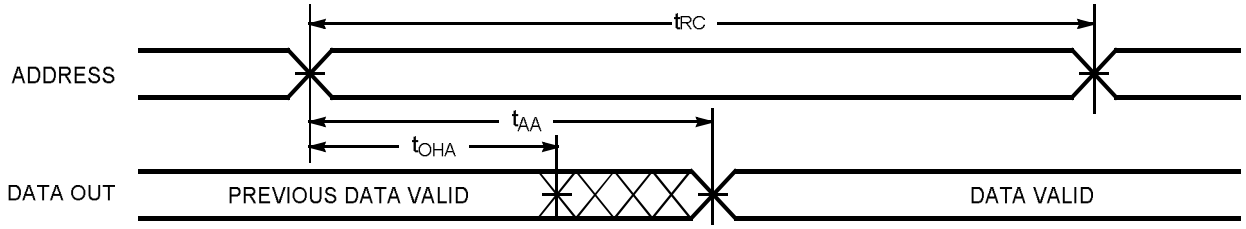


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [24, 25]

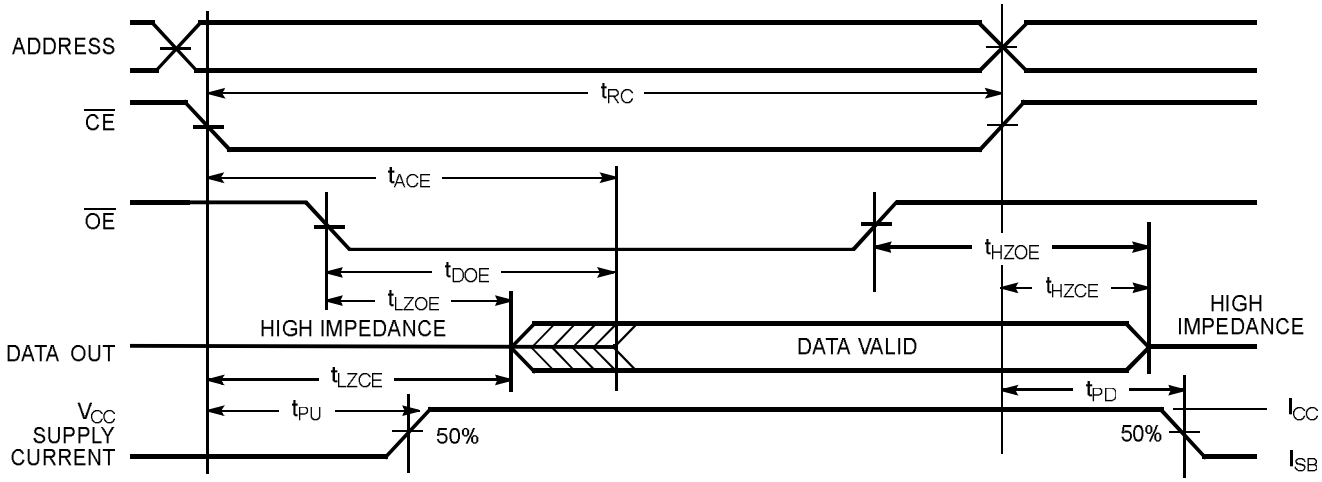
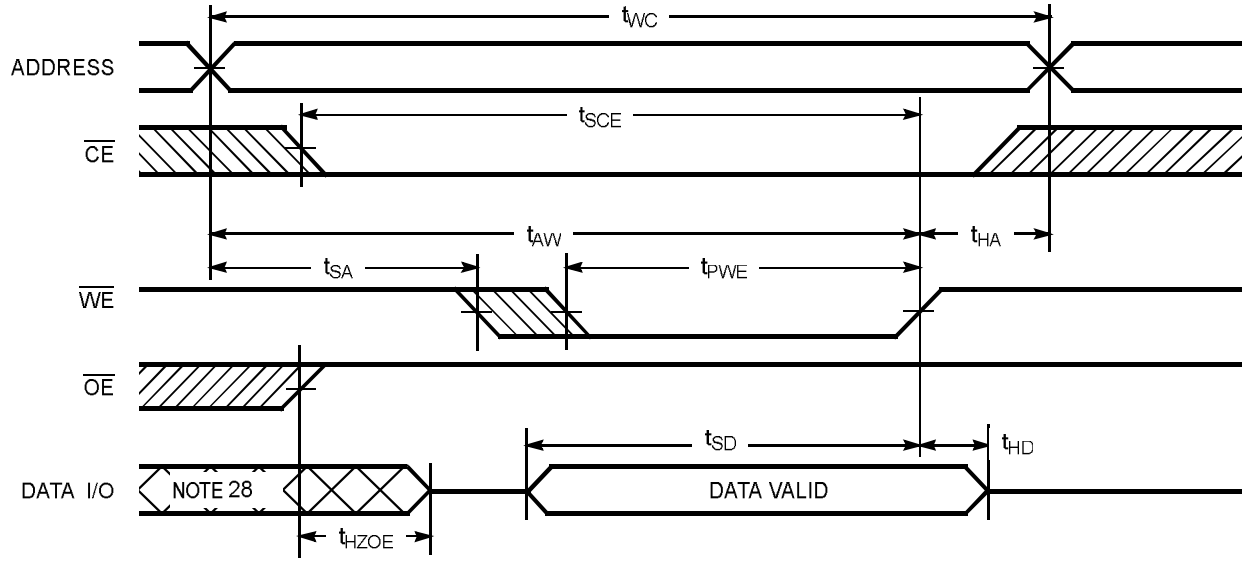


Figure 6. Write Cycle No. 1 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write) [26, 27]



Notes
23. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
24. $\overline{WE}$ is HIGH for read cycles.
25. Address valid before or similar to $\overline{CE}$ transition LOW.
26. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
27. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
28. During this period, the I/Os are in output state and input signals must not be applied.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 2 ($\overline{CE}$ Controlled) [29, 30]

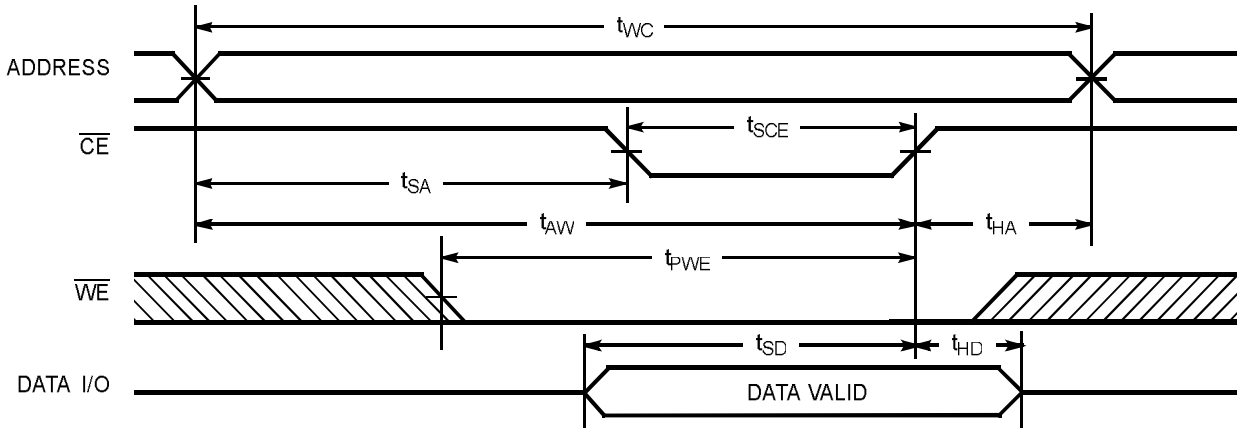
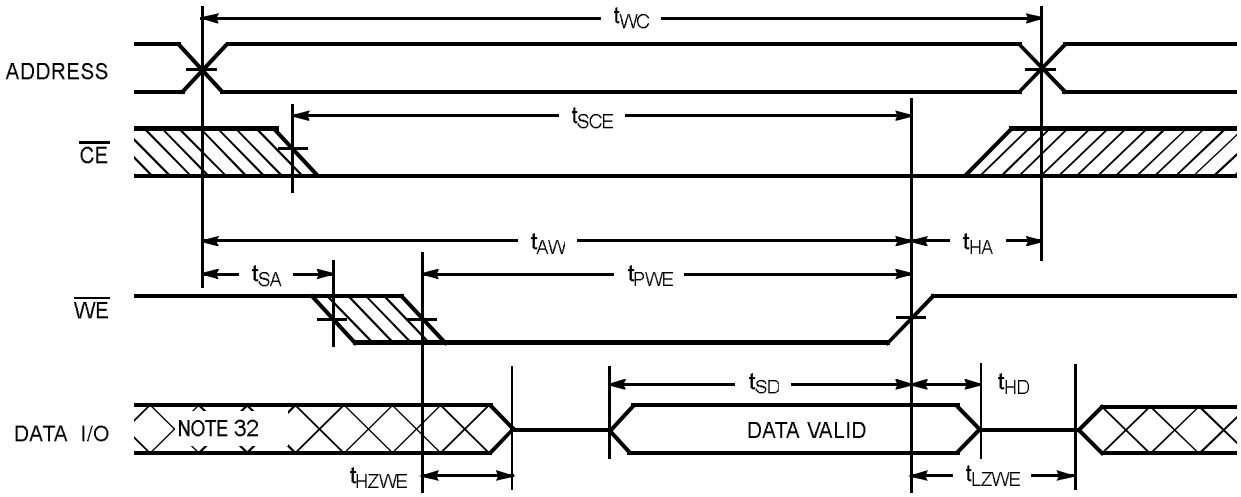


Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [30, 31]



Notes
29. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
30. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
31. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE}.
32. During this period, the I/Os are in output state and input signals must not be applied.

Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Mode	Power
H [33]	X	X	High Z	Deselect/power-down	Standby (I_{SB})
L	H	L	Data out	Read	Active (I_{CC})
L	L	X	Data in	Write	Active (I_{CC})
L	H	H	High Z	Selected, outputs disabled	Active (I_{CC})

Note
33. Chip enable ($\overline{CE}$) must be HIGH at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Ordering Information

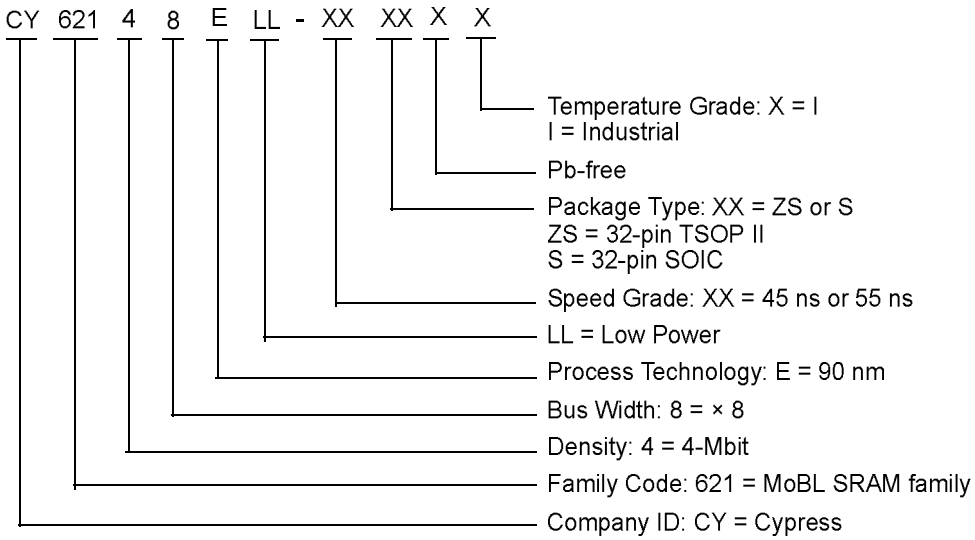
Table 1 lists the CY62148E MoBL key package features and ordering codes. The table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products.

Table 1. Key features and Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62148ELL-45ZSXI	51-85095	32-pin TSOP II (Pb-free)	Industrial
55	CY62148ELL-55SXI	51-85081	32-pin SOIC (Pb-free)	Industrial

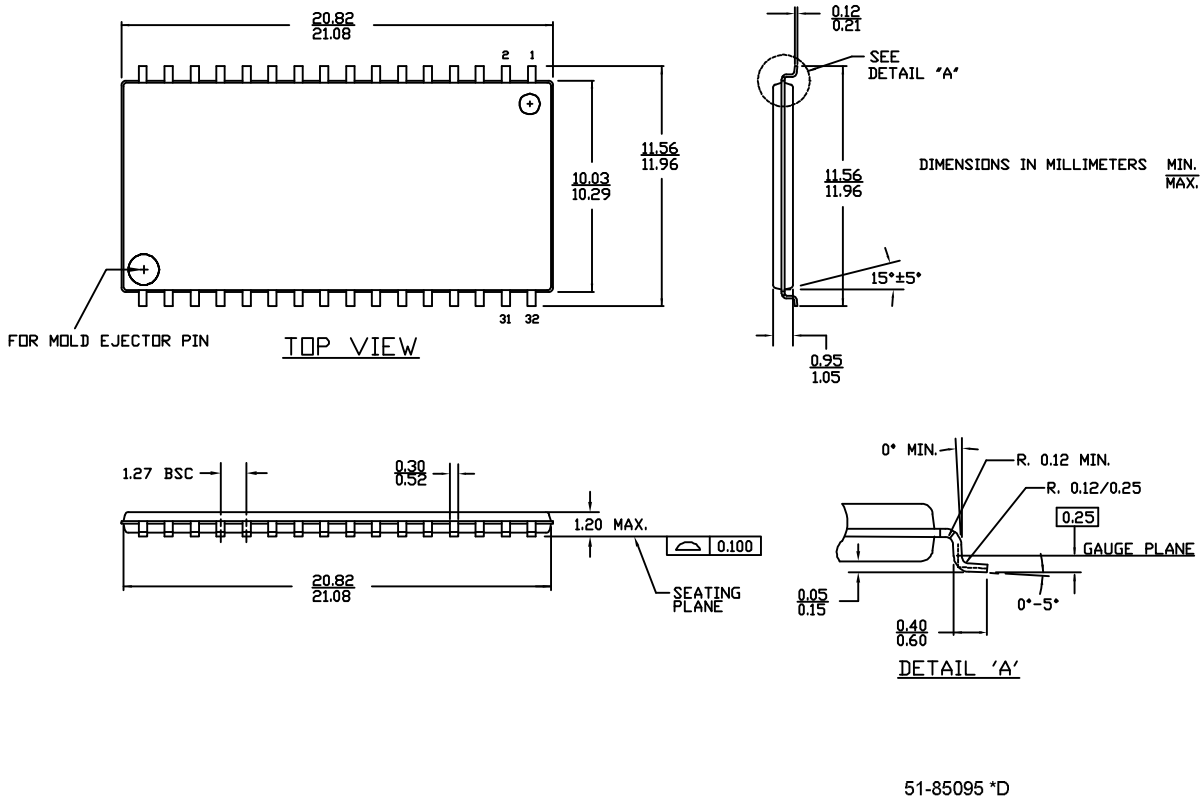
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



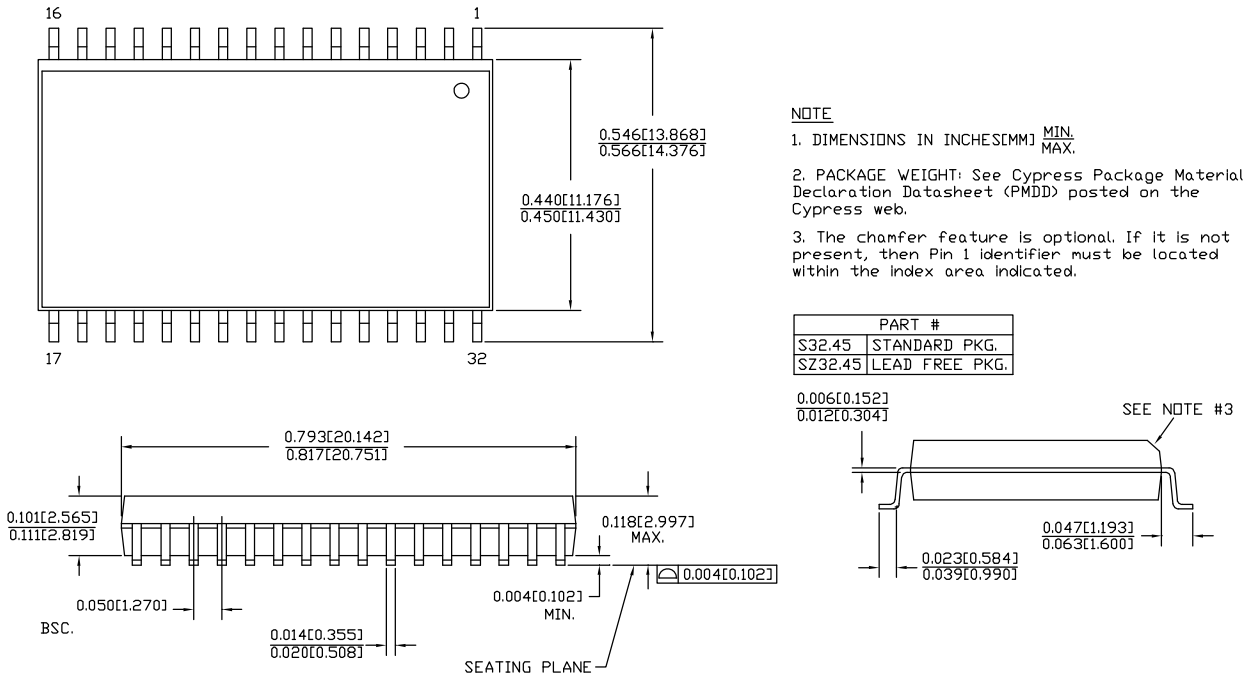
Package Diagrams

Figure 9. 32-pin TSOP II (20.95 × 11.76 × 1.0 mm) Package Outline, 51-85095



Package Diagrams (continued)

Figure 10. 32-pin SOIC (450 Mils) Package Outline, 51-85081



Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
MoBL	More Battery Life
SOIC	Small Outline Integrated Circuit
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62148E MoBL, 4-Mbit (512K × 8) Static RAM Document Number: 38-05442			
Revision	**ECN**	**Submission Date**	**Description of Change**
**	201580	01/08/2004	New data sheet.
*A	249276	08/03/2004	Changed status from Advance Information to Preliminary. Updated Features: Added RTSOP II Package related information. Removed FBGA Package related information. Updated Functional Description: Added RTSOP II package related information. Removed FBGA Package related information. Updated Pin Configurations: Added RTSOP II package related information. Removed FBGA Package related information. Updated Operating Range: Updated Note 6 (Changed V_{CC} stabilization time from 100 µs to 200 µs). Updated Data Retention Characteristics: Changed maximum value of I_{CCDR} parameter from 2.0 µA to 2.5 µA. Changed minimum value of t_R parameter from 100 µs to t_{RC} ns. Updated Switching Characteristics: Changed minimum value of t_{OHA} parameter from 6 ns to 10 ns corresponding to both 35 ns and 45 ns speed bins. Changed maximum value of t_{DOE} parameter from 15 ns to 18 ns corresponding to 35 ns speed bin. Changed maximum value of t_{HZOE}, t_{HZWE} parameters from 12 ns to 15 ns corresponding to 35 ns speed bin and 15 ns to 18 ns corresponding to 45 ns speed bin. Changed minimum value of t_{SCE} parameter from 25 ns to 30 ns corresponding to 35 ns speed bin and 40 ns to 35 ns corresponding to 45 ns speed bin. Changed maximum value of t_{HZCE} parameter from 12 ns to18 ns corresponding to 35 ns speed bin and 15 ns to 22 ns corresponding to 45 ns speed bin. Changed minimum value of t_{SD} parameter from 15 ns to 18 ns corresponding to 35 ns speed bin and 20 ns to 22 ns corresponding to 45 ns speed bin. Updated Ordering Information: Corrected typo in Package Name column. Updated part numbers.
*B	414820	12/16/2005	Changed status from Preliminary to Final. Changed the address of Cypress Semiconductor Corporation on Page 1 from “3901 North First Street” to “198 Champion Court”. Updated Features: Removed 35 ns speed bin. Updated Pin Configurations: Removed Note “DNU pins have to be left floating or tied to V_{SS} to ensure proper application.” and its reference. Updated Product Portfolio: Removed 35 ns speed bin. Updated Maximum Ratings: Updated Note 4 (to include current limit).

Document History Page (continued)

Document Title: CY62148E MoBL, 4-Mbit (512K × 8) Static RAM Document Number: 38-05442			
Revision	**ECN**	**Submission Date**	**Description of Change**
*B (cont.)	414820	12/16/2005	Updated Electrical Characteristics: Removed "L" version of CY62148E. Changed typical value of I_{CC} parameter from 1.5 mA to 2 mA corresponding to Test Condition "f = 1 MHz". Changed maximum value of I_{CC} parameter from 2 mA to 2.5 mA corresponding to Test Condition "f = 1 MHz". changed typical value of I_{CC} parameter from 12 mA to 15 mA corresponding to Test Condition "f = f_{max}". Removed I_{SB1} parameter and its corresponding details. Changed typical value of I_{SB2} parameter from 0.7 µA to 1 µA. Changed maximum value of I_{SB2} parameter from 2.5 µA to 7 µA. Updated AC Test Loads and Waveforms: Changed the AC test load capacitance from 100 pF to 30 pF in Figure 2. Changed test load parameters R_1, R_2, R_{TH} and V_{TH} from 1838 Ω, 994 Ω, 645 Ω and 1.75 V to 1800 Ω, 990 Ω, 639 Ω and 1.77 V. Updated Data Retention Characteristics: Changed maximum value of I_{CCDR} parameter from 2.5 µA to 7 µA. Added typical value for I_{CCDR} parameter. Updated Switching Characteristics: Removed 35 ns speed bin. Changed minimum value of t_{LZOE} parameter from 3 ns to 5 ns. Changed minimum value of t_{LZCE} and t_{LZWE} parameters from 6 ns to 10 ns. Changed maximum value of t_{HZCE} parameter from 22 ns to 18 ns. Changed minimum value of t_{PWE} parameter from 30 ns to 35 ns. Changed minimum value of t_{SD} parameter from 22 ns to 25 ns. Updated Ordering Information: Updated part numbers. Removed "Package Name" column. Added "Package Diagram" column. Updated to new template.
*C	464503	05/25/2006	Updated Product Portfolio (Included Automotive Range). Updated Operating Range (Included Automotive Range). Updated Electrical Characteristics (Included Automotive Range). Updated Data Retention Characteristics (Included Automotive Range). Updated Switching Characteristics (Included Automotive Range). Updated Ordering Information: Updated part numbers.
*D	485639	07/21/2006	Updated Operating Range: Replaced "2.2 V to 3.6 V" with "4.5 V to 5.5 V" in "V_{CC}" column.
*E	833080	03/09/2007	Updated Electrical Characteristics: Added SOIC package in "Test Conditions" of V_{IL} parameter and also added corresponding values. Added Note 10 and referred the same note in maximum value of V_{IL} parameter corresponding to SOIC package.

Document History Page (continued)

Document Title: CY62148E MoBL, 4-Mbit (512K × 8) Static RAM Document Number: 38-05442			
Revision	**ECN**	**Submission Date**	**Description of Change**
*F	890962	03/09/2007	Updated Pin Configurations: Added Note 2 and referred the same note in Figure 1. Updated Product Portfolio: Included Automotive-A range and removed Automotive-E range. Updated Operating Range: Included Automotive-A range and removed Automotive-E range. Updated Electrical Characteristics: Included Automotive-A range and removed Automotive-E range. Added Note 11 (related to I_{SB2}) and referred the same note in I_{SB2} parameter. Updated Data Retention Characteristics: Included Automotive-A range and removed Automotive-E range. Updated Switching Characteristics: Included Automotive-A range and removed Automotive-E range. Updated Ordering Information: Updated part numbers.
*G	2947039	06/10/2010	Updated Truth Table: Added Note 33 and referred the same note in "$\overline{CE}$" column. Updated Ordering Information: Updated part numbers. Updated Package Diagrams: spec 51-85095 – Changed revision from ** to *A. spec 51-85081 – Changed revision from *B to *C. Updated to new template.
*H	3006318	08/23/2010	Updated Data Retention Characteristics: Added Note 14 and referred the same note in I_{CCDR} parameter. Updated Ordering Information: No change in part numbers. Added Ordering Code Definitions. Added Acronyms and Units of Measure. Updated to new template.
*I	3235744	04/20/2011	Updated Functional Description: Removed "For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines." at the end. Updated Package Diagrams: spec 51-85095 – Changed revision from *A to *B. Completing Sunset Review.
*J	3302815	07/14/2011	Updated to new template.
*K	3539544	03/01/2012	Updated Electrical Characteristics: Updated Note 10. Updated Package Diagrams: spec 51-85081 – Changed revision from *C to *D. Completing Sunset Review.
*L	3992135	05/06/2013	Updated Functional Description: Updated description. Updated Electrical Characteristics: Added one more Test Condition "V_{CC} = 5.5 V, I_{OH} = –0.1 mA" for V_{OH} parameter and also added corresponding values. Updated Package Diagrams: spec 51-85081 – Changed revision from *D to *E. Completing Sunset Review.

Document History Page (continued)

Document Title: CY62148E MoBL, 4-Mbit (512K × 8) Static RAM Document Number: 38-05442			
Revision	**ECN**	**Submission Date**	**Description of Change**
*M	4099045	08/19/2013	Updated Switching Characteristics: Added Note 16 and referred the same note in “Parameter” column. Updated to new template.
*N	4576526	11/21/2014	Updated Features: Added “For a complete list of related documentation, click here.” at the end. Updated Switching Characteristics: Added Note 22 and referred the same note in “Write Cycle”. Updated Switching Waveforms: Added Note 31 and referred the same note in Figure 8.
*O	4794169	06/11/2015	Updated Package Diagrams: spec 51-85095 – Changed revision from *B to *D. Updated to new template.
*P	5285890	06/01/2016	Updated Thermal Resistance: Replaced “two-layer” with “four-layer” in “Test Conditions” column. Updated all values in “32-pin SOIC Package” and “32-pin TSOP II Package” columns. Updated Data Retention Characteristics: Removed details in “Conditions” column corresponding to t_R parameter (To match the speed grade). Updated to new template. Completing Sunset Review.
*Q	6072272	02/15/2018	Updated Ordering Information: Updated part numbers. Updated to new template.
*R	6533264	04/04/2019	Updated to new template. Completing Sunset Review.
*S	6906316	06/26/2020	Updated Features: Changed value of Typical standby current from 1 µA to 2.5 µA. Changed value of Typical active current from 2 mA to 3.5 mA. Updated Product Portfolio: Changed typical value of Operating I_{CC} from 2 mA to 3.5 mA corresponding to all packages and “f = 1 MHz”. Changed maximum value of Operating I_{CC} from 2.5 mA to 6 mA corresponding to all packages and “f = 1 MHz”. Changed typical value of Standby, I_{SB2} from 1 µA to 2.5 µA corresponding to all packages. Updated Electrical Characteristics: Changed typical value of I_{CC} parameter from 2 mA to 3.5 mA corresponding to all speed bins and Test Condition “f = 1 MHz”. Changed maximum value of I_{CC} parameter from 2.5 mA to 6 mA corresponding to all speed bins and Test Condition “f = 1 MHz”. Changed typical value of I_{SB1} parameter from 1 µA to 2.5 µA corresponding to all speed bins. Changed typical value of I_{SB2} parameter from 1 µA to 2.5 µA corresponding to all speed bins. Updated Data Retention Characteristics: Changed typical value of I_{CCDR} parameter from 1 µA to 3 µA. Changed maximum value of I_{CCDR} parameter from 7 µA to 8.8 µA. Updated Package Diagrams: spec 51-85081 – Changed revision from *E to *F. Updated to new template.

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Continuity of ordering part numbers

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CY62146EV30 MoBL

4-Mbit (256K × 16) Static RAM

Features

- Very high speed: 45 ns
- Temperature ranges
  - Industrial: –40 °C to +85 °C
  - Automotive-A: –40 °C to +85 °C
- Wide voltage range: 2.20 V to 3.60 V
- Pin compatible with CY62146DV30
- Ultra low standby power
  - Typical standby current: 2.5 µA
  - Maximum standby current: 7 µA
- Ultra low active power
  - Typical active current: 3.5 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in a Pb-free 48-ball very fine-pitch ball grid array (VFBGA) and 44-pin TSOP II Packages

Functional Description

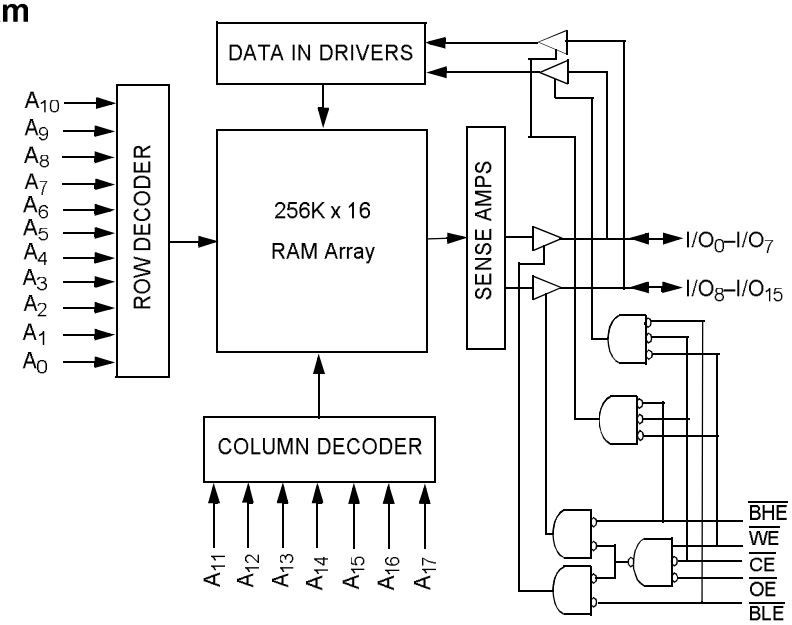
The CY62146EV30 is a high performance CMOS static RAM organized as 256K words by 16 bits. This device features an advanced circuit design designed to provide an ultra low active current. Ultra low active current is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption by 80 percent when addresses are not toggling.The device can also be put into standby mode reducing power consumption by more than 99 percent when deselected ($\overline{CE}$ HIGH). The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or a write operation is in progress ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{17}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from the I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{17}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appears on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See the Truth Table on page 11 for a complete description of read and write modes.

For a complete list of related documentation, click here.

Logic Block Diagram



Contents

Pin Configurations

Figure 1. 48-ball VFBGA pinout [1, 2]

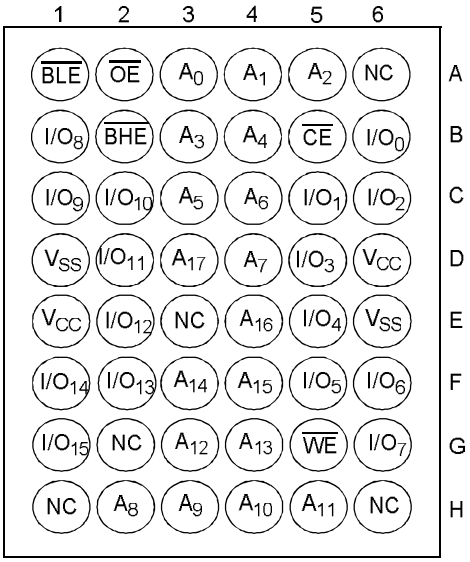
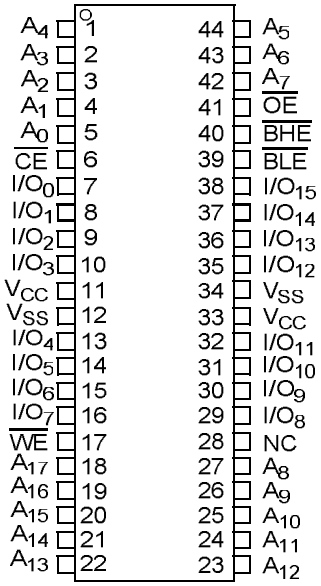


Figure 2. 44-pin TSOP II pinout [1]



Product Portfolio

Product	Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
						f = 1 MHz		f = f_{max}			
		Min	Typ [3]	Max		Typ [3]	Max	Typ [3]	Max	Typ [3]	Max
CY62146EV30LL	Industrial/ Automotive-A	2.2	3.0	3.6	45	3.5	6	15	20	2.5	7

Notes
1. NC pins are not connected on the die.
2. Pins H1, G2, and H6 in the BGA package are address expansion pins for 8Mb, 16Mb and 32Mb respectively.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to + 150 °C

Ambient temperature with power applied ..... –55 °C to + 125 °C

Supply voltage to ground potential .....–0.3 V to + 3.9 V (V_{CCmax} + 0.3 V)

DC voltage applied to outputs in High-Z state [4, 5] ..... –0.3 V to 3.9 V (V_{CCmax} + 0.3 V)

DC input voltage [4, 5] ..... –0.3 V to 3.9 V ($V_{CC\ max}$ + 0.3 V)

Output current into outputs (LOW) ..... 20 mA

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... >2001 V

Latch-up Current ..... >200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC} [6]
CY62146EV30	Industrial/ Automotive-A	–40 °C to +85 °C	2.2 V to 3.6 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		45 ns (Industrial/Automotive-A)			Unit
				Min	Typ [7]	Max	
V_{OH}	Output high voltage	I_{OH} = –0.1 mA		2.0	–	–	V
		I_{OH} = –1.0 mA, $V_{CC} \geq$ 2.70 V		2.4	–	–	V
V_{OL}	Output low voltage	I_{OL} = 0.1 mA		–	–	0.4	V
		I_{OL} = 2.1 mA, $V_{CC} \geq$ 2.70 V		–	–	0.4	V
V_{IH}	Input high voltage	V_{CC} = 2.2 V to 2.7 V		1.8	–	V_{CC} + 0.3	V
		V_{CC} = 2.7 V to 3.6 V		2.2	–	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage	V_{CC} = 2.2 V to 2.7 V		–0.3	–	0.6	V
		V_{CC}= 2.7 V to 3.6 V		–0.3	–	0.8	V
I_{IX}	Input leakage current	GND $\leq V_I \leq V_{CC}$		–1	–	+1	µA
I_{OZ}	Output leakage current	GND $\leq V_O \leq V_{CC}$, Output disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	f = f_{max} = $1/t_{RC}$	V_{CC} = $V_{CC(max)}$, I_{OUT} = 0 mA CMOS levels	–	15	20	mA
		f = 1 MHz		–	3.5	6	
I_{SB1}	Automatic CE power down current – CMOS inputs	$\overline{CE}$ > V_{CC} – 0.2 V, V_{IN} > V_{CC} – 0.2 V or V_{IN} < 0.2 V, f = f_{max} (Address and data only), f = 0 ($\overline{OE}$, $\overline{BHE}$, $\overline{BLE}$ and $\overline{WE}$), V_{CC} = 3.60 V		–	2.5	7	µA
I_{SB2} [8]	Automatic CE power down current – CMOS inputs	$\overline{CE} \geq V_{CC}$ – 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V or $V_{IN} \leq$ 0.2 V, f = 0, V_{CC} = 3.60 V		–	2.5	7	µA

Notes

4. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
5. $V_{IH(max)}$ = V_{CC} + 0.75 V for pulse durations less than 20 ns.
6. Full device AC operation assumes a minimum of 100 µs ramp time from 0 to V_{cc}(min) and 200 µs wait time after V_{cc} stabilization.
7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
8. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB1}/I_{SB2}/I_{CCDR} spec. Other inputs can be left floating.

Capacitance

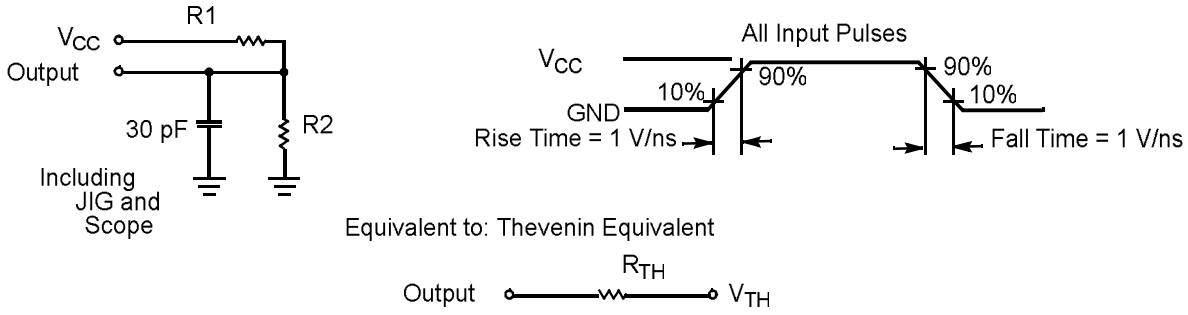
Parameter [9]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [9]	Description	Test Conditions	VFBGA	TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	42.10	55.52	°C/W
Θ_{JC}	Thermal resistance (junction to case)		23.45	16.03	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Parameter	2.50 V	3.0 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Note
9. Tested initially and after any design or process changes that may affect these parameters.

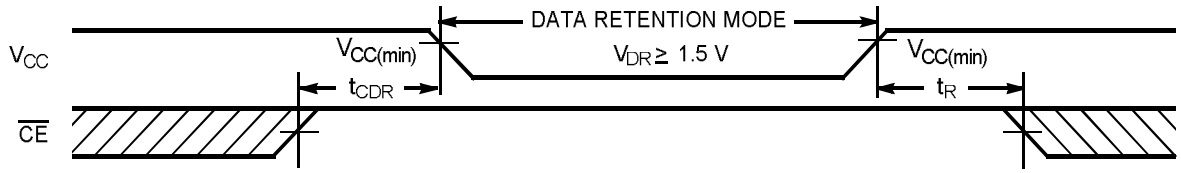
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions		Min	Typ [10]	Max	Unit
V_{DR}	V_{CC} for data retention			1.5	–	–	V
I_{CCDR} [11]	Data retention current	V_{CC} = 1.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	Industrial/ Automotive-A	–	3	8.8	µA
t_{CDR} [12]	Chip deselect to data retention time	–		0	–	–	ns
t_R [13]	Operation recovery time	–		45	–	–	ns

Data Retention Waveform

Figure 4. Data Retention Waveform



Notes

10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
11. Chip enable (CE) and byte enables (BHE and BLE) need to be tied to CMOS levels to meet the $I_{SB1}/I_{SB2}/I_{CCDR}$ spec. Other inputs can be left floating.
12. Tested initially and after any design or process changes that may affect these parameters.
13. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.

Switching Characteristics

Over the Operating Range

Parameter [14, 15]	Description	45 ns (Industrial/Automotive-A)		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	45	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z [16]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z [16, 17]	–	18	ns
t_{LZCE}	$\overline{CE}$ LOW to Low-Z [16]	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High-Z [16, 17]	–	18	ns
t_{PU}	$\overline{CE}$ LOW to power up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power down	–	45	ns
t_{DBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to data valid	–	22	ns
t_{LZBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low-Z [16]	5	–	ns
t_{HZBE}	$\overline{BLE}$ / $\overline{BHE}$ HIGH to High-Z [16, 17]	–	18	ns
Write Cycle [18, 19]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	ns
t_{BW}	$\overline{BLE}$ / $\overline{BHE}$ LOW to write end	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z [16, 17]	–	18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z [16]	10	–	ns

Notes

14. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1 V/ns) or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the Figure 3 on page 5.
15. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Notes AN13842 and AN66311. However, the issue has been fixed and in production now, and hence, these Application Notes are no longer applicable. They are available for download on our website as they contain information on the date code of the parts, beyond which the fix has been in production.
16. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
17. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
18. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write
19. The minimum write pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 5. Read Cycle 1 (Address Transition Controlled) [20, 21]

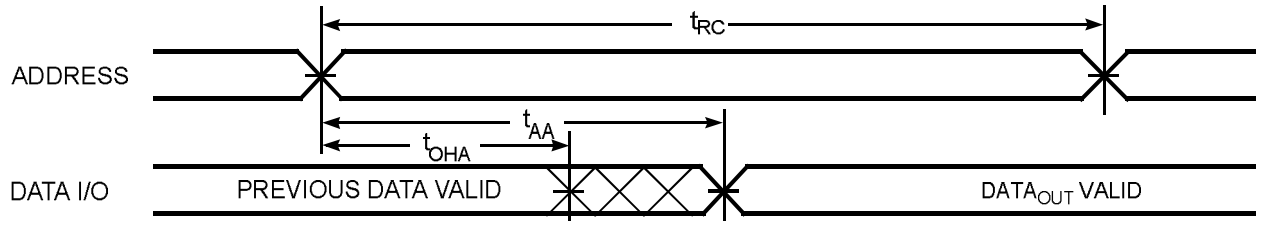
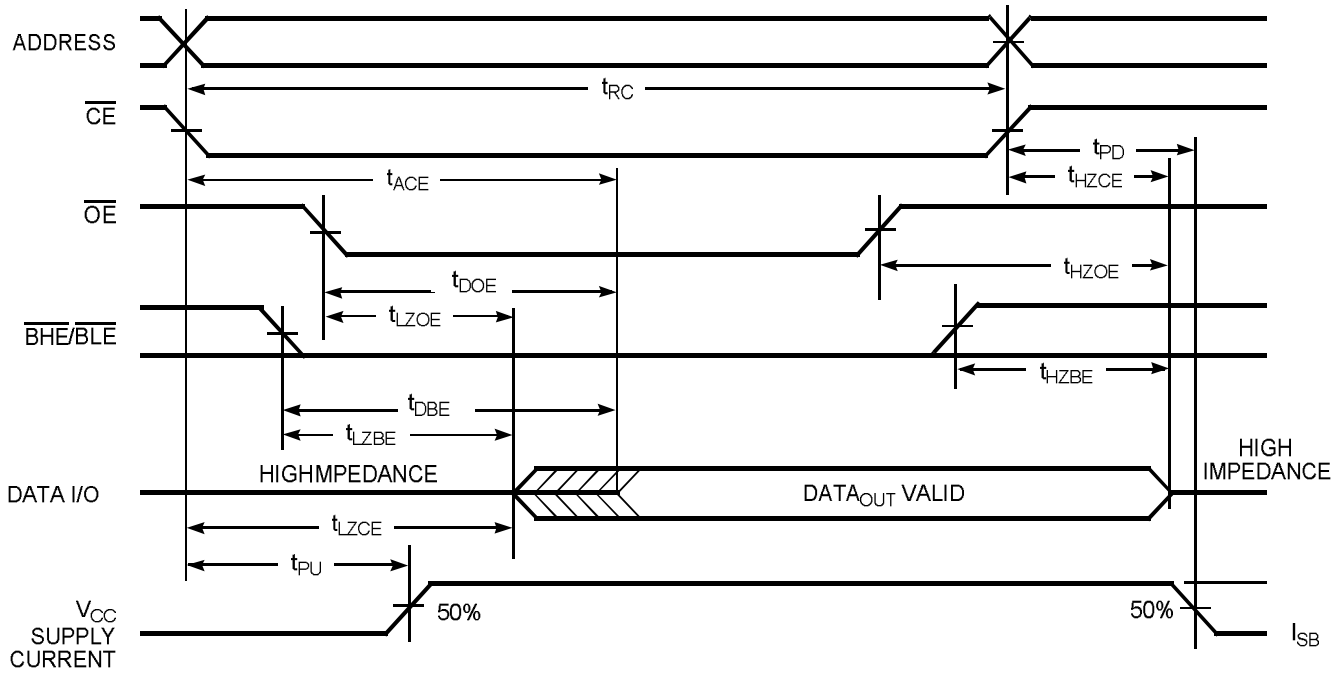


Figure 6. Read Cycle No. 2 ($\overline{OE}$ Controlled) [21, 22]



Notes
20. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}.
21. $\overline{WE}$ is HIGH for read cycle.
22. Address valid before or similar to $\overline{CE}$ and $\overline{BHE}$, $\overline{BLE}$ transition LOW.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 (WE Controlled) [23, 24, 25]

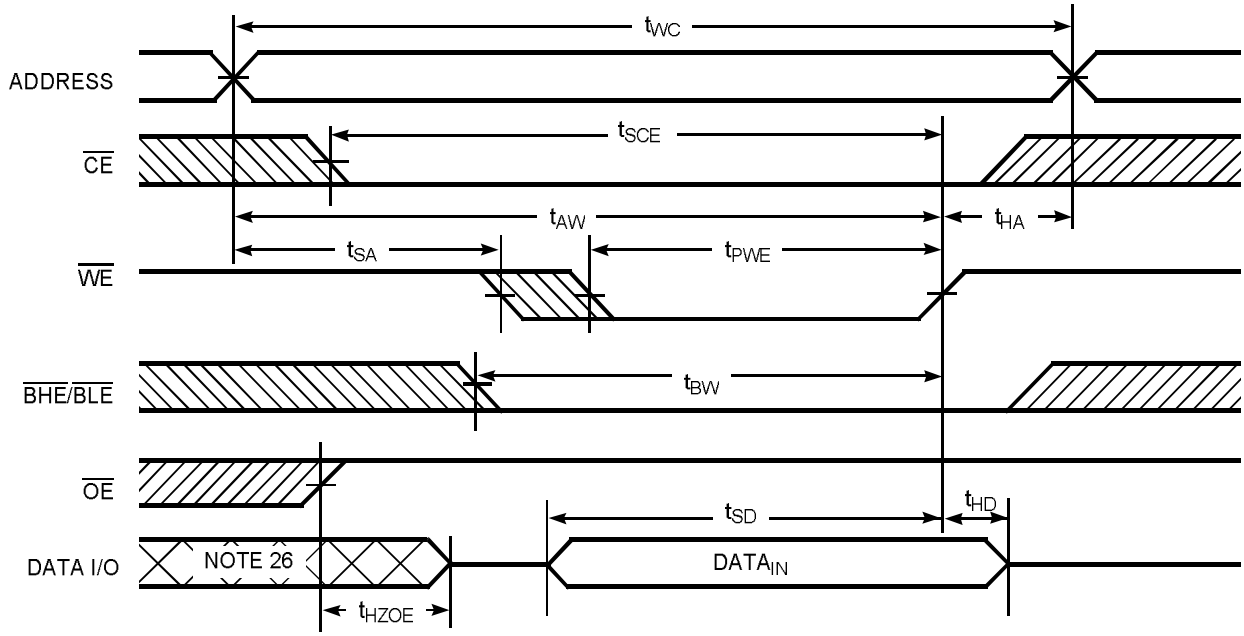
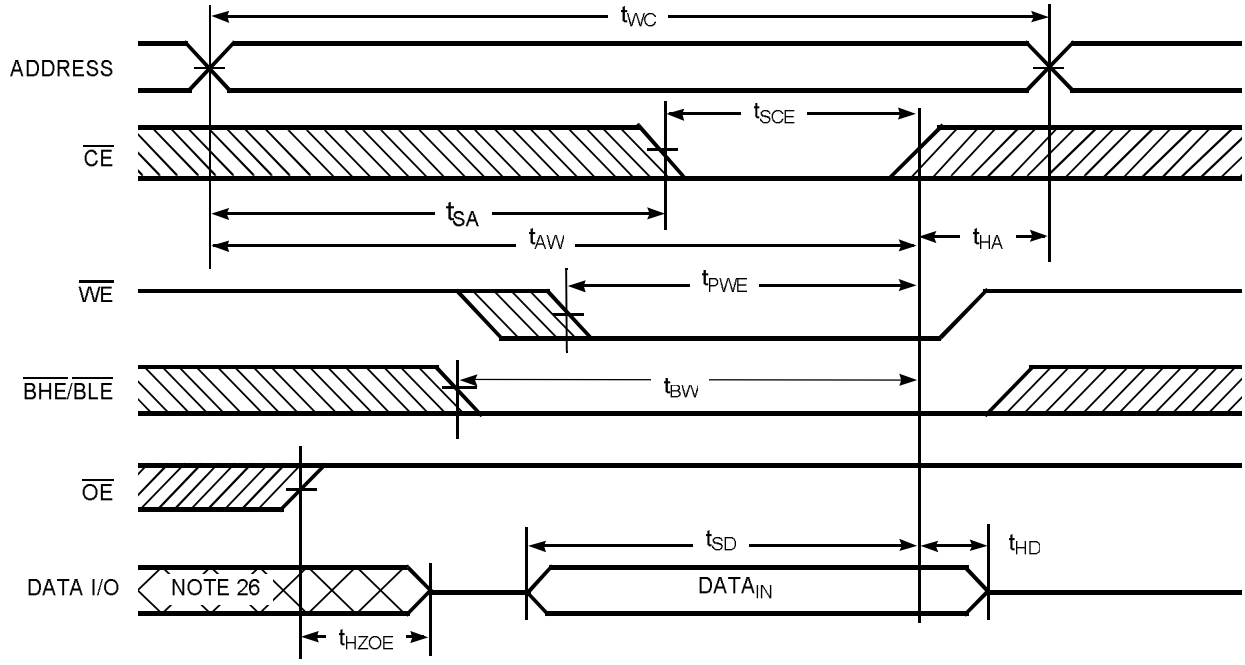


Figure 8. Write Cycle No. 2 (CE Controlled) [23, 24, 25]



Notes

23. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
24. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
25. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
26. During this period, the I/Os are in output state and input signals must not be applied.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 (WE Controlled, OE LOW) [27, 28]

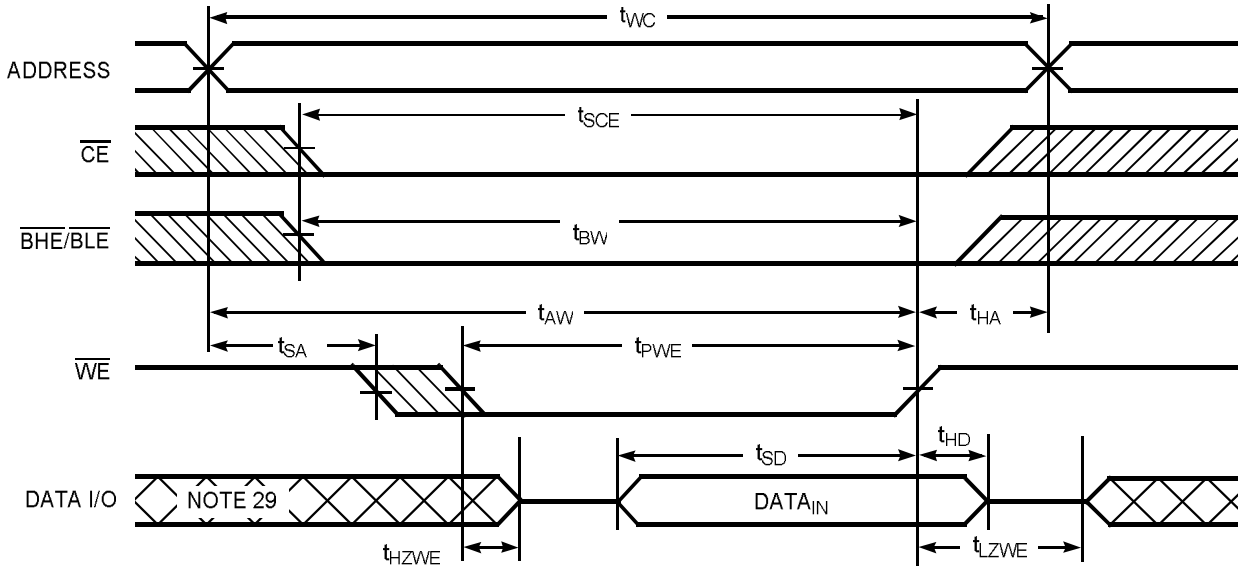
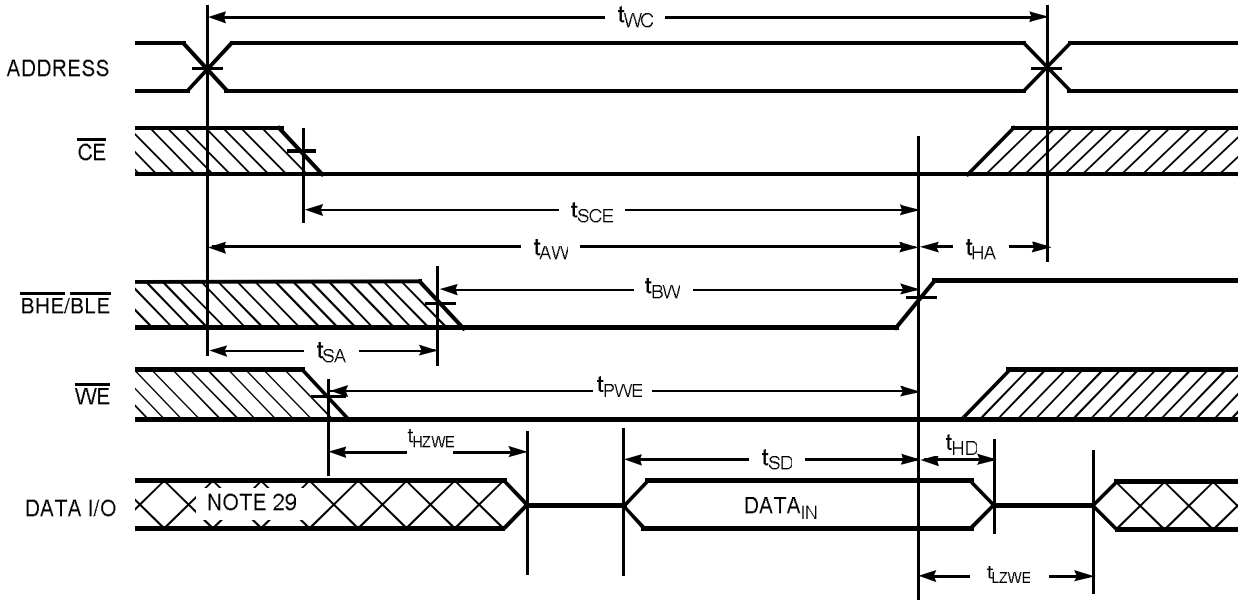


Figure 10. Write Cycle No. 4 (BHE/BLE Controlled, OE LOW) [27]



Notes
27. If CE goes HIGH simultaneously with WE = V_{IH}, the output remains in a high impedance state.
28. The minimum write pulse width for Write Cycle No. 3 (WE Controlled, OE LOW) should be sum of t_{HZWE} and t_{SD}.
29. During this period, the I/Os are in output state and input signals must not be applied.

Truth Table

$\overline{CE}$ [30]	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High-Z	Deselect/power-down	Standby (I_{SB})
L	X	X	H	H	High-Z	Output disabled	Active (I_{CC})
L	H	L	L	L	Data out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data out (I/O_0–I/O_7); I/O_8–I/O_{15} in High-Z	Read	Active (I_{CC})
L	H	L	L	H	Data out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High-Z	Read	Active (I_{CC})
L	H	H	L	L	High-Z	Output disabled	Active (I_{CC})
L	H	H	H	L	High-Z	Output disabled	Active (I_{CC})
L	H	H	L	H	High-Z	Output disabled	Active (I_{CC})
L	L	X	L	L	Data in (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data in (I/O_0–I/O_7); I/O_8–I/O_{15} in High-Z	Write	Active (I_{CC})
L	L	X	L	H	Data in (I/O_8–I/O_{15}); I/O_0–I/O_7 in High-Z	Write	Active (I_{CC})

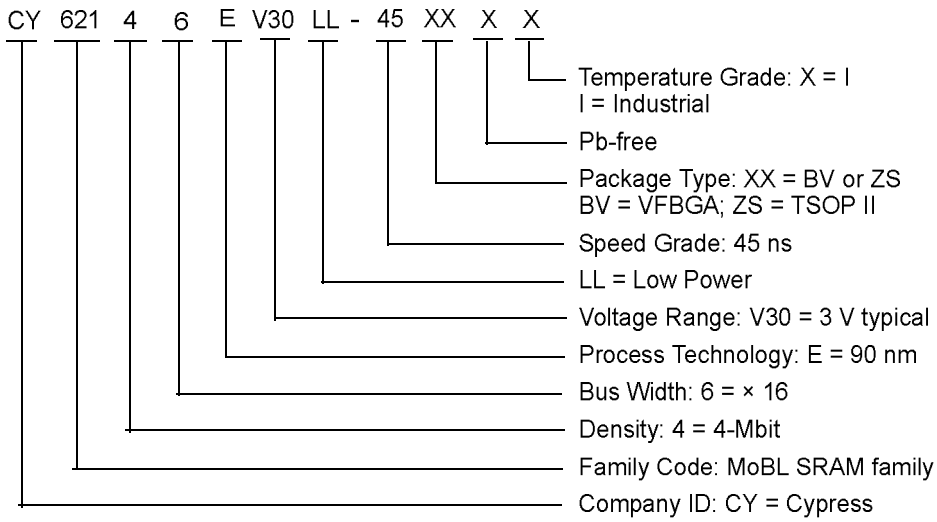
Note
30. Chip enable must be at CMOS levels (not floating). Intermediate voltage levels on this pin is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62146EV30LL-45BVXI	51-85150	48-ball VFBGA (Pb-free)	Industrial
	CY62146EV30LL-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	

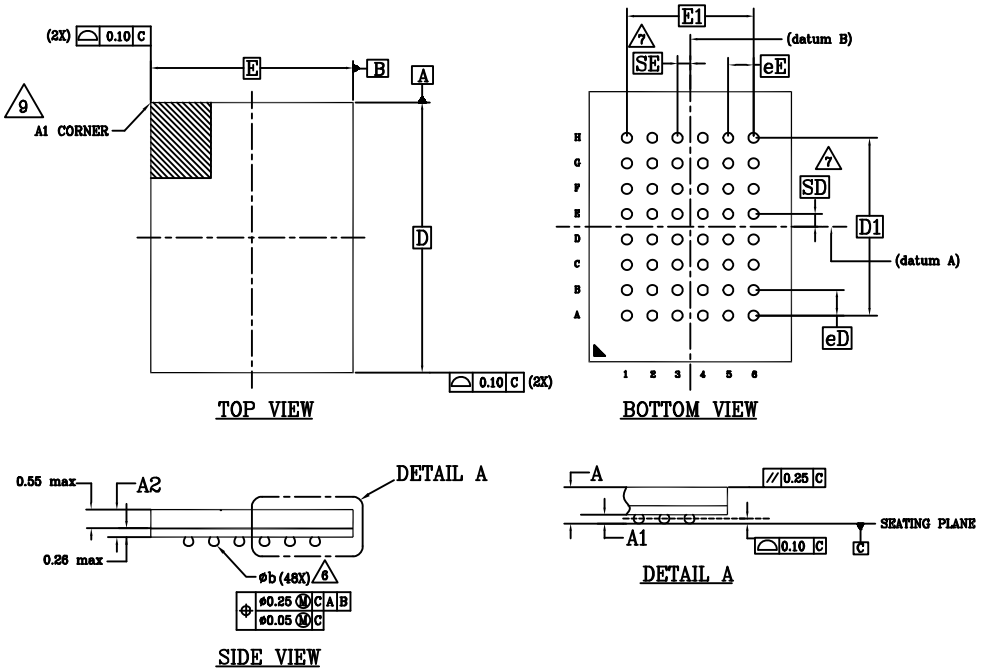
Please contact your local Cypress sales representative for availability of other parts

Ordering Code Definitions



Package Diagrams

Figure 11. 48-ball VFBGA (6 × 8 × 1.0 mm) Package Outline, 51-85150



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.16	-	-
A2	-	-	0.81
D	8.00 BSC		
E	6.00 BSC		
D1	5.25 BSC		
E1	3.75 BSC		
MD	8		
ME	6		
n	48		
Ø b	0.25	0.30	0.35
eE	0.75 BSC		
eD	0.75 BSC		
SD	0.375 BSC		
SE	0.375 BSC		

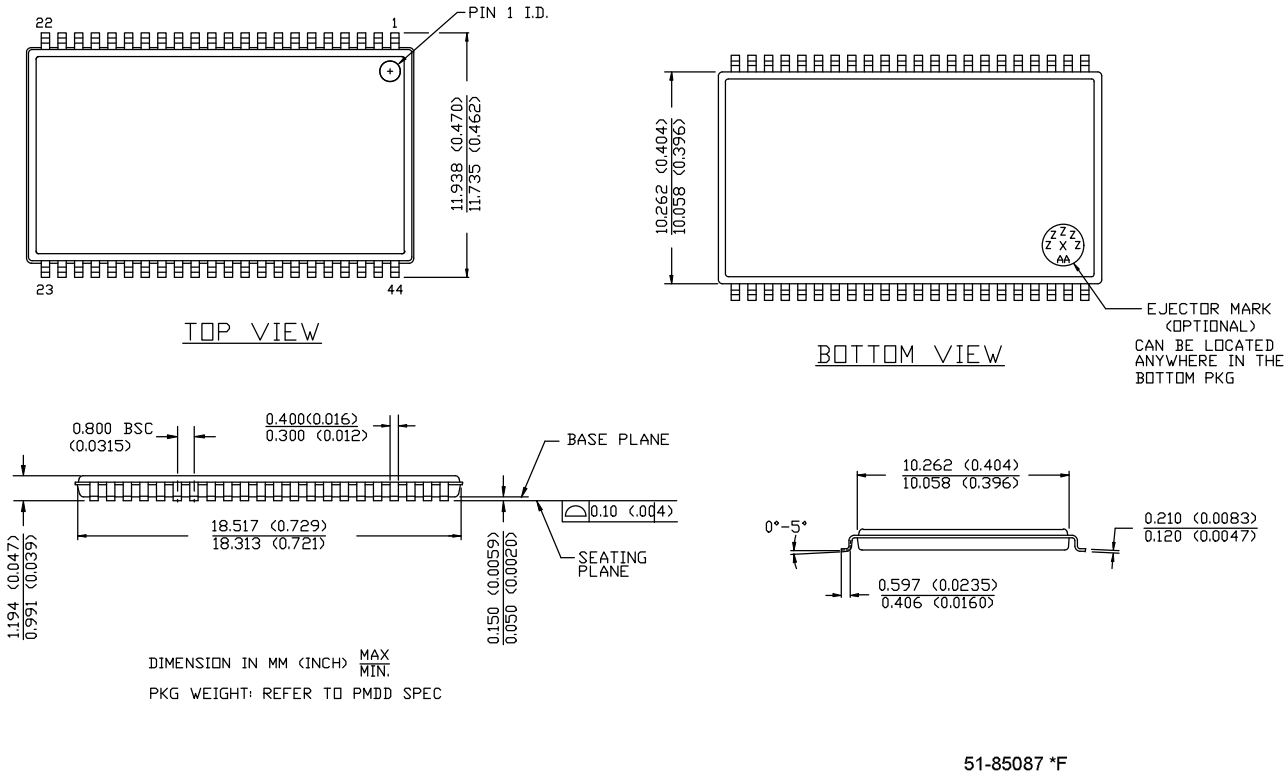
NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. [e] REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.

51-85150 *I

Package Diagrams (continued)

Figure 12. 44-pin TSOP II (18.4 × 10.2 × 1.194 mm) Package Outline, 51-85087



51-85087 *F

Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
CMOS	Complementary Metal Oxide Semiconductor
$\overline{CE}$	Chip Enable
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Gird Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62146EV30 MoBL, 4-Mbit (256K × 16) Static RAM Document Number: 38-05567			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
**	223225	05/05/2004	New data sheet.
*A	247373	07/28/2004	Changed status from Advance Information to Preliminary. Updated Operating Range: Updated Note 6 (Replaced "100 µs wait time" with "200 µs wait time"). Updated Data Retention Characteristics: Changed maximum value of I_{CCDR} parameter from 2.0 µA to 2.5 µA. Changed minimum value of t_R parameter from 100 µs to t_{RC} ns. Updated Switching Characteristics: Changed minimum value of t_{OHA} parameter from 6 ns to 10 ns corresponding to both 35 ns and 45 ns speed bin. Changed maximum value of t_{DOE} parameter from 15 ns to 18 ns corresponding to 35 ns speed bin. Changed maximum value of t_{HZOE}, t_{HZBE}, and t_{HZWE} parameters from 12 ns to 15 ns corresponding 35 ns speed bin and from 15 ns to 18 ns corresponding to 45 ns speed bin. Changed maximum value of t_{HZCE} parameter from 12 ns to 18 ns corresponding to 35 ns speed bin and from 15 ns to 22 ns corresponding to 45 ns speed bin. Changed maximum value of t_{DBE} parameter from 15 ns to 18 ns corresponding to 35 ns speed bin. Changed minimum value of t_{SCE} and t_{BW} parameters from 25 to 30 ns corresponding to 35 ns speed bin and from 40 ns to 35 ns corresponding to 45 ns speed bin. Changed minimum value of t_{SD} parameter from 15 ns to 18 ns corresponding to 35 ns speed bin and from 20 ns to 22 ns corresponding to 45 ns speed bin. Removed Note "If both Byte Enables ($\overline{BHE}$ and $\overline{BLE}$) are toggled together then this value is 6 ns min. Otherwise this value is 3 ns min." and its reference in t_{LZBE} parameter. Updated Ordering Information: Updated part numbers.
*B	414807	12/16/2005	Changed status from Preliminary to Final. Removed "L" version of CY62146EV30 part in all instances across the document. Removed 35 ns speed bin related information in all instances across the document. Changed the address of Cypress Semiconductor Corporation in Page 1 from "3901 North First Street" to "198 Champion Court". Updated Pin Configurations: Updated Figure 1 (Replaced DNU with NC corresponding to ball E3). Removed Note "DNU pins have to be left floating or tied to V_{SS} to ensure proper application." and its reference. Updated Electrical Characteristics: Changed typical value of I_{CC} parameter from 12 mA to 15 mA corresponding to 45 ns speed bin and Test Condition "f = f_{max}". Changed typical value of I_{CC} parameter from 1.5 mA to 2 mA corresponding to 45 ns speed bin and Test Condition "f = 1 MHz". Changed maximum value of I_{CC} parameter from 2 mA to 2.5 mA corresponding to 45 ns speed bin and Test Condition "f = 1 MHz". Changed typical value of I_{SB1} parameter from 0.7 µA to 1 µA corresponding to 45 ns speed bin. Changed maximum value of I_{SB1} parameter from 2.5 µA to 7 µA corresponding to 45 ns speed bin. Changed typical value of I_{SB2} parameter from 0.7 µA to 1 µA corresponding to 45 ns speed bin. Changed maximum value of I_{SB2} parameter from 2.5 µA to 7 µA corresponding to 45 ns speed bin. Updated AC Test Loads and Waveforms: Updated Figure 3 (Replaced 50 pF with 30 pF).

Document History Page (continued)

Document Title: CY62146EV30 MoBL, 4-Mbit (256K × 16) Static RAM Document Number: 38-05567			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
*B (cont.)	414807	12/16/2005	Updated Data Retention Characteristics: Changed maximum value of I_{CCDR} parameter from 2.5 µA to 7 µA. Added typical value of I_{CCDR} parameter. Updated Switching Characteristics: Changed minimum value of t_{LZOE} parameter from 3 ns to 5 ns corresponding to 45 ns speed bin. Changed minimum value of t_{LZCE} parameter from 6 ns to 10 ns corresponding to 45 ns speed bin. Changed maximum value of t_{HZCE} parameter from 22 ns to 18 ns corresponding to 45 ns speed bin. Changed minimum value of t_{LZBE} parameter from 6 ns to 5 ns corresponding to 45 ns speed bin. Changed minimum value of t_{PWE} parameter from 30 ns to 35 ns corresponding to 45 ns speed bin. Changed minimum value of t_{SD} parameter from 22 ns to 25 ns corresponding to 45 ns speed bin. Changed minimum value of t_{LZWE} parameter from 6 ns to 10 ns corresponding to 45 ns speed bin. Updated Ordering Information: Updated part numbers. Removed “Package Name” column. Added “Package Diagram” column. Updated Package Diagrams: spec 51-85150 – Changed revision from *B to *D. Updated to new template.
*C	925501	04/09/2007	Updated Electrical Characteristics: Added Note 8 and referred the same note in I_{SB2} parameter. Updated Data Retention Characteristics: Added Note 11 and referred the same note in I_{CCDR} parameter. Updated Switching Characteristics: Added Note 15 and referred the same note in “Parameter” column.
*D	2678796	03/25/2009	Added Automotive-A Temperature Range related information in all instances across the document. Completing Sunset Review.
*E	2944332	06/04/2010	Updated Truth Table: Added Note 30 and referred the same note in “$\overline{CE}$” column. Updated Package Diagrams: spec 51-85150 – Changed revision from *D to *E. spec 51-85087 – Changed revision from *A to *C. Updated to new template.
*F	3109050	12/13/2010	Changed all Table Footnotes to Notes in all instances across the document. Updated Ordering Information: No change in part numbers. Added Ordering Code Definitions. Updated Package Diagrams: spec 51-85150 – Changed revision from *E to *F.
*G	3302915	07/14/2011	Updated Functional Description: Removed “For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.” at the end. Updated Ordering Information: No change in part numbers. Updated Ordering Code Definitions. Added Units of Measure. Updated to new template.

Document History Page (continued)

Document Title: CY62146EV30 MoBL, 4-Mbit (256K × 16) Static RAM Document Number: 38-05567			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
*H	3961126	04/10/2013	Updated Package Diagrams: spec 51-85150 – Changed revision from *F to *H. spec 51-85087 – Changed revision from *C to *E. Completing Sunset Review.
*I	4101995	08/22/2013	Updated Switching Characteristics: Updated Note 15. Updated to new template.
*J	4348752	04/16/2014	Updated Switching Characteristics: Added Note 19 and referred the same note in “Write Cycle”. Updated Switching Waveforms: Added Note 28 and referred the same note in Figure 9 (for t_{PWE} parameter in $\overline{WE}$ Controlled, $\overline{OE}$ LOW Write Cycle). Completing Sunset Review.
*K	4576526	11/21/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*L	5233278	04/21/2016	Updated Thermal Resistance: Replaced “two-layer” with “four-layer” in “Test Conditions” column. Updated all values in “VFBGA” and “TSOP II” columns. Updated to new template. Completing Sunset Review.
*M	6029183	01/12/2018	Updated Ordering Information: Updated part numbers. Updated to new template.
*N	6560465	04/29/2019	Updated Package Diagrams: spec 51-85150 – Changed revision from *H to *I. Updated to new template. Completing Sunset Review.
*O	6906316	06/26/2020	Updated Features: Changed value of Typical standby current from 1 µA to 2.5 µA. Changed value of Typical active current from 2 mA to 3.5 mA. Updated Product Portfolio: Changed typical value of Operating I_{CC} from 2 mA to 3.5 mA corresponding to “f = 1 MHz”. Changed maximum value of Operating I_{CC} from 2.5 mA to 6 mA corresponding to “f = 1 MHz”. Changed typical value of Standby, I_{SB2} from 1 µA to 2.5 µA. Updated Electrical Characteristics: Changed typical value of I_{CC} parameter from 2 mA to 3.5 mA corresponding to Test Condition “f = 1 MHz”. Changed maximum value of I_{CC} parameter from 2.5 mA to 6 mA corresponding to Test Condition “f = 1 MHz”. Changed typical value of I_{SB1} parameter from 1 µA to 2.5 µA. Changed typical value of I_{SB2} parameter from 1 µA to 2.5 µA. Updated Data Retention Characteristics: Changed typical value of I_{CCDR} parameter from 0.8 µA to 3 µA. Changed maximum value of I_{CCDR} parameter from 7 µA to 8.8 µA. Updated Package Diagrams: spec 51-85087 – Changed revision from *E to *F. Updated to new template.

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CY62148EV30 MoBL

4-Mbit (512K × 8) Static RAM

Features

- Very high speed: 45 ns
  - Wide voltage range: 2.20 V to 3.60 V
- Temperature range:
  - Industrial: –40 °C to +85 °C
  - Automotive-A: –40 °C to +85 °C
- Pin compatible with CY62148DV30
- Ultra low standby power
  - Typical standby current: 2.5 µA
  - Maximum standby current: 7 µA (Industrial)
- Ultra low active power
  - Typical active current: 3.5 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 36-ball very fine-pitch ball grid array (VFBGA), 32-pin thin small outline package (TSOP) II, and 32-pin small outline integrated circuit (SOIC)[1] packages

Functional Description

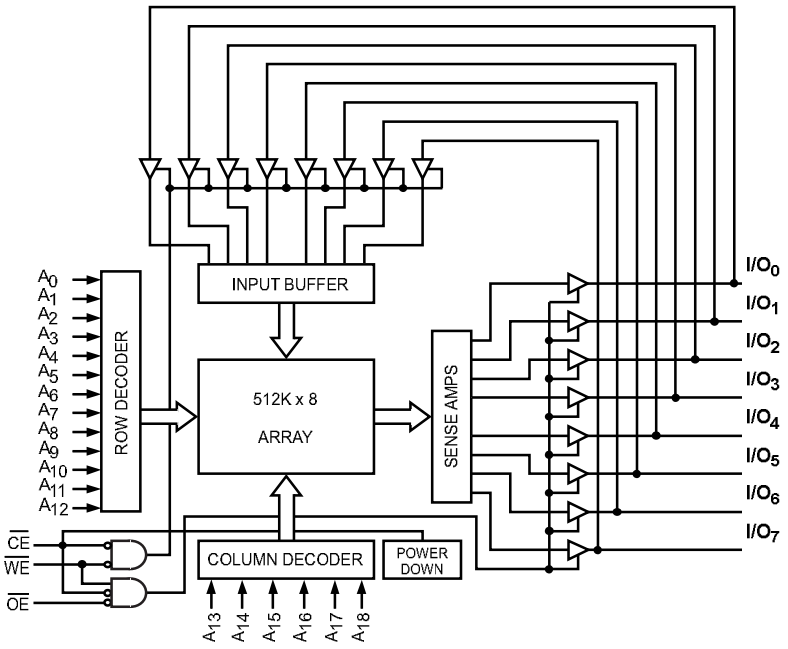
The CY62148EV30 is a high performance CMOS static RAM organized as 512K words by 8 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption. Placing the device into standby mode reduces power consumption by more than 99 percent when deselected ($\overline{CE}$ HIGH). The eight input and output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

For a complete list of related 1documentation, click here.

Logic Block Diagram



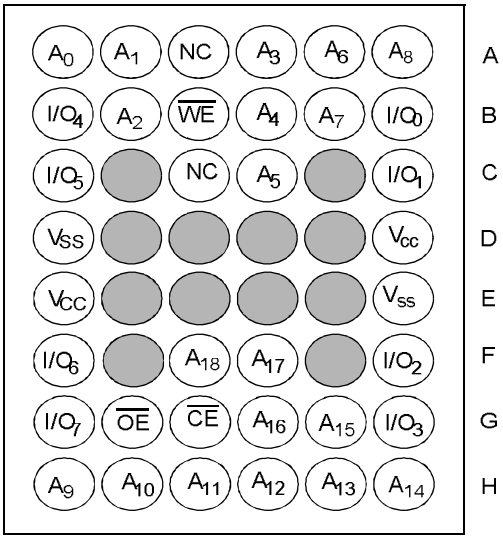
Note
1. SOIC package is available only in 55 ns speed bin.

Contents

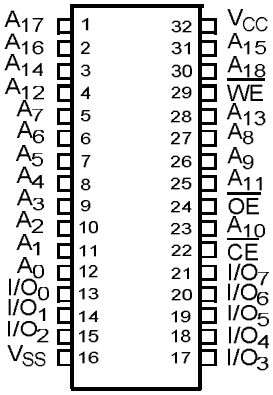
Pin Configurations

VFBGA, SOIC and TSOP II pinouts are as follows. [2, 3]

36-ball VFBGA pinout
Top View



32-pin SOIC/TSOP II pinout
Top View



Product Portfolio

Product		Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
							Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
							f = 1 MHz		f = f_{max}			
			Min	Typ [4]	Max		Typ [4]	Max	Typ [4]	Max	Typ [4]	Max
CY62148EV30LL	VFBGA	Industrial	2.2	3.0	3.6	45	3.5	6	15	20	2.5	7
	TSOP II	Industrial / Automotive-A										
	SOIC	Industrial	2.2	3.0	3.6	55	3.5	6	15	20	2.5	7

Notes
2. SOIC package is available only in 55 ns speed bin.
3. NC pins are not connected on the die.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... 55 °C to +125 °C

Supply voltage to ground potential .....–0.3 V to $V_{CC(max)}$ + 0.3 V

DC voltage applied to outputs in High Z State [5, 6] .....–0.3 V to $V_{CC(max)}$ + 0.3 V

DC input voltage [5, 6] .....–0.3 V to $V_{CC(max)}$ + 0.3 V

Output current into outputs (LOW) .....20 mA

Static discharge voltage (MIL-STD-883, Method 3015) ..... > 2001 V

Latch up current ..... > 200 mA

Operating Range

Product	Range	Ambient Temperature	V_{CC} [7]
CY62148EV30	Industrial/ Automotive-A	–40 °C to +85 °C	2.2 V to 3.6 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		-45 (Industrial / Automotive-A)			-55 [8]			Unit
				Min	Typ [9]	Max	Min	Typ [9]	Max	
V_{OH}	Output high voltage	I_{OH} = –0.1 mA		2.0	–	–	2.0	–	–	V
		I_{OH} = –1.0 mA, $V_{CC} \geq$ 2.70 V		2.4	–	–	2.4	–	–	V
V_{OL}	Output low voltage	I_{OL} = 0.1 mA		–	–	0.4	–	–	0.2	V
		I_{OL} = 2.1 mA, $V_{CC} \geq$ 2.70 V		–	–	0.4	–	–	0.4	V
V_{IH}	Input high voltage	V_{CC} = 2.2 V to 2.7 V		1.8	–	V_{CC} + 0.3	1.8	–	V_{CC} + 0.3	V
		V_{CC} = 2.7 V to 3.6 V		2.2	–	V_{CC} + 0.3	2.2	–	V_{CC} + 0.3	V
V_{IL}	Input low voltage	V_{CC} = 2.2 V to 2.7 V	For VFBGA and TSOP II packages	–0.3	–	0.6	–	–	–	V
			For SOIC package	–	–	–	–0.3	–	0.4 [10]	V
		V_{CC} = 2.7 V to 3.6 V	For VFBGA and TSOP II packages	–0.3	–	0.8	–	–	–	V
			For SOIC package	–	–	–	–0.3	–	0.6 [10]	
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_C		–1	–	+1	–1	–	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, Output disabled		–1	–	+1	–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	f = f_{max} = 1/t_{RC}	V_{CC} = $V_{CC(max)}$, I_{OUT} = 0 mA, CMOS levels	–	15	20	–	15	20	mA
		f = 1 MHz		–	3.5	6	–	3.5	6	
I_{SB1} [11]	Automatic CE power down current – CMOS inputs	$\overline{CE} \geq V_{CC}$ – 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V, $V_{IN} \leq$ 0.2 V, f = f_{max} (Address and Data Only), f = 0 ($\overline{OE}$ and $\overline{WE}$), V_{CC} = 3.60 V		–	2.5	7	–	2.5	7	µA
I_{SB2} [11]	Automatic CE power down current – CMOS inputs	$\overline{CE} \geq V_{CC}$ – 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V or $V_{IN} \leq$ 0.2 V, f = 0, V_{CC} = 3.60 V		–	2.5	7	–	2.5	7	µA

Notes

5. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
6. $V_{IH(max)}$ = V_{CC} + 0.75 V for pulse durations less than 20 ns.
7. Full device AC operation assumes a minimum of 100 µs ramp time from 0 to $V_{CC(min)}$ and 200 µs wait time after V_{CC} stabilization.
8. SOIC package is available only in 55 ns speed bin.
9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
10. Under DC conditions the device meets a V_{IL} of 0.8V (for V_{CC} range of 2.7 V to 3.6 V) and 0.6 V (for V_{CC} range of 2.2 V to 2.7 V). However, in dynamic conditions Input LOW voltage applied to the device must not be higher than 0.6V and 0.4V for the above ranges. This is applicable to SOIC package only.
11. Chip Enable ($\overline{CE}$) must be HIGH at CMOS level to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

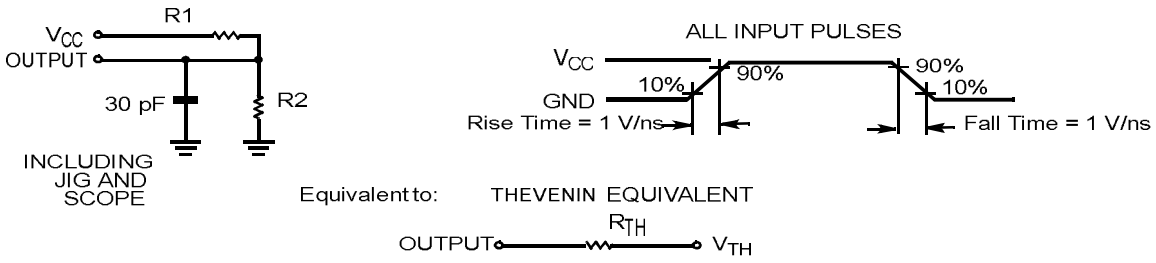
Parameter [12]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [12]	Description	Test Conditions	36-ball VFBGA Package	32-pin TSOP II Package	32-pin SOIC Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	44.79	59.10	51.57	°C/W
Θ_{JC}	Thermal resistance (junction to case)		23.17	12.19	25.01	°C/W

AC Test Loads and Waveforms

Figure 1. AC Test Loads and Waveforms



Parameter	2.50 V	3.0 V	Unit
R_1	16667	1103	Ω
R_2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Note
12. Tested initially and after any design or process changes that may affect these parameters.

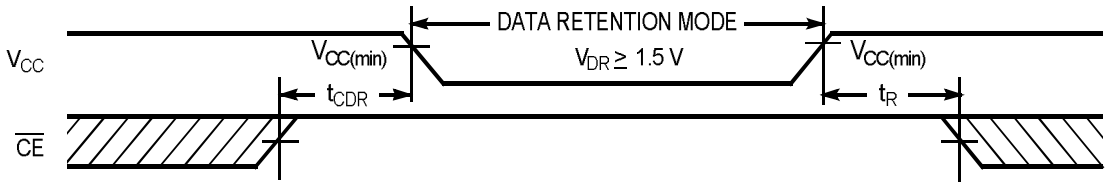
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions		Min	Typ [13]	Max	Unit
V_{DR}	V_{CC} for data retention			1.5	–	–	V
I_{CCDR} [14]	Data retention current	V_{CC} = 1.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	Industrial/ Automotive-A	–	3	8.8	µA
t_{CDR} [15]	Chip deselect to data retention time			0	–	–	ns
t_R [16]	Operation recovery time		CY62148EV30LL-45	45	–	–	ns
			CY62148EV30LL-55	55	–	–	ns

Data Retention Waveform

Figure 2. Data Retention Waveform



Notes

13. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
14. Chip Enable ($\overline{CE}$) must be HIGH at CMOS level to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
15. Tested initially and after any design or process changes that may affect these parameters.
16. Full device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.

Switching Characteristics

Over the Operating Range

Parameter [17, 18]	Description	-45 (Industrial / Automotive-A)		-55 [19]		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	45	–	55	–	ns
t_{AA}	Address to data valid	–	45	–	55	ns
t_{OHA}	Data hold from address change	10	–	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	45	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	–	25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z [20]	5	–	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [20, 21]	–	18	–	20	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z [20]	10	–	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z [20, 21]	–	18	–	20	ns
t_{PU}	$\overline{CE}$ LOW to power-up	0	–	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down	–	45	–	55	ns
Write Cycle [22, 23]						
t_{WC}	Write cycle time	45	–	55	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	35	–	40	–	ns
t_{AW}	Address setup to write end	35	–	40	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	40	–	ns
t_{SD}	Data setup to write end	25	–	25	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [20, 21]	–	18	–	20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [20]	10	–	10	–	ns

Notes

17. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the chip enable signal as described in the Application Note AN66311. However, the issue has been fixed and in production now, and hence, this Application Note is no longer applicable. It is available for download on our website as it contains information on the date code of the parts, beyond which the fix has been in production.
18. Test Conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the Figure 1 on page 5.
19. SOIC package is available only in 55 ns speed bin.
20. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
21. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the output enter a high impedance state.
22. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
23. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 3. Read Cycle No. 1 (Address Transition Controlled) [24, 25]

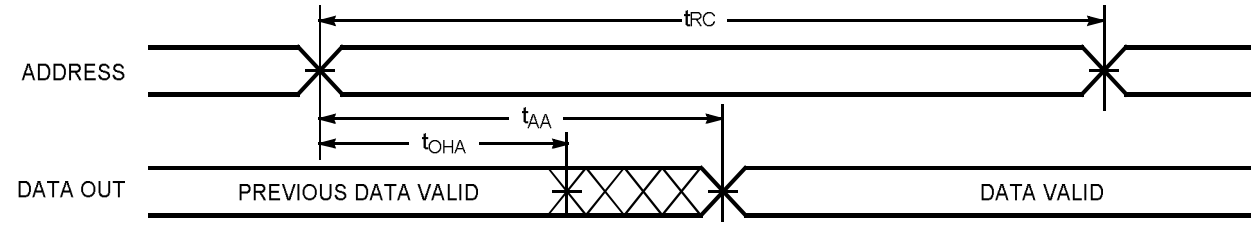


Figure 4. Read Cycle No. 2 ($\overline{OE}$ Controlled) [25, 26]

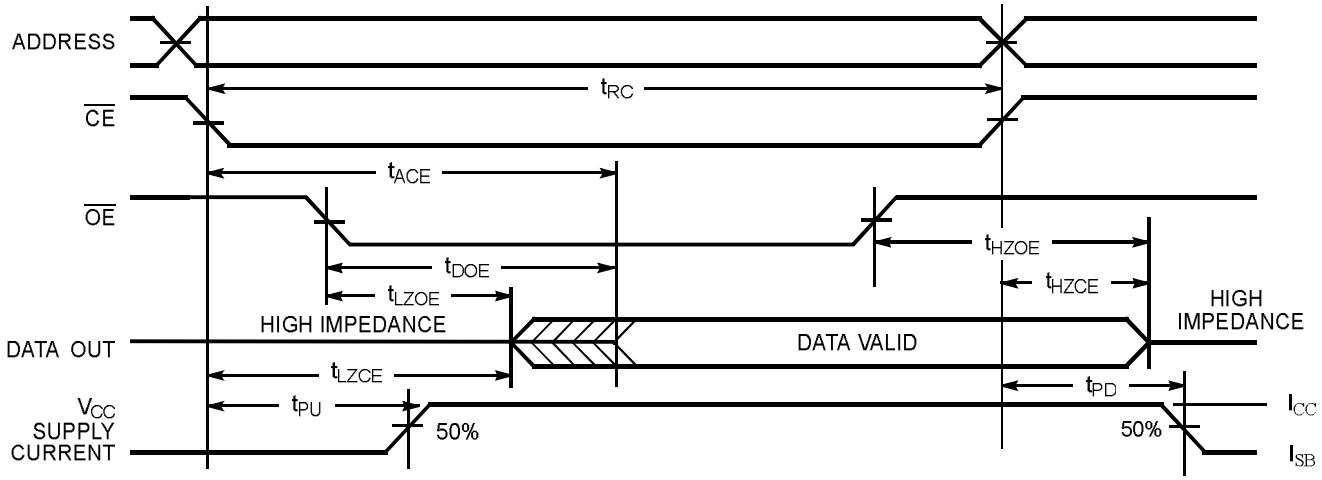
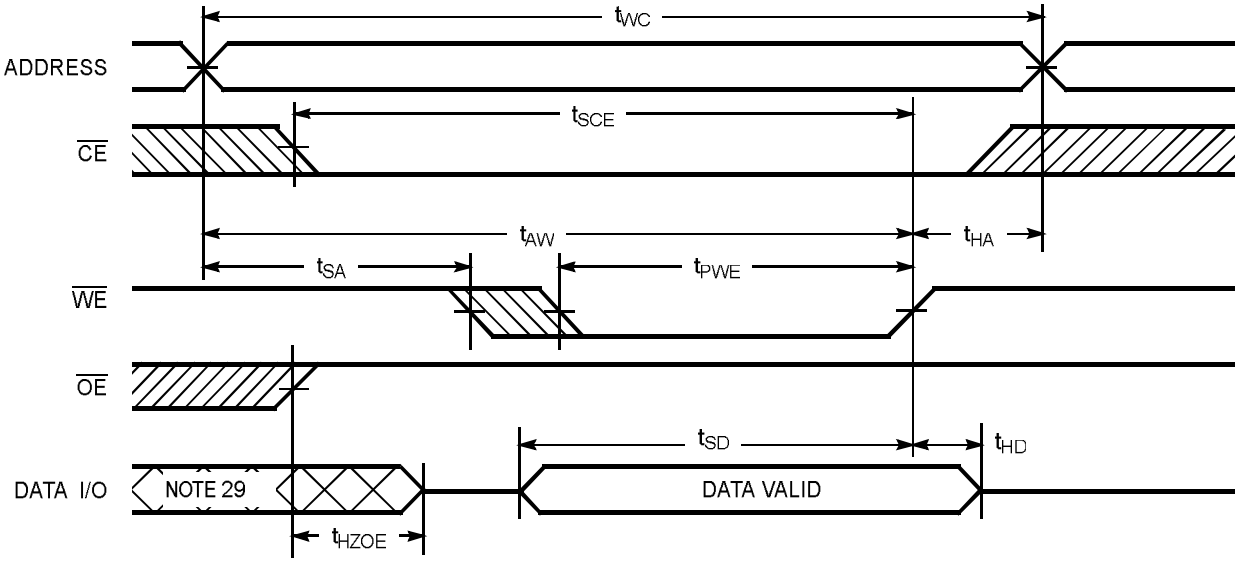


Figure 5. Write Cycle No. 1 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write) [27, 28]



Notes

24. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
25. $\overline{WE}$ is HIGH for read cycles.
26. Address valid before or similar to $\overline{CE}$ transition LOW.
27. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
28. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
29. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 2 ($\overline{CE}$ Controlled) [30, 31]

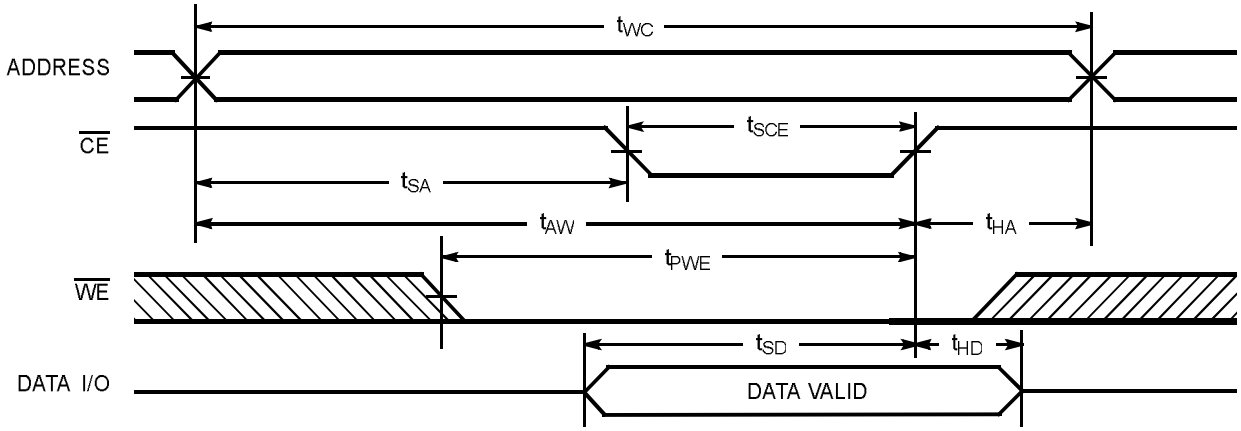
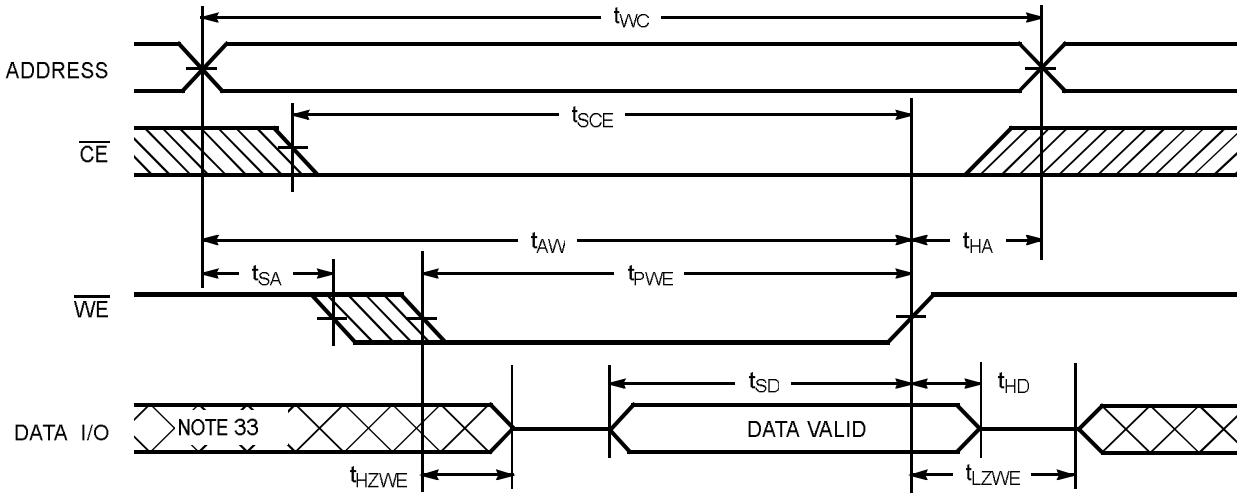


Figure 7. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [31, 32]



Notes
30. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
31. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
32. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE}.
33. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{CE}$ [34]	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power down	Standby (I_{SB})
L	H	L	Data out	Read	Active (I_{CC})
L	H	H	High Z	Output disabled	Active (I_{CC})
L	L	X	Data in	Write	Active (I_{CC})

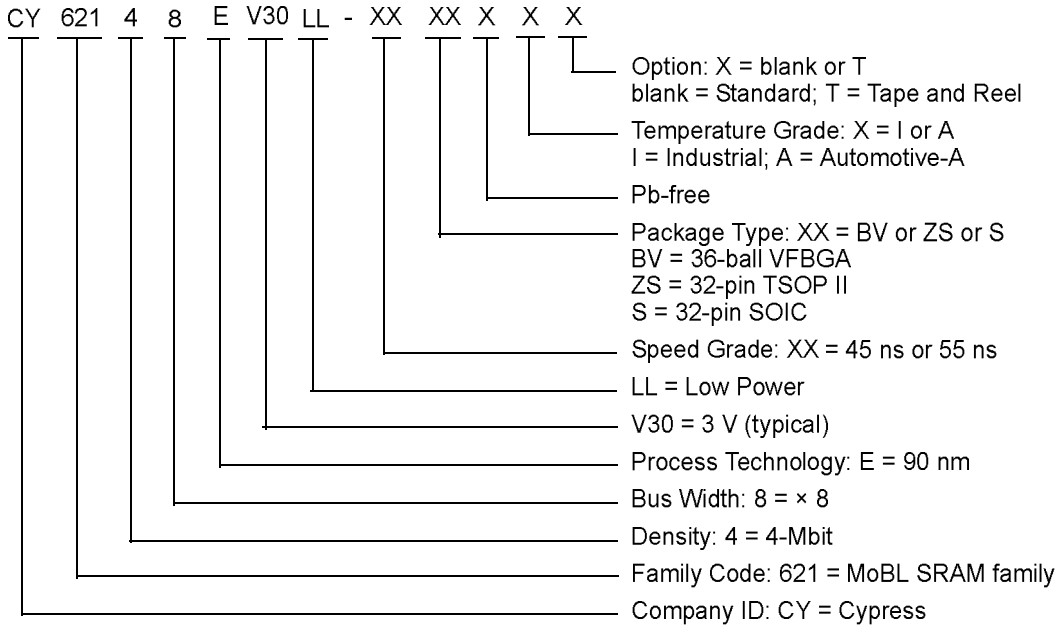
Note
34. Chip enable must be at CMOS levels (not floating). Intermediate voltage levels on this pin is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62148EV30LL-45BVI	51-85149	36-ball VFBGA	Industrial
	CY62148EV30LL-45BVXI	51-85149	36-ball VFBGA (Pb-free)	
	CY62148EV30LL-45BVXIT	51-85149	36-ball VFBGA (Pb-free)	
	CY62148EV30LL-45ZSXI	51-85095	32-pin TSOP II (Pb-free)	
55	CY62148EV30LL-55SXI	51-85081	32-pin SOIC (Pb-free)	Industrial

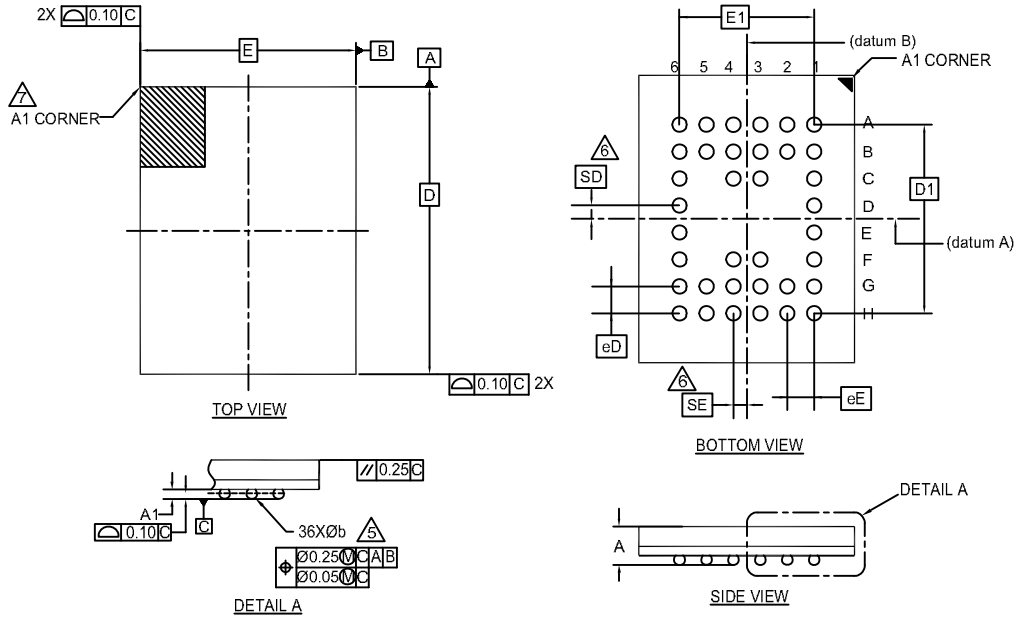
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagrams

Figure 8. 36-ball VFBGA (8.0 × 6.0 × 1.0 mm) Package Outline, 51-85149



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.16	-	-
D	8.00 BSC		
E	6.00 BSC		
D1	5.25 BSC		
E1	3.75 BSC		
MD	8		
ME	6		
N	36		
Ø b	0.25	0.30	0.35
eD	0.75 BSC		
eE	0.75 BSC		
SD	0.375 BSC		
SE	0.375 BSC		

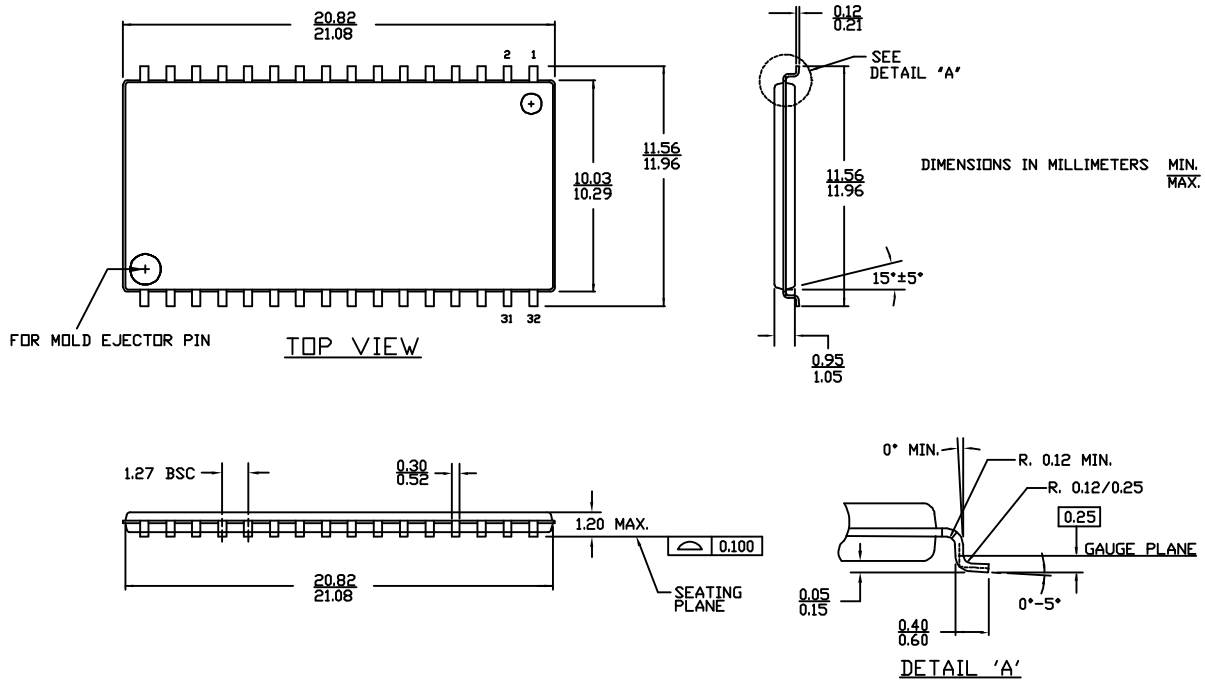
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.

51-85149 *G

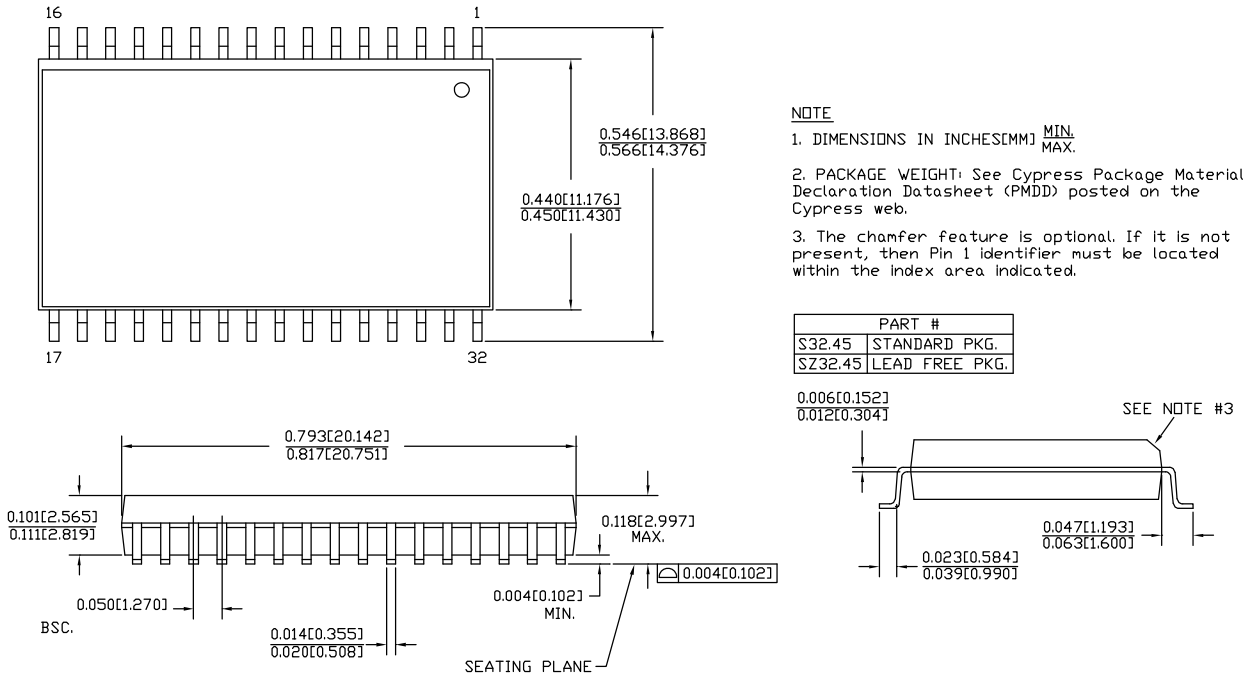
Package Diagrams (continued)

Figure 9. 32-pin TSOP II (20.95 × 11.76 × 1.0 mm) Package Outline, 51-85095



Package Diagrams (continued)

Figure 10. 32-pin SOIC (450 Mils) Package Outline, 51-85081



51-85081 *F

Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
CMOS	Complementary Metal Oxide Semiconductor
$\overline{CE}$	Chip Enable
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
µA	microampere
mA	milliampere
ns	nanosecond
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62148EV30 MoBL, 4-Mbit (512K × 8) Static RAM Document Number: 38-05576			
Region	**ECN**	**Submission Date**	**Description of Change**
**	223225	05/05/2004	New data sheet.
*A	247373	07/28/2004	Changed status from Advance Information to Preliminary. Updated Operating Range: Updated Note 7 (Changed V_{CC} stabilization time from 100 µs to 200 µs). Updated Data Retention Characteristics: Changed maximum value of I_{CCDR} parameter from 2.0 µA to 2.5 µA. Changed minimum value of t_R parameter from 100 µs to t_{RC} ns. Updated Switching Characteristics: Changed minimum value of t_{OHA} parameter from 6 ns to 10 ns corresponding to both 35 ns and 45 ns speed bins. Changed maximum value of t_{DOE} parameter from 15 ns to 18 ns corresponding to 35 ns speed bin. Changed maximum value of t_{HZOE}, t_{HZWE} parameters from 12 ns to 15 ns corresponding to 35 ns speed bin and 15 ns to 18 ns corresponding to 45 ns speed bin. Changed minimum value of t_{SCE} parameter from 25 ns to 30 ns corresponding to 35 ns speed bin and 40 ns to 35 ns corresponding to 45 ns speed bin. Changed maximum value of t_{HZCE} parameter from 12 ns to 18 ns corresponding to 35 ns speed bin and 15 ns to 22 ns corresponding to 45 ns speed bin. Changed minimum value of t_{SD} parameter from 15 ns to 18 ns corresponding to 35 ns speed bin and 20 ns to 22 ns corresponding to 45 ns speed bin. Updated Ordering Information: Updated part numbers.
*B	414807	12/16/2005	Changed status from Preliminary to Final. Changed the address of Cypress Semiconductor Corporation on page 1 from “3901 North First Street” to “198 Champion Court”. Updated Features: Removed 35 ns speed bin related information. Updated Pin Configurations: Changed ball C3 from DNU to NC. Removed the Note “DNU pins have to be left floating or tied to V_{SS} to ensure proper application.” and its reference. Added 32-pin SOIC pinout. Updated Electrical Characteristics: Removed “L” version of CY62148EV30. Changed typical value of I_{CC} parameter from 12 mA to 15 mA corresponding to Test Condition “f = f_{max}”. Changed typical value of I_{CC} parameter from 1.5 mA to 2 mA corresponding to Test Condition “f = 1 MHz”. Changed maximum value of I_{CC} parameter from 2 mA to 2.5 mA corresponding to Test Condition “f = 1 MHz”. Changed typical value of I_{SB1} and I_{SB2} parameters from 0.7 µA to 1 µA. Changed maximum value of I_{SB1} and I_{SB2} parameters from 2.5 µA to 7 µA. Updated AC Test Loads and Waveforms: Changed the AC test load capacitance value from 50 pF to 30 pF. Updated Data Retention Characteristics: Changed maximum value of I_{CCDR} parameter from 2.5 µA to 7 µA. Added typical value of I_{CCDR} parameter. Updated Switching Characteristics: Changed minimum value of t_{LZOE} parameter from 3 ns to 5 ns. Changed minimum value of t_{LZCE} and t_{LZWE} parameters from 6 ns to 10 ns. Changed maximum value of t_{HZCE} parameter from 22 ns to 18 ns. Changed minimum value of t_{PWE} parameter from 30 ns to 35 ns. Changed minimum value of t_{SD} parameter from 22 ns to 25 ns.

Document History Page (continued)

Document Title: CY62148EV30 MoBL, 4-Mbit (512K × 8) Static RAM Document Number: 38-05576			
Region	**ECN**	**Submission Date**	**Description of Change**
*B (cont.)	414807	12/16/2005	Updated Ordering Information: Updated part numbers. Removed "Package Name" column. Added "Package Diagram" column. Updated Package Diagrams: spec 51-85149 – Changed revision from *B to *C. Added spec 51-85081 *B. Updated to new template.
*C	464503	05/25/2006	Added Automotive Temperature Range related information in all instances across the document. Updated Ordering Information: Updated part numbers.
*D	833080	03/09/2007	Updated Electrical Characteristics: Added details of V_{IL} parameter corresponding to Test Condition "SOIC package". Added Note 10 and referred the same note in the maximum value of V_{IL} parameter corresponding to SOIC package.
*E	890962	03/30/2007	Removed Automotive Temperature Range related information in all instances across the document. Updated Features: Added Note 1 and referred the same note in 32-pin SOIC package. Updated Electrical Characteristics: Added Note 11 and referred the same note in I_{SB2} parameter. Updated Switching Characteristics: Added values for all parameters corresponding to 55 ns Industrial Temperature Range. Updated Ordering Information: Updated part numbers.
*F	987940	04/18/2007	Updated Electrical Characteristics: Changed maximum value of V_{OL} parameter from 0.4 V to 0.2 V corresponding to Industrial Temperature Range at I_{OL} = 0.1 mA. Changed maximum value of V_{IL} parameter from 0.6 V to 0.4 V corresponding to Industrial Temperature Range, SOIC package at V_{CC} = 2.2 V to 2.7 V. Updated Note 10. Updated Note 11 (made the note applicable for both I_{SB2} and I_{CCDR} parameters).
*G	2548575	08/05/2008	Added Automotive-A Temperature Range related information in all instances across the document. Updated Ordering Information: Updated part numbers. Updated to new template.
*H	2769239	09/25/2009	Updated Ordering Information: Updated part numbers.
*I	2944332	06/04/2010	Updated Truth Table: Added Note 34 and referred the same note in "$\overline{CE}$" column. Updated Package Diagrams: spec 51-85149 – Changed revision from *C to *D. spec 51-85095 – Changed revision from ** to *A. spec 51-85081 – Changed revision from *B to *C.
*J	3007403	08/13/2010	Updated Ordering Information: No change in part numbers. Added Ordering Code Definitions. Updated to new template. Completing Sunset Review.

Document History Page (continued)

Document Title: CY62148EV30 MoBL, 4-Mbit (512K × 8) Static RAM Document Number: 38-05576			
Region	**ECN**	**Submission Date**	**Description of Change**
*K	3110202	12/14/2010	Updated Logic Block Diagram. Updated Ordering Information: No change in part numbers. Updated Ordering Code Definitions.
*L	3302901	07/06/2011	Updated Functional Description: Removed "For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines." at the end. Updated Ordering Information: No change in part numbers. Updated Ordering Code Definitions. Updated Package Diagrams: spec 51-85095 – Changed revision from *A to *B. Updated to new template. Completing Sunset Review.
*M	3363097	09/07/2011	Updated Data Retention Characteristics: Removed reference of Note 12 in I_{CCDR} parameter. Added Note 14 and referred the same note in I_{CCDR} parameter. Updated Package Diagrams: spec 51-85149 – Changed revision from *D to *E. spec 51-85081 – Changed revision from *C to *D.
*N	3546715	03/09/2012	Updated Electrical Characteristics: Updated Note 10 (Removed the line "Refer to AN13470 for details".).
*O	3733339	09/04/2012	Minor text edits. Completing Sunset Review.
*P	4102967	08/23/2013	Updated Switching Characteristics: Added Note 17 and referred the same note in "Parameter" column. Updated Package Diagrams: spec 51-85081 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.
*Q	4307881	04/09/2014	Updated Switching Characteristics: Updated description of t_{PD} parameter (Replaced "$\overline{CE}$ HIGH to power-up" with "$\overline{CE}$ HIGH to power-down").
*R	4576526	11/21/2014	Updated Functional Description: Added "For a complete list of related 1documentation, click here." at the end. Updated Switching Characteristics: Added Note 23 and referred the same note in "Write Cycle". Updated Switching Waveforms: Added Note 32 and referred the same note in Figure 7.
*S	4802206	06/18/2015	Updated Package Diagrams: spec 51-85149 – Changed revision from *E to *F. spec 51-85095 – Changed revision from *B to *D. Updated to new template.
*T	5234869	04/22/2016	Updated Ordering Information: Updated part numbers. Updated Ordering Code Definitions (Added Tape and Reel option). Updated Package Diagrams: spec 51-85149 – Changed revision from *F to *G. Updated to new template.

Document History Page (continued)

Document Title: CY62148EV30 MoBL, 4-Mbit (512K × 8) Static RAM Document Number: 38-05576			
Region	**ECN**	**Submission Date**	**Description of Change**
*U	5480386	10/18/2016	Updated Thermal Resistance: Replaced “two-layer” with “four-layer” in “Test Conditions” column. Updated values of Θ_{JA} parameter and Θ_{JC} parameter corresponding to all packages. Updated to new template. Completing Sunset Review.
*V	6045156	01/25/2018	Updated Ordering Information: Updated part numbers. Updated to new template.
*W	6531864	04/03/2019	Updated to new template.
*X	6906316	06/26/2020	Updated Features: Changed value of Typical standby current from 1 µA to 2.5 µA. Changed value of Typical active current from 2 mA to 3.5 mA. Updated Product Portfolio: Changed typical value of Operating I_{CC} from 2 mA to 3.5 mA corresponding to all packages and “f = 1 MHz”. Changed maximum value of Operating I_{CC} from 2.5 mA to 6 mA corresponding to all packages and “f = 1 MHz”. Changed typical value of Standby, I_{SB2} from 1 µA to 2.5 µA corresponding to all packages. Updated Electrical Characteristics: Changed typical value of I_{CC} parameter from 2 mA to 3.5 mA corresponding to all speed bins and Test Condition “f = 1 MHz”. Changed maximum value of I_{CC} parameter from 2.5 mA to 6 mA corresponding to all speed bins and Test Condition “f = 1 MHz”. Changed typical value of I_{SB1} parameter from 1 µA to 2.5 µA corresponding to all speed bins. Changed typical value of I_{SB2} parameter from 1 µA to 2.5 µA corresponding to all speed bins. Updated Data Retention Characteristics: Changed typical value of I_{CCDR} parameter from 0.8 µA to 3 µA. Changed maximum value of I_{CCDR} parameter from 7 µA to 8.8 µA. Updated Package Diagrams: spec 51-85081 – Changed revision from *E to *F. Updated to new template.

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