



Product Change Notification / SYST-07RIBE717

Date:

08-Jul-2020

Product Category:

N-Channel Enhancement Mode MOSFETs

PCN Type:

Document Change

Notification Subject:

Data Sheet - TN0604 N-Channel Enhancement-Mode Vertical DMOS FET Data Sheet

Affected CPNs:

[SYST-07RIBE717_Affected_CPN_07082020.pdf](#)

[SYST-07RIBE717_Affected_CPN_07082020.csv](#)

Notification Text:

SYST-07RIBE717

Microchip has released a new Product Documents for the TN0604 N-Channel Enhancement-Mode Vertical DMOS FET Data Sheet of devices. If you are using one of these devices please read the document located at [TN0604 N-Channel Enhancement-Mode Vertical DMOS FET Data Sheet](#).

Notification Status: Final

Description of Change: 1) Converted Supertex Doc# DSFP-TN0604 to Microchip DS20005934A 2) Created a pin function table 3) Changed the package marking format 4) Removed the TN0604 N3 P002, P003, and P014 media types 5) Updated the packaging medium of the TN0604 N3 P013 media type from 2000/Reel to 2000/Reel (Ammo Pack) to align it with the actual BQM 6) Made minor text changes throughout the document

Impacts to Data Sheet: None

Reason for Change: Conversion of Supertex datasheet to Microchip datasheet conventions.

Change Implementation Status: Complete

Date Document Changes Effective: 08 Jul 2020

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

[TN0604 N-Channel Enhancement-Mode Vertical DMOS FET Data Sheet](#)

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N-Channel Enhancement-Mode Vertical DMOS FET

Features

- 1.6V Maximum Low Threshold
- High Input Impedance
- 140 pF Typical Low Input Capacitance
- Fast Switching Speeds
- Low On-Resistance
- Free from Secondary Breakdown
- Low Input and Output Leakage

Applications

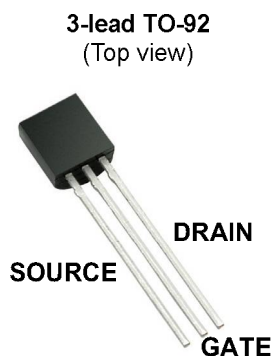
- Logic-Level Interfaces (Ideal for TTL and CMOS)
- Solid-State Relays
- Battery-Operated Systems
- Photovoltaic Drives
- Analog Switches
- General Purpose Line Drivers
- Telecommunication Switches

General Description

The TN0604 low-threshold, Enhancement-mode (normally-off) transistor uses a vertical DMOS structure and a well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

Microchip's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Type



See [Table 3-1](#) for pin information.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

| | |
|--------------------------------------------|-----------------------------------|
| Drain-to-Source Voltage | BV_{DSS} |
| Drain-to-Gate Voltage | BV_{DGS} |
| Gate-to-Source Voltage | $\pm 20V$ |
| Operating Ambient Temperature, T_A | $-55^{\circ}C$ to $+150^{\circ}C$ |
| Storage Temperature, T_S | $-55^{\circ}C$ to $+150^{\circ}C$ |

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: $T_A = 25^{\circ}C$ unless otherwise specified. All DC parameters are 100% tested at $25^{\circ}C$ unless otherwise stated. Pulse test: 300 μs pulse, 2% duty cycle

| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions |
|--------------------------------------------|---------------------|------|------|------|-----------------|---------------------------------------------------------------------------------------------|
| Drain-to-Source Breakdown Voltage | BV_{DSS} | 40 | — | — | V | $V_{GS} = 0V$, $I_D = 2\text{ mA}$ |
| Gate Threshold Voltage | $V_{GS(th)}$ | 0.6 | — | 1.6 | V | $V_{GS} = V_{DS}$, $I_D = 1\text{ mA}$ |
| Change in $V_{GS(th)}$ with Temperature | $\Delta V_{GS(th)}$ | — | -3.8 | -4.5 | mV/ $^{\circ}C$ | $V_{GS} = V_{DS}$, $I_D = 1\text{ mA}$ (Note 1) |
| Gate Body Leakage Current | I_{GSS} | — | — | 100 | nA | $V_{GS} = \pm 20V$, $V_{DS} = 0V$ |
| Zero-Gate Voltage Drain Current | I_{DSS} | — | — | 10 | μA | $V_{GS} = 0V$, $V_{DS} = \text{Maximum rating}$ |
| | | — | — | 1 | mA | $V_{DS} = 0.8 \text{ Maximum rating}$, $V_{GS} = 0V$, $T_A = 125^{\circ}C$ (Note 1) |
| On-State Drain Current | $I_{D(ON)}$ | 1.5 | 2.1 | — | A | $V_{GS} = 5V$, $V_{DS} = 20V$ |
| | | 4 | 7 | — | A | $V_{GS} = 10V$, $V_{DS} = 20V$ |
| Static Drain-to-Source On-State Resistance | $R_{DS(ON)}$ | — | 1 | 1.6 | Ω | $V_{GS} = 5V$, $I_D = 0.75A$ |
| | | — | 0.6 | 0.75 | Ω | $V_{GS} = 10V$, $I_D = 1.5A$ |
| Change in $R_{DS(ON)}$ with Temperature | $\Delta R_{DS(ON)}$ | — | 0.5 | 0.75 | %/ $^{\circ}C$ | $V_{GS} = 10V$, $I_D = 1.5A$ (Note 1) |

Note 1: Specification is obtained by characterization and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: $T_A = 25^\circ\text{C}$ unless otherwise specified. Specification is obtained by characterization and is not 100% tested.

| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions |
|----------------------------------|---------------------|------|------|------|------|----------------------------------------------------------------------------|
| Forward Transconductance | G _{FS} | 500 | 800 | — | mmho | V _{DS} = 20V, I _D = 1.5A |
| Input Capacitance | C _{ISS} | — | 140 | 190 | pF | V _{GS} = 0V, V _{DS} = 20V, f = 1 MHz |
| Common-Source Output Capacitance | C _{OSS} | — | 75 | 110 | pF | |
| Reverse Transfer Capacitance | C _{RSS} | — | 25 | 50 | pF | |
| Turn-On Delay Time | t _{d(ON)} | — | — | 10 | ns | V _{DD} = 20V, I _D = 0.5A, R _{GEN} = 25Ω |
| Rise Time | t _r | — | — | 6 | ns | |
| Turn-Off Delay Time | t _{d(OFF)} | — | — | 25 | ns | |
| Fall Time | t _f | — | — | 20 | ns | |
| DIODE PARAMETER | | | | | | |
| Diode Forward Voltage Drop | V _{SD} | — | 1.2 | 1.8 | V | V _{GS} = 0V, I _{SD} = 1.5A (Note 1) |
| Reverse Recovery Time | t _{rr} | — | 300 | — | ns | V _{GS} = 0V, I _{SD} = 1A |

Note 1: All DC parameters are 100% tested at $+25^\circ\text{C}$ unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle)

TEMPERATURE SPECIFICATIONS

| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions |
|-----------------------------------|---------------|------|------|------|--------------------|------------|
| TEMPERATURE RANGE | | | | | | |
| Operating Ambient Temperature | T_A | -55 | — | +150 | $^\circ\text{C}$ | |
| Storage Temperature | T_S | -55 | — | +150 | $^\circ\text{C}$ | |
| PACKAGE THERMAL RESISTANCE | | | | | | |
| 3-lead TO-92 | θ_{JA} | — | 132 | — | $^\circ\text{C/W}$ | |

THERMAL CHARACTERISTICS

| Package | I_D (Note 1) (Continuous) (A) | I_D (Pulsed) (A) | Power Dissipation at $T_A = 25^\circ\text{C}$ (W) | I_{DR} (Note 1) (A) | I_{DRM} (A) |
|--------------|------------------------------------------------|--------------------------|---------------------------------------------------------|-----------------------------------|------------------|
| 3-lead TO-92 | 0.7 | 4.6 | 0.74 | 0.7 | 4.6 |

Note 1: I_D (continuous) is limited by maximum rated T_J .

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

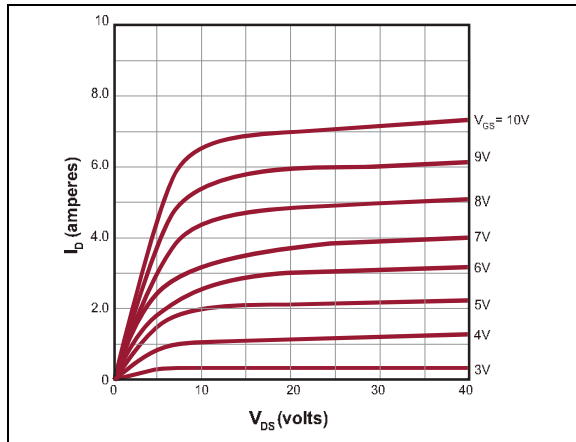


FIGURE 2-1: Output Characteristics.

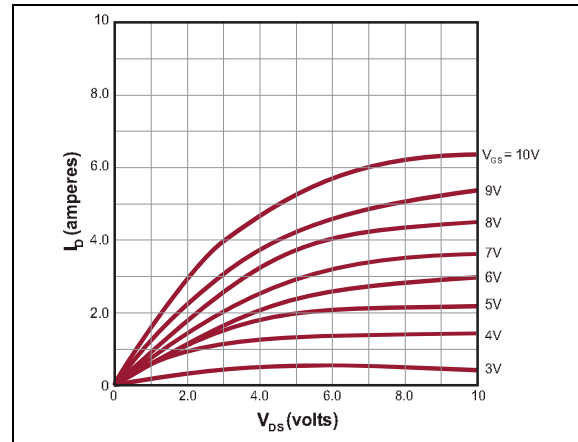


FIGURE 2-4: Saturation Characteristics.

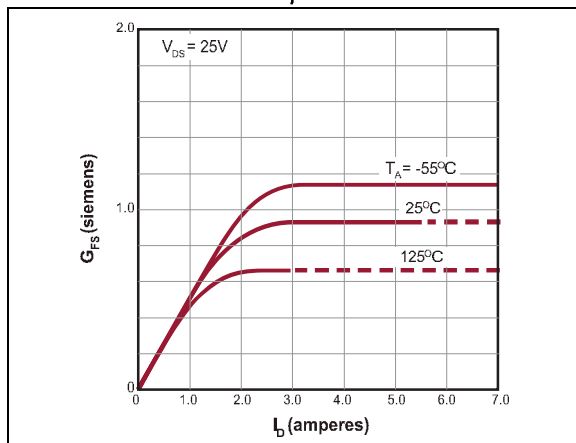


FIGURE 2-2: Transconductance vs. Drain Current.

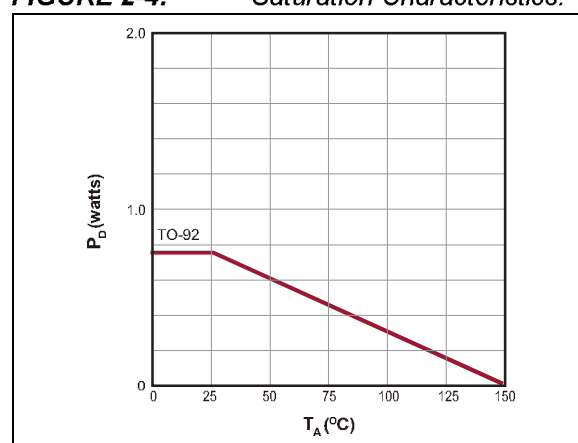


FIGURE 2-5: Power Dissipation vs. Ambient Temperature.

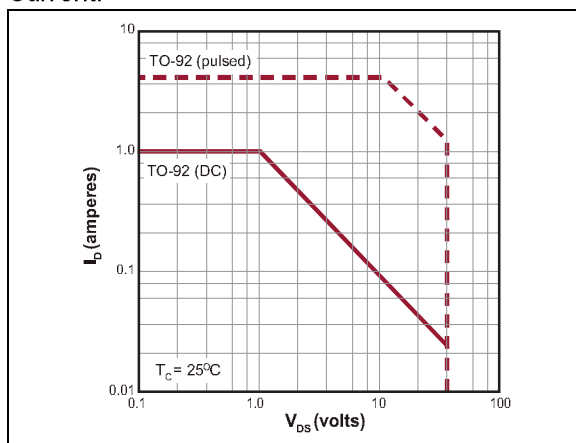


FIGURE 2-3: Maximum Rated Safe Operating Area.

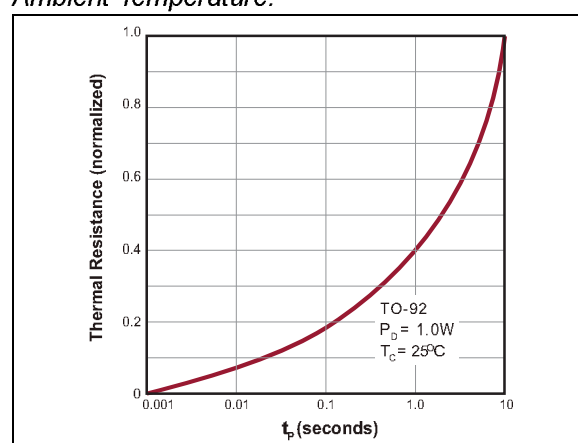


FIGURE 2-6: Thermal Response Characteristics.

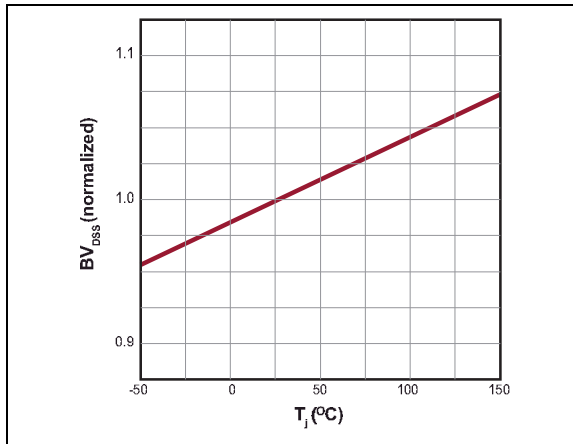


FIGURE 2-7: BV_{DSS} Variation with Temperature.

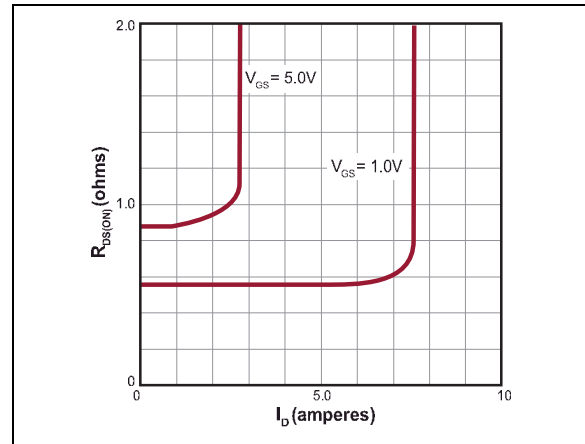


FIGURE 2-10: On-Resistance vs. Drain Current.

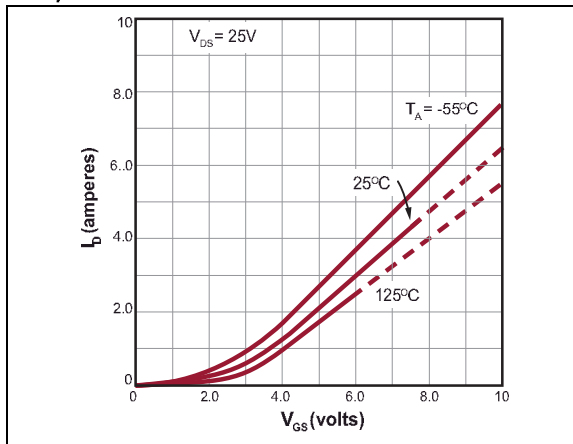


FIGURE 2-8: Transfer Characteristics.

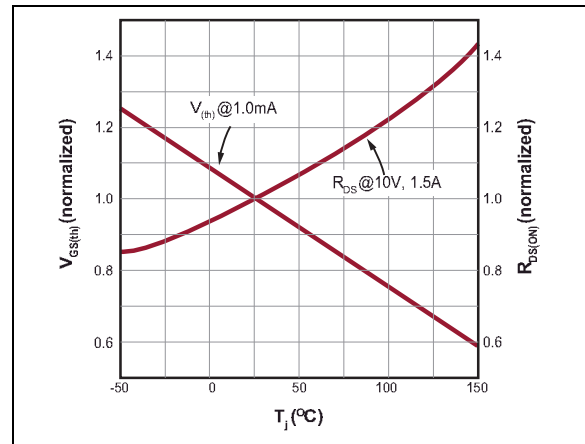


FIGURE 2-11: $V_{(th)}$ and R_{DS} Variation with Temperature.

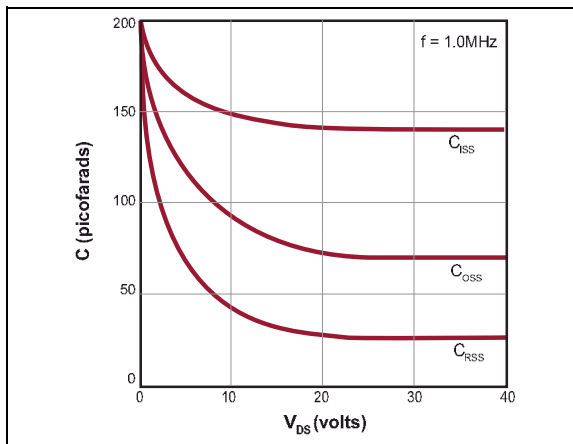


FIGURE 2-9: Capacitance vs. Drain-to-Source Voltage.

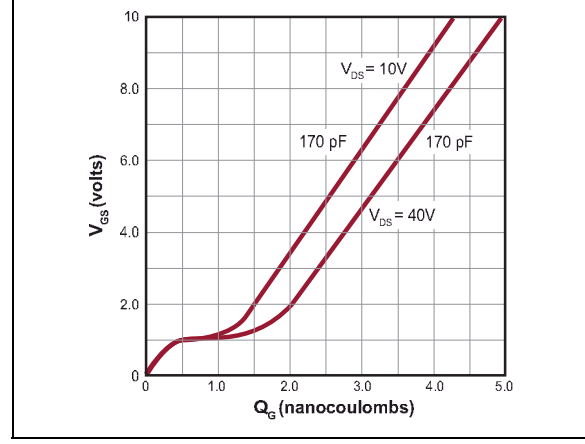


FIGURE 2-12: Gate Drive Dynamic Characteristics.

3.0 PIN DESCRIPTION

Table 3-1 shows the description of pins in TN0604.
Refer to [Package Type](#) for the location of pins.

TABLE 3-1: PIN FUNCTION TABLE

| Pin Number | Pin Name | Description |
|------------|----------|-------------|
| 1 | Source | Source |
| 2 | Gate | Gate |
| 3 | Drain | Drain |

4.0 FUNCTIONAL DESCRIPTION

Figure 4-1 illustrates the switching waveforms and test circuit for TN0604.

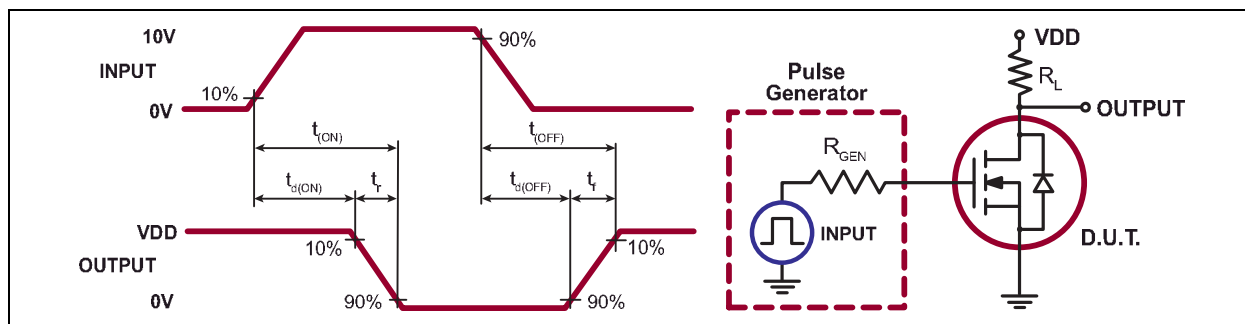


FIGURE 4-1: Switching Waveforms and Test Circuit.

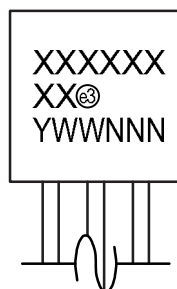
TABLE 4-1: PRODUCT SUMMARY

| BV_{DSS}/BV_{DGS} (V) | $R_{DS(ON)}$ (Maximum) (Ω) | $I_{b(ON)}$ (Minimum) (A) | $V_{GS(th)}$ (Maximum) (V) |
|----------------------------|-------------------------------------------|---------------------------------|----------------------------------|
| 40 | 0.75 | 4 | 1.6 |

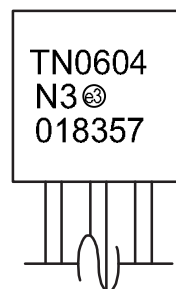
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

3-lead TO-92



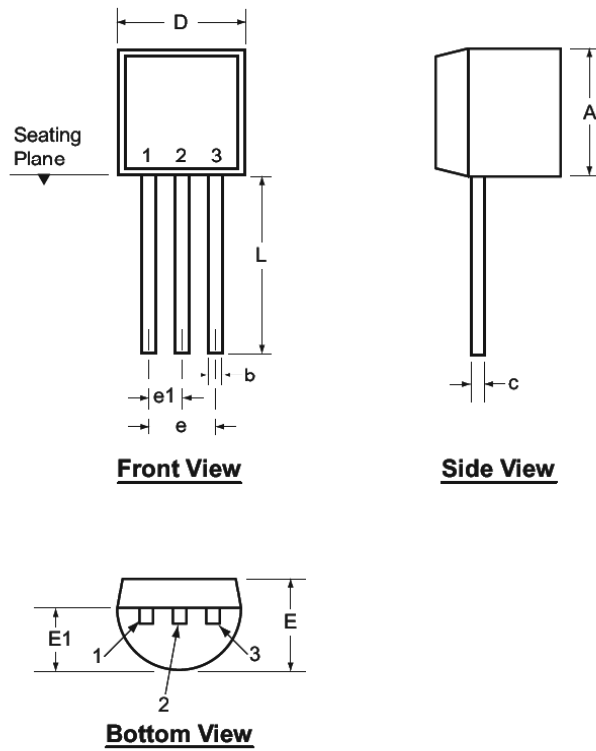
Example



| | | |
|----------------|--------|------------------------------------------------------------------------------------------------------------------|
| Legend: | XX...X | Product Code or Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | ⓔ3 | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator (ⓔ3) can be found on the outer packaging for this package. |

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

3-Lead TO-92 Package Outline (L/LL/N3)



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

| Symbol | | A | b | c | D | E | E1 | e | e1 | L |
|------------------------|-----|------|-------------------|-------------------|------|------|------|------|------|-------|
| Dimensions (inches) | MIN | .170 | .014 [†] | .014 [†] | .175 | .125 | .080 | .095 | .045 | .500 |
| | NOM | - | - | - | - | - | - | - | - | - |
| | MAX | .210 | .022 [†] | .022 [†] | .205 | .165 | .105 | .105 | .055 | .610* |

JEDEC Registration TO-92.

* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

APPENDIX A: REVISION HISTORY

Revision A (July 2020)

- Converted Supertex Doc# DSFP-TN0604 to Microchip DS20005934A
- Created a pin function table
- Changed the package marking format
- Removed the TN0604 N3 P002, P003, and P014 media types
- Updated the packaging medium of the TN0604 N3 P013 media type from 2000/Reel to 2000/Reel (Ammo Pack) to align it with the actual BQM
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

| PART NO. | | | | Examples: | |
|----------------|-----------------|---------------|----------------------------------------------|---------------------|------------------------------------------------------------------------------------|
| Device | Package Options | Environmental | Media Type | | |
| Device: | TN0604 | = | N-Channel Enhancement-Mode Vertical DMOS FET | a) TN0604N3-G: | N-Channel Enhancement-Mode, Vertical DMOS FET, 3-lead TO-92, 1000/Bag |
| Package: | N3 | = | 3-lead TO-92 | b) TN0604N3-G-P005: | N-Channel Enhancement-Mode, Vertical DMOS FET, 3-lead TO-92, 2000/Reel |
| Environmental: | G | = | Lead (Pb)-free/RoHS-compliant Package | c) TN0604N3-G-P013: | N-Channel Enhancement-Mode, Vertical DMOS FET, 3-lead TO-92, 2000/Reel (Ammo Pack) |
| Media Types: | (blank) | = | 1000/Bag for an N3 Package | | |
| | P005 | = | 2000/Reel for an N3 Package | | |
| | P013 | = | 2000/Reel (Ammo Pack) for an N3 Package | | |

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Netherlands - Drunen
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Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
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SYST-07RIBE717 - Data Sheet - TN0604 N-Channel Enhancement-Mode Vertical DMOS FET Data Sheet

Affected Catalog Part Numbers(CPN)

TN0604N3-G

TN0604N3-G-P005

TN0604N3-G-P013