Product Change Notification / SYST-26UVZA349

Date:

29-Jun-2020

Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ERRATA - PIC18F25/45/55Q43 Silicon Errata and Data Sheet Clarifications Document Revision

Affected CPNs:

SYST-26UVZA349_Affected_CPN_06292020.pdf
SYST-26UVZA349_Affected_CPN_06292020.csv

Notification Text:

SYST-26UVZA349

Microchip has released a new Product Documents for the PIC18F25/45/55Q43 Silicon Errata and Data Sheet Clarifications of devices. If you are using one of these devices please read the document located at PIC18F25/45/55Q43 Silicon Errata and Data Sheet Clarifications.

Notification Status: Final

Description of Change: Adding silicon erratum item 1.4.1

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 29 June 2020

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

PIC18F25/45/55Q43 Silicon Errata and Data Sheet Clarifications

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

PIC18F25Q43-E/ML
PIC18F25Q43-E/SO
PIC18F25Q43-E/SP
PIC18F25Q43-E/SS
PIC18F25Q43-E/STX
PIC18F25Q43-I/ML
PIC18F25Q43-I/SO
PIC18F25Q43-I/SP
PIC18F25Q43-I/SS
PIC18F25Q43-I/STX
PIC18F25Q43T-I/ML
PIC18F25Q43T-I/SO
PIC18F25Q43T-I/SS
PIC18F25Q43T-I/STX
PIC18F45Q43-E/ML
PIC18F45Q43-E/MP
PIC18F45Q43-E/P
PIC18F45Q43-E/PT
PIC18F45Q43-I/ML
PIC18F45Q43-I/MP
PIC18F45Q43-I/P
PIC18F45Q43-I/PT
PIC18F45Q43T-I/ML
PIC18F45Q43T-I/MP
PIC18F45Q43T-I/PT
PIC18F55Q43-E/6LX
PIC18F55Q43-E/PT
PIC18F55Q43-I/6LX
PIC18F55Q43-I/PT
PIC18F55Q43T-I/6LX
PIC18F55Q43T-I/PT

PIC18F25/45/55Q43

PIC18F25/45/55Q43 Silicon Errata and Data Sheet Clarifications

The PIC18F25/45/55Q43 devices you have received conform functionally to the current device data sheet (DS40002170B), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC18F25/45/55Q43 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID
		B0
PIC18F25Q43	0x73C0	0xA040
PIC18F45Q43	0x73E0	0xA040
PIC18F55Q43	0x7400	0xA040

Important: Refer to the **Device/Revision ID** section in the current **"PIC18FXXQ43 Family Programming Specification"** (DS40002079) for more detailed information on Device Identification and Revision IDs for your specific device.

Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions
				B0
ADCC	Capacitive Voltage Divider	1.1.1	CVD is only functional on PORTA[2:0] and PORTB[4:0]	X
Oscillator	XT mode	1.2.1	Max. clock frequency limited to 2 MHz for XT mode	X
I2C	I2C	1.3.1	I2CxADR0/1/2/3 registers have incorrect reset value	X
SRAM	SRAM Readback	1.4.1	SRAM readback can be incorrect	X
Note: Only those issues indicated in the last column apply to the current silicon revision.				

Table of Contents

1. Silicon Errata Issues

Notice: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1 Module: Analog-to-Digital Converter with Computation (ADCC)

1.1.1 Capacitive Voltage Divider (CVD)

The CVD feature is only functional on PORTA[2:0] and PORTB[4:0]. This feature is not recommended for use on any other pins.

Work around

None.

Affected Silicon Revisions

B0
X

1.2 Module: Oscillator

1.2.1 Maximum Clock Frequency Limited to 2 MHz for XT Mode

The maximum clock frequency for the intermediate gain setting that supports quartz crystal and ceramic resonator operation, XT mode, is being reduced from 4 MHz to 2 MHz.

Work around

For crystal or resonator frequencies above 2 MHz, use HS mode.

Affected Silicon Revisions

B0
X

1.3 Module: I^2C

1.3.1 I2CxADR0/1/2/3 Registers Have Incorrect Reset Value

The I2CxADR0/1/2/3 registers reset to 0xFF when the I2CxMD is enabled instead of 0x00.

Work around

None.

Affected Silicon Revisions

B0
X

1.4 Module: SRAM

1.4.1 SRAM Readback

Following a device power up sequence, there is a possibility that some SRAM locations will not return the expected written value but will read back '00' instead.

Work around

None. The device can only recover by power cycling.

This erroneous condition can be detected by running the following code that writes non-zero values to SRAM and then verifies the returned read values are not '00'. If a returned value is '00', the application code should be put into a safe state until a POR event occurs. This code should be executed immediately after power-up. If the test passes, device operation will be normal.

```
// SRAM test

FSR0 = 0xcff;         // Write data into RAM address for devices up to 2K RAM
INDF0 = 0x55;
PROD = INDF0;         // Read back data
if (PROD == 0){
    SAFE_STATE();     // RAM incorrectly read, suspend operation and go to safe state
}

//For devices with more than 2K of SRAM add the following code
FSR0 = 0x14ff;        // Write data into RAM
INDF0 = 0x55;
PROD = INDF0;         // Read back data
if (PROD == 0){
    SAFE_STATE();     // RAM incorrectly read, suspend operation and go to safe state
}

//For devices with more than 4K of SRAM add the following code
FSR0 = 0x24ff;        // Write data into RAM
INDF0 = 0x55;
PROD = INDF0;         // Read back data
if (PROD == 0){
    SAFE_STATE();     // RAM incorrectly read, suspend operation and go to safe state
}
```

Affected Silicon Revisions

B0
X

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (40002170B):

Note:

Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1 Module: Temperature Indicator

2.1.1 Temperature Calculation

Equation 39-1 used to calculate the temperature using the ADC reading of the internal temperature indicator module is incorrect. The corresponding code example, **Example 39-1**, is also incorrect. The correct equation and modified code example are shown below.

Equation 39-1: Sensor Temperature (in °C)

$$T_{MEAS} = \frac{\frac{(ADC_{MEAS} \times Gain)}{256} + Offset}{10}$$

Example 39-1: Temperature Calculation (°C)

```
// offset is int16_t data type
// gain is int16_t data type
// ADC_MEAS is uint16_t data type
// Temp_in_C is int24_t data type

ADC_MEAS = ((ADRESH << 8) + ADRESL);        // Store the ADC Result
Temp_in_C = (int24_t)(ADC_MEAS) * gain;     // Multiply the ADC Result by
                                            // Gain and store the result in a
                                            // signed variable
Temp_in_C = Temp_in_C / 256;                // Divide (ADC Result * Gain) by 256
Temp_in_C = Temp_in_C + offset;             // Add (Offset) to the result
Temp_in_C = Temp_in_C / 10;                 // Divide the result by 10 and store
                                            // the calculated temperature
```

3. APPENDIX A: Revision History

Doc Rev.	Date	Comments
E	06/2020	Adding silicon erratum item 1.4.1
D	06/2020	Adding silicon erratum item 1.3.1
C	04/2020	Adding XT mode erratum and Temperature Indicator data sheet clarification.
B	02/2020	Add working pins for CVD.
A	12/2019	Initial document release.

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