Product Change Notification - SYST-30SVKR031

Date:

04 May 2020

Product Category:

32-bit Microcontrollers

Affected CPNs:

Notification subject:

ERRATA - PIC32MM0256GPM064 Family Silicon Errata and Data Sheet Clarification

Notification text:

SYST-30SVKR031

Microchip has released a new Product Documents for the PIC32MM0256GPM064 Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at PIC32MM0256GPM064 Family Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change: 1) Added Silicon Revision A4. 2) Added silicon issue 26 (UART).
Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Estimated First Ship Date: 04 June 2020
NOTE: Please be advised that after the estimated first ship date customers may receive pre and post change parts.

Markings to Distinguish Revised from Unrevised Devices: Traceability Code

Attachment(s):

PIC32MM0256GPM064 Family Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

PIC32MM0064GPM028-E/M6
PIC32MM0064GPM028-E/ML
PIC32MM0064GPM028-E/SS
PIC32MM0064GPM028-I/M6
PIC32MM0064GPM028-I/ML
PIC32MM0064GPM028-I/SS
PIC32MM0064GPM028T-I/M6
PIC32MM0064GPM028T-I/ML
PIC32MM0064GPM028T-I/SS
PIC32MM0064GPM036-E/M2
PIC32MM0064GPM036-E/MV
PIC32MM0064GPM036-I/M2
PIC32MM0064GPM036-I/MV
PIC32MM0064GPM036T-I/M2
PIC32MM0064GPM036T-I/MV
PIC32MM0064GPM048-E/M4
PIC32MM0064GPM048-E/PT
PIC32MM0064GPM048-I/M4
PIC32MM0064GPM048-I/PT
PIC32MM0064GPM048T-I/M4
PIC32MM0064GPM048T-I/PT
PIC32MM0064GPM064-E/MR
PIC32MM0064GPM064-E/PT
PIC32MM0064GPM064-I/MR
PIC32MM0064GPM064-I/PT
PIC32MM0064GPM064T-I/MR
PIC32MM0064GPM064T-I/PT
PIC32MM0128GPM028-E/M6
PIC32MM0128GPM028-E/ML
PIC32MM0128GPM028-E/SS
PIC32MM0128GPM028-I/M6
PIC32MM0128GPM028-I/ML
PIC32MM0128GPM028-I/SS
PIC32MM0128GPM028T-I/M6
PIC32MM0128GPM028T-I/ML
PIC32MM0128GPM028T-I/SS
PIC32MM0128GPM036-E/M2
PIC32MM0128GPM036-E/MV
PIC32MM0128GPM036-I/M2
PIC32MM0128GPM036-I/MV
PIC32MM0128GPM036T-I/M2
PIC32MM0128GPM036T-I/MV
PIC32MM0128GPM048-E/M4
PIC32MM0128GPM048-E/PT
PIC32MM0128GPM048-I/M4
PIC32MM0128GPM048-I/PT

PIC32MM0128GPM048T-I/M4
PIC32MM0128GPM048T-I/PT
PIC32MM0128GPM064-E/MR
PIC32MM0128GPM064-E/PT
PIC32MM0128GPM064-I/MR
PIC32MM0128GPM064-I/PT
PIC32MM0128GPM064T-I/MR
PIC32MM0128GPM064T-I/PT
PIC32MM0256GPM028-E/M6
PIC32MM0256GPM028-E/ML
PIC32MM0256GPM028-E/SS
PIC32MM0256GPM028-E/SSVAO
PIC32MM0256GPM028-I/M6
PIC32MM0256GPM028-I/ML
PIC32MM0256GPM028-I/MLVAO
PIC32MM0256GPM028-I/SS
PIC32MM0256GPM028T-I/M6
PIC32MM0256GPM028T-I/ML
PIC32MM0256GPM028T-I/ML026
PIC32MM0256GPM028T-I/ML028
PIC32MM0256GPM028T-I/MLVAO
PIC32MM0256GPM028T-I/SS
PIC32MM0256GPM036-E/M2
PIC32MM0256GPM036-E/MV
PIC32MM0256GPM036-I/M2
PIC32MM0256GPM036-I/MV
PIC32MM0256GPM036T-I/M2
PIC32MM0256GPM036T-I/MV
PIC32MM0256GPM036T-I/MVC36
PIC32MM0256GPM064-E/MR
PIC32MM0256GPM064-E/PT
PIC32MM0256GPM064-I/MR
PIC32MM0256GPM064-I/PT
PIC32MM0256GPM064T-I/MR
PIC32MM0256GPM064T-I/PT
PIC32MM0256GPM064T-I/PT023
PIC32MM0256GPM064T-I/PT025

PIC32MM0256GPM064 Family Silicon Errata and Data Sheet Clarification

The PIC32MM0256GPM064 family devices that you have received conform functionally to the current Device Data Sheet (DS60001387**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC32MM0256GPM064 silicon.

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A4**).

Data Sheet clarifications and corrections start on page 10, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

> **Note:** If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC32MM0256GPM064 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)				Part Number	Device ID(1)	Revision ID for Silicon Revision(2)			
		A1	A2	A3	A4			A1	A2	A3	A4
PIC32MM0064GPM028	0x7708	01h	02h	03h	04h	PIC32MM0064GPM048	0x772C	01h	02h	03h	04h
PIC32MM0128GPM028	0x7710					PIC32MM0128GPM048	0x7734				
PIC32MM0256GPM028	0x7718					PIC32MM0256GPM048	0x773C				
PIC32MM0064GPM036	0x770A					PIC32MM0064GPM064	0x770E				
PIC32MM0128GPM036	0x7712					PIC32MM0128GPM064	0x7716				
PIC32MM0256GPM036	0x771A					PIC32MM0256GPM064	0x771E				

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC32MM Families Flash Programming Specification"* (DS60001364) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions			
				A1	A2	A3	A4
ADC	12-Bit Conversion	1.	The ADC may miss one or more of the following codes in 12-bit mode: 1023, 2046, 2047, 3070 and 3071.	X	X	X	X
ADC	Format Options	2.	32-bit signed format option is the same as the 16-bit signed format option.	X	X	X	X
UART	Receive Buffer Overflow Disable	3.	Overflow disable feature controlled by the OVFDIS bit is not functional.	X			
MCCP	OCM3A Output	4.	The OCM3A output for MCCP3 is not functional.	X	X	X	X
Primary Oscillator	Primary Oscillator Start-up Timer (OST)	5.	The Primary Oscillator Start-up Timer (OST) may indicate the oscillator is ready for use and set the POSCRDY (CLKSTAT[2]) bit too early.	X	X	X	X
Reset	Reset	6.	Current consumption in Reset is high.	X	X	X	X
Timer1	External Clock Mode	7.	Timer1 does not overflow in External Clock mode when PR1 = 1 and the prescaler is 1:1.	X	X	X	X
Timer1	External Clock Mode	8.	The first increment value is not visible when using External Clock mode and a 1:1 prescaler.	X	X	X	X
I^2C Slave	I^2C Slave	9.	I^2C line does not return to Idle after receiving a NACK from the Master. Writes to I2CxTRN are not ignored in this condition.	X	X	X	X
I^2C Slave	I^2C Slave	10.	Slave reports a Bus Collision (BLC) for every transaction when SBCDE is enabled.	X	X	X	X
I^2C Slave	I^2C Slave	11.	When BOEN = 0, RBF = 0 and I2COV = 1, a NACK is generated but the address is not received.	X	X	X	X
I^2C Slave	I^2C Slave	12.	The Slave may ACK subsequent data after it has gone Idle after a NACK.	X	X	X	X
I^2C Slave	I^2C Slave	13.	The Slave will not Acknowledge reserved addresses in the '111_10xx' range, regardless of the STRICT setting.	X	X	X	X
Power	Retention Sleep	14.	When the device wakes up from Retention Sleep mode, a device Reset may occur. The BOR, POR and EXTR bits in the RCON register are set erroneously for this Reset.	X			
Programming	Programming	15.	The JTAG TDO (RC9) pin toggles during programming when using the PGEC1/ PGED1 or PGEC2/PGED2 pairs.	X			
Oscillator	Secondary Oscillator (SOSC)	16.	Enabling POSC in XT or HS mode may inhibit SOSC operation.	X			
ADC	ADC Performance	17.	Enabling POSC in XT or HS mode may degrade ADC performance.	X			
Power	BOR	18.	BOR: The main BOR may not function.	X	X		
I/O	Schmitt Trigger Inputs	19.	Schmitt Trigger inputs may have glitches with slow signal rise/fall times.	X	X		
SPI	SRMT Bit	20.	In SPI Slave mode, the SRMT bit may be set if the FIFO or Shift register is not empty.	X	X	X	X

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions			
				A1	A2	A3	A4
ICSP™ Programming	Programming	21.	Programming in Retention Sleep.	X	X		
ICSP Programming	Programming	22.	Self-programming after a POR or $\overline{\text{MCLR}}$ Reset.	X	X		
MCCP	Single Edge Compare Mode	23.	The Single Edge Compare mode does not work when the Timebase Prescaler is not 1:1.	X	X		
Reset	Configuration Mismatch	24.	The CMR bit in RCON may be erroneously set after a POR, BOR or when exiting Retention Sleep.	X	X		
ADC	Current	25.	ADC draws additional current when enabled.	X	X	X	
UART	UART	26.	The Stop bit is short by one baud clock.	X	X	X	

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

1. Module: ADC

The ADC may miss one or more of the following codes in 12-bit mode: 1023, 2046, 2047, 3070 and 3071.

Work around

There is no work around in 12-bit mode. If all codes are desired in the application, use 10-Bit Operating mode.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X	X	X				

2. Module: ADC

The 32-bit signed format option is the same as the 16-bit signed format option.

Work around

Use software to correct the output format. Sign-extend the ADC module's 16-bit signed integer output to a 32-bit signed integer. Using the MPLAB® XC32 C compiler, this can be accomplished by casting the ADC1BUFx SFR contents to a volatile short type, followed by a cast to a volatile int type.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X	X	X				

3. Module: UART

The overflow disable feature controlled by the OVFDIS bit is not functional.

Work around

None.

Affected Silicon Revisions

A1	A2	A3	A4				
X							

4. Module: MCCP

The OCM3A output for MCCP3 is not functional.

Work around

Select the OCM3B, OCM3C, OCM3D output, or use MCCP1 OCM1A or MCCP2 OCM2A output.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X	X	X				

5. Module: Primary Oscillator

The Primary Oscillator Start-up Timer (OST) may indicate the oscillator is ready for use and set the POSCRDY (CLKSTAT[2]) bit too early. Clocking the device before the oscillator is ready may result in incorrect execution and exceptions.

Work around

Make sure that the Primary Oscillator clock is ready before using it by following these steps:

1. Running on non-POSC source, request the POSC clock using a peripheral such as REFO.
2. Provide a delay to stabilize POSC.
3. Switch to the POSC source.

Example 1 shows a work around for the device power-on and Example 2 shows the work around when the device wakes from Sleep.

EXAMPLE 1: USING POSC AT POWER-ON

```
#pragma  config FNOSC = FRCDIV        // Oscillator Selection bits (Fast RC oscillator (FRC))
// Clock Switching Enabled (Failsafe Clock Monitor can be enabled or disabled)
#pragma  config FCKSM = CSECMD
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
void    main()
{
// configure REFO to request POSC
REFO1CONbits.ROSEL = 2;               // POSC = 2
REFO1CONbits.OE = 0;                  // disable output
REFO1CONbits.ON = 1;                  // enable module
// wait for POSC stable clock
// this delay may vary depending on different application conditions
// such as voltage, temperature, layout, XT or HS mode and components
{ // delay for 9 ms
unsigned int start = __builtin_mfc0(_CP0_COUNT, _CP0_COUNT_SELECT);
while((__builtin_mfc0(_CP0_COUNT, _CP0_COUNT_SELECT)) - start < (unsigned int)(0.009*8000000/2));
}
// unlock OSCCON
SYSKEY = 0;
SYSKEY = 0xAA996655;
SYSKEY = 0x556699AA;
// switch to POSC = 2
OSCCONCLR = _OSCCON_NOSC_MASK | _OSCCON_CLKLOCK_MASK | _OSCCON_OSWEN_MASK;
OSCCONSET = (2<<_OSCCON_NOSC_POSITION) | _OSCCON_OSWEN_MASK;
while(OSCCONbits.OSWEN == 1);         // wait for switch
```

EXAMPLE 2: USING POSC WHEN AWAKENED FROM SLEEP

```
// Clock Switching Enabled (Failsafe Clock Monitor can be enabled or disabled)
#pragma  config FCKSM = CSECMD
// unlock OSCCON
SYSKEY = 0;
SYSKEY = 0xAA996655;
SYSKEY = 0x556699AA;
// switch to FRC = 0 before entering to sleep
OSCCONCLR = _OSCCON_NOSC_MASK | _OSCCON_CLKLOCK_MASK | _OSCCON_OSWEN_MASK;
OSCCONSET = (0<<_OSCCON_NOSC_POSITION) | _OSCCON_OSWEN_MASK;
while(OSCCONbits.OSWEN == 1);                 // wait for switch
// enter sleep mode
asm      volatile("wait");
// configure REFO to request POSC
REFO1CONbits.ROSEL = 2;                       // POSC = 2
REFO1CONbits.OE = 0;                          // disable output
REFO1CONbits.ON = 1;                          // enable module
// wait for POSC stable clock
// this delay may vary depending on different application conditions
// such as voltage, temperature, layout, XT or HS mode and components
{ // delay for 9 ms
unsigned int start = __builtin_mfc0(_CP0_COUNT, _CP0_COUNT_SELECT);
while((__builtin_mfc0(_CP0_COUNT, _CP0_COUNT_SELECT)) - start < (unsigned int)(0.009*8000000/2));
}
// switch to POSC = 2
OSCCONCLR = _OSCCON_NOSC_MASK | _OSCCON_CLKLOCK_MASK | _OSCCON_OSWEN_MASK;
OSCCONSET = (2<<_OSCCON_NOSC_POSITION) | _OSCCON_OSWEN_MASK;
while(OSCCONbits.OSWEN == 1);                 // wait for switch
```

Affected Silicon Revisions

A1	A2	A3	A4				
X	X	X	X				

6. Module: Reset

Current consumption in Master Clear Reset is high.

Work around

Do not use $\overline{\text{MCLR}}$ to hold device in Reset to save power.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X	X	X				

7. Module: Timer1

Timer1 does not overflow in External Clock mode when PR1 = 1 and the prescaler is 1:1.

Work around

Use a PR1 value greater than one.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X	X	X				

8. Module: Timer1

The first increment value is not visible when using External Clock mode and a 1:1 prescaler.

Work around

None.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X	X	X				

9. Module: I²C Slave

The I²C line does not return to Idle after receiving a NACK from the Master. Writes to I2CxTRN are not ignored in this condition.

Work around

Do not write to the I2CxTRN register after a NACK has been received.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X	X	X				

10. Module: I²C Slave

Slave reports a Bus Collision (BLC) for every transaction when SBCDE is enabled.

Work around

Do not enable SBCDE.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X	X	X				

11. Module: I²C Slave

When BOEN = 0, RBF = 0 and I2COV = 1, a NACK is generated but the address is not received.

Work around

Service the receive buffer to prevent an overflow.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X	X	X				

12. Module: I²C Slave

The Slave may ACK subsequent data after it has gone Idle after a NACK.

Work around

The Master should not send data following a NACK without generating a Start condition

Affected Silicon Revisions

A1	A2	A3	A4				
X	X	X	X				

13. Module: I²C Slave

The Slave will not Acknowledge reserved addresses in the '111_10xx' range, regardless of the STRICT bit setting.

Work around

None.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X	X	X				

14. Module: Power

When the device wakes up from Retention Sleep mode, a device Reset may occur. The BOR, POR and EXTR bits in RCON register are set erroneously for this Reset.

Work around

To provide a consistent behavior when the device wakes up from the Retention Sleep mode, the software sequence should be performed following the `SLEEP` instruction. In this case, a Reset will always be generated when the device wakes up from Retention Sleep.

Affected Silicon Revisions

A1	A2	A3	A4				
X							

15. Module: Programming

The JTAG TDO (RC9) pin toggles during programming when using the PGEC1/PGED1 or PGEC2/PGED2 pairs.

Work around

Do not connect external circuitry to the TDO pin that cannot tolerate toggling when programming using the PGEC1/PGED1 or PGEC2/PGED2 pins.

Affected Silicon Revisions

A1	A2	A3	A4				
X							

16. Module: Oscillator

Enabling POSC in XT or HS mode may inhibit SOSC operation.

Work around

If SOSC operation is required, use FRC or FRCPLL instead of POSC.

Affected Silicon Revisions

A1	A2	A3	A4				
X							

17. Module: ADC

Enabling POSC in XT or HS mode may degrade ADC performance in 10-bit and 12-bit mode.

Work around

If ADC operation that meets the data sheet specification is required, use FRC or FRCPLL instead of POSC.

Affected Silicon Revisions

A1	A2	A3	A4				
X							

18. Module: Power

The main BOR may not occur when the operating voltage drops below the BOR trip voltage.

Work around

Ensure the device operating voltage does not violate the specified values.

Use an external supervisor circuit to reset the device if the operating voltage can be outside the specified values.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X						

19. Module: I/O

If the input signal rise or fall time is more than 500 nS, the I/O Schmitt Trigger output may have glitches.

Work around

The rise/fall time of the input signal must be less than 500 nS.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X						

20. Module: SPI

In SPI Slave mode, the SRMT bit may be set if the FIFO or Shift register is not empty.

Work around

The following work arounds can be implemented in the application to detect when the FIFO and Shift register are empty:

1. Check the SPITBF bit before checking the SRMT bit. If the SPITBF flag is cleared and the SRMT flag is set, then all data were transmitted. Example 3 demonstrates the SPITBF and SRMT bits polling.
2. Read the SRMT bit twice, back-to-back. If the SRMT bit is set two reads in a row, then the FIFO and Shift register are empty. Example 4 demonstrates the SRMT bit polling using double read.

EXAMPLE 3: EMPTY STATUS DETECTION USING SPITBF AND SRMT BITS POLLING

```
// Both flags must indicate empty status.
while(SPI1STATLbits.SPITBF);
while(!SPI1STATLbits.SRMT);
```

EXAMPLE 4: EMPTY STATUS DETECTION USING SRMT BIT POLLING WITH BACK-TO-BACK READS

```
// If SRMT bit is set two reads in a row
   then it set correctly.
asm  volatile("\n\
la   $t0, SPI1STAT;\
loop:;\
lw   $t1, 0($t0);\
lw   $t2, 0($t0);\
and  $t1, $t1, $t2;\
andi $t1, $t2, 0x80;\
beqz $t1, loop;");
```

Affected Silicon Revisions

A1	A2	A3	A4				
X	X	X	X				

21. Module: ICSP™ Programming

After a POR or $\overline{\text{MCLR}}$ Reset, the device may fail to program if Retention Sleep is invoked within 40 ms.

Work around

Provide a delay in firmware to ensure the device does not enter Retention Sleep within 40 ms of a POR or $\overline{\text{MCLR}}$ Reset.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X						

22. Module: ICSP Programming

After a POR or $\overline{\text{MCLR}}$ Reset, the device may fail to program using ICSP if user firmware performs self-programming within 40 ms.

Work around

Provide a delay in firmware to ensure the device does not perform self-programming within 40 ms of a POR or $\overline{\text{MCLR}}$ Reset.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X						

23. Module: MCCP

The Single Edge Compare mode does not work when the Timebase Prescaler is not 1:1.

Work around

Use 1:1 Prescaler value.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X						

24. Module: Reset

The CMR bit in RCON may be erroneously set after a POR, BOR or when exiting Retention Sleep.

Work around

Clear the CMR bit following a POR, BOR or exit from Retention Sleep.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X						

25. Module: ADC

On some devices, the current draw may increase by up to 12 mA when the ADC is enabled. This current draw is not affected by the device Power Save modes or ADC configuration. This additional current does not affect the ADC or device performance.

Work around

Disable the ADC when it is not converting or not used in the application.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X	X					

26. Module: UART

The Stop bit is short by one baud clock. In BRGH = 0 mode, the Stop bit is short by 1/16 bit time. In BRGH = 1 mode, the Stop bit is short by 1/4 bit time. When two Stop bits are enabled, the total Stop bit time is short by 1/16 or 1/4 bit time based on the BRGH mode.

Work around

1. Use a timer driven interrupt to write data to the UART Transmit Shift register, one byte at a time. The timer period must be greater than the sum of the number of bits in the serial data, the Start bit and the Stop bit(s). The difference in time between interrupt timer period and the sum of bit time creates the line Idle time needed to extend the Stop bit.

   For example, at 9600 baud, eight data bits, one Stop bit: 10 * 104.17 µs = 1041.7 µs. The time between writes to the UART TX buffer must be greater than 1041.7 µs

2.a If only transmission is required, use two Stop bits. This will be interpreted by a UART configured for one Stop bit as one Stop bit and a 15/16 bit time line Idle.

2.b If transmit and receive are required, use two UARTs. Configure one for transmit (as described in #1 above); configure the other UART for receive with one Stop bit.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X	X					

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001387**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (3/2017)

Initial release of this document; issued for revision A1.

Rev B Document (5/2017)

Adds silicon revision **A2.**

Updates Table 1 and Table 2.

Adds new silicon issues 18 (Power), 19 (I/O), 20 (SPI) and 21 (ICSP™ Programming).

Rev C Document (6/2017)

Updates Table 2.

Adds new silicon issues 22 (ICSP Programming).

Adds new data sheet clarification 1 (Electrical Characteristics).

Rev D Document (7/2018)

Adds silicon revision **A3**.

Adds new silicon issues 23 (MCCP) and 24 (Reset).

Removes data sheet clarification 1 (Electrical Characteristics) since this issue was corrected in the latest data sheet revision DS60001387**C**.

Rev E Document (1/2019)

Adds silicon issue 25 (ADC).

Rev F Document (4/2020)

Adds silicon revision **A4**.

Adds silicon issue 26 (UART).

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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